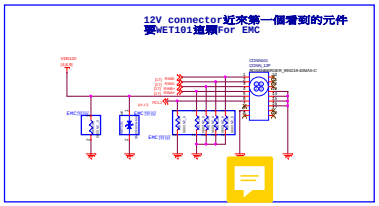
HSD CONN



PDB Control

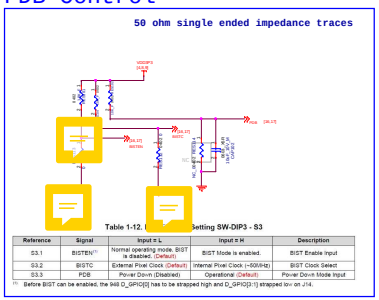
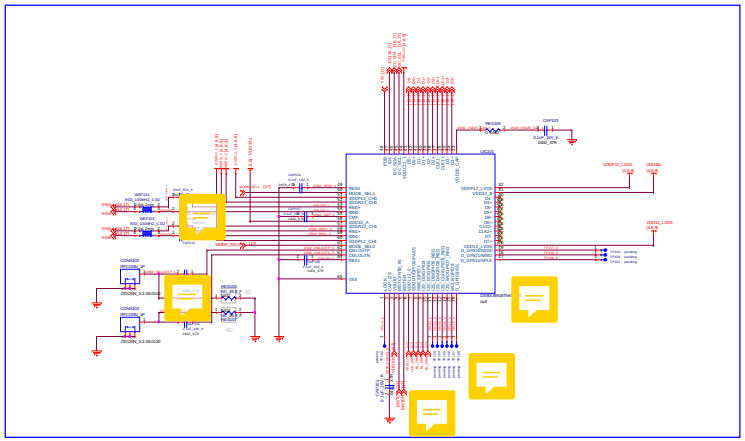


Table 1-12. Setting SW-DIP3 - S3

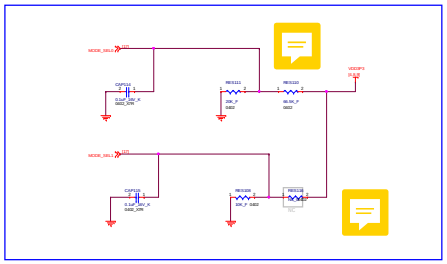
Reference	Signal	Input = L	Input = H	Description
S3.1	BISTEN(1)	Normal operating mode. BIST is disabled. (Default)	BIST Mode is enabled.	BIST Enable Input
S3.2	BISTC	External Pixel Clock (Default)	Internal Pixel Clock (~600Mhz)	BIST Clock Select
S3.3	PDB	Power Down (Disabled)	Operational (Default)	Power Down Mode Input

(1) Before BIST can be enabled, the 948 D_GPIO[0] has to be strapped high and D_GPIO[3:1] strapped low on J14.

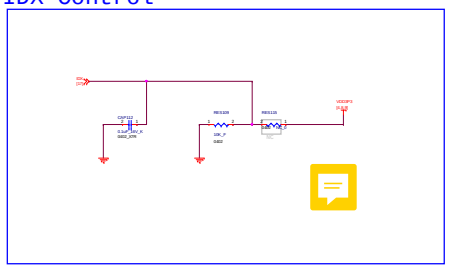
Controller



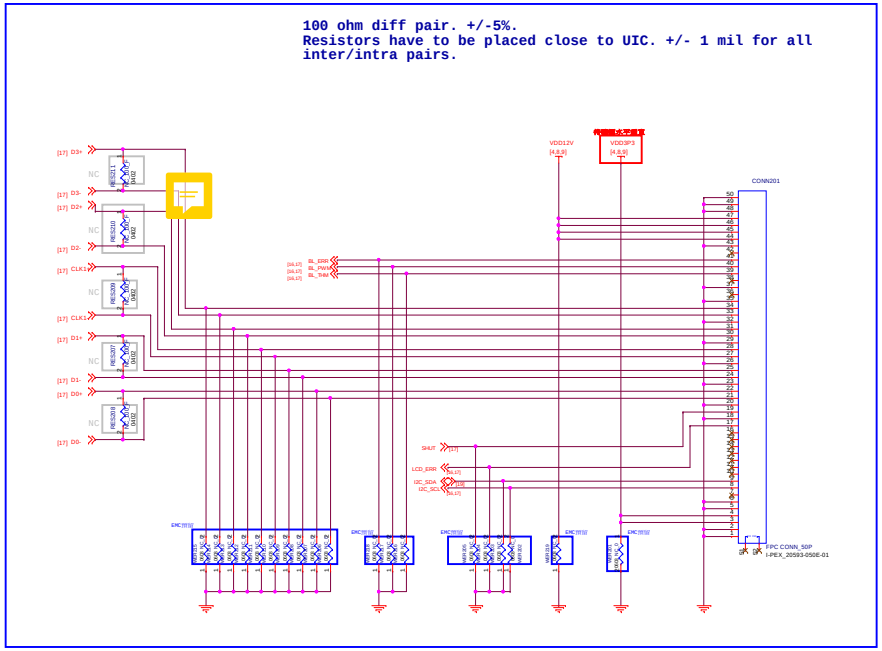
MODE_SEL0/1 Control



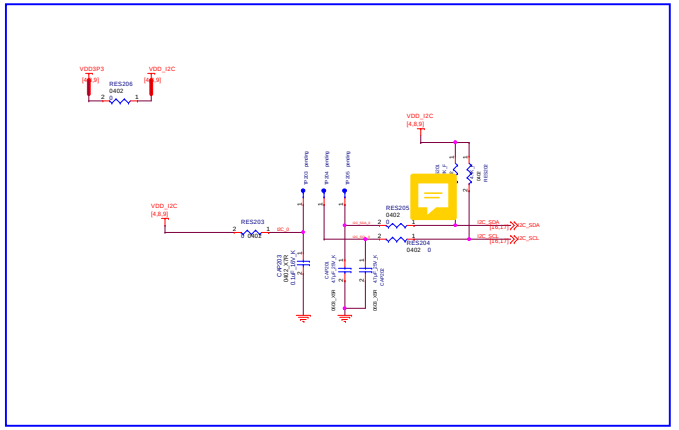
IDX Control



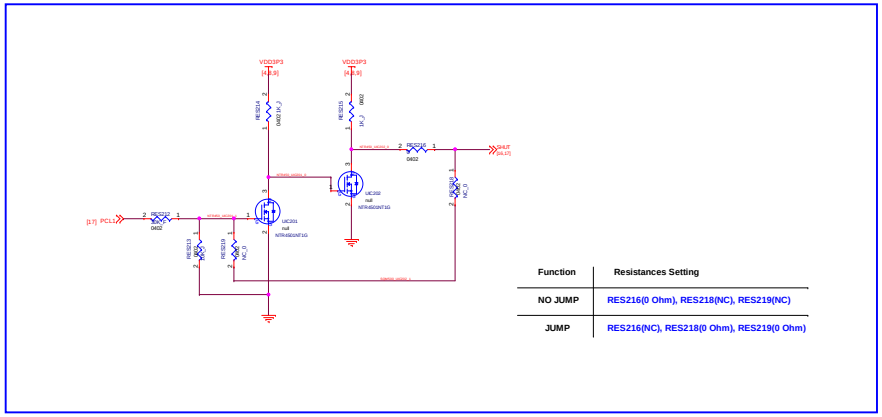
FPC CONN



External I2C connection

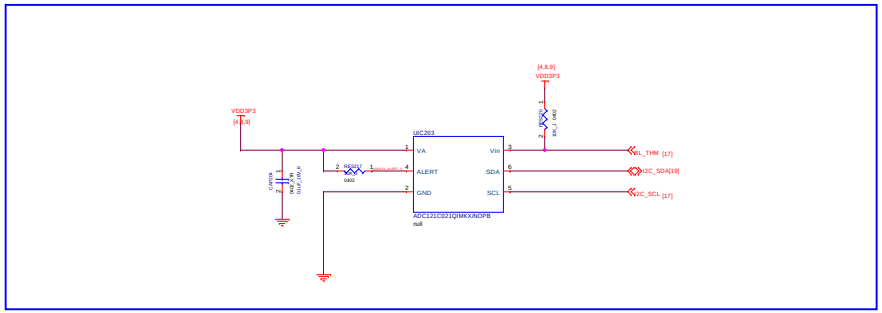


N-MOFET_Confirm PCL1



Function	Resistances Setting
NO JUMP	RES216(0 Ohm), RES218(NC), RES219(NC)
JUMP	RES216(NC), RES218(0 Ohm), RES219(0 Ohm)

ADC converter to I2C



Title	02_Output and Termination_Jossen
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Rev	<RevCode>
Date	Thursday, June 03, 2021
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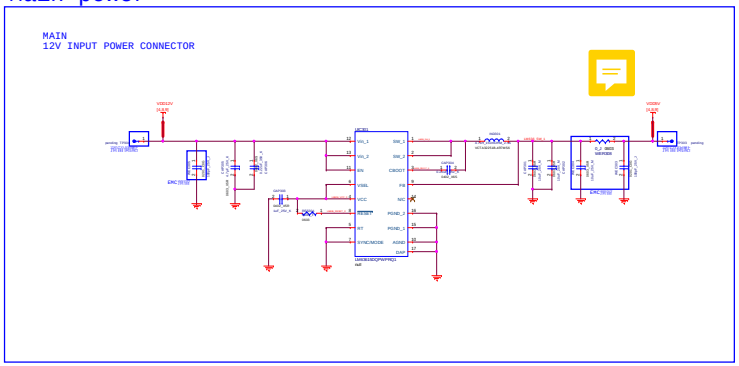
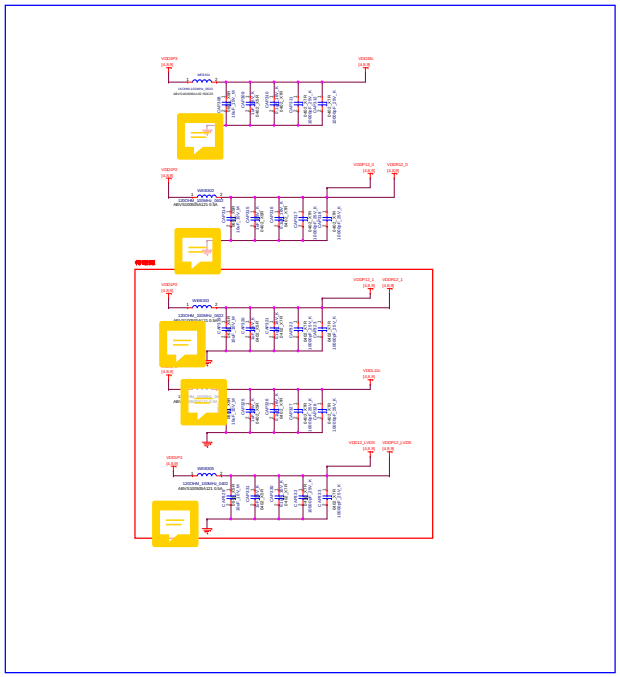
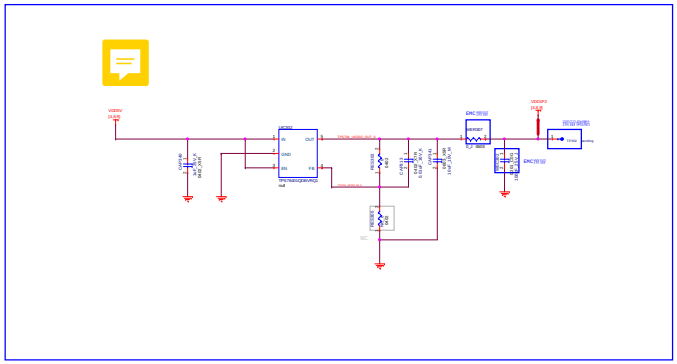
Main power



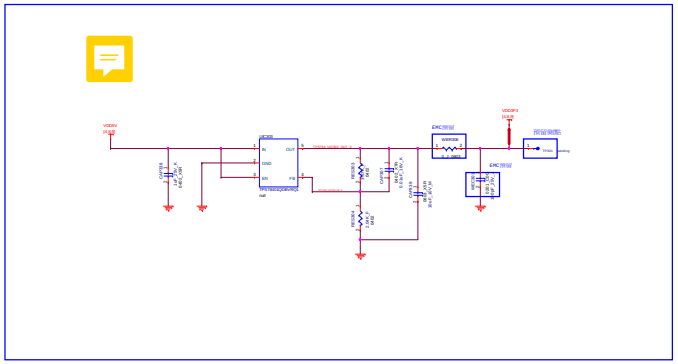
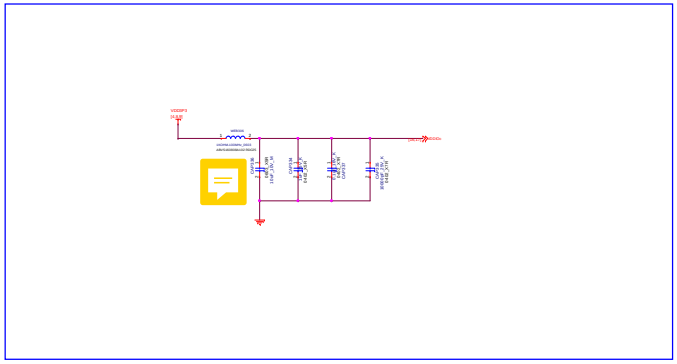
需靠近至UIC101,並放置在Bottom layer



1V2_Power Supply



3V3_Power Supply



需靠近至UIC101,並放置在Bottom layer