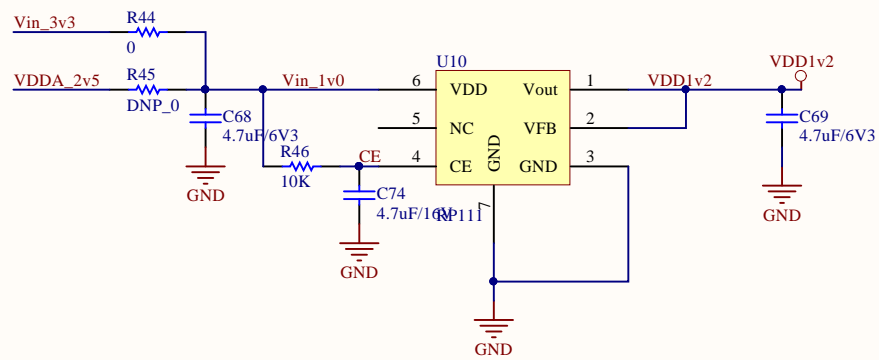
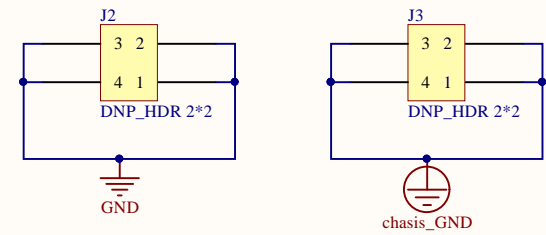
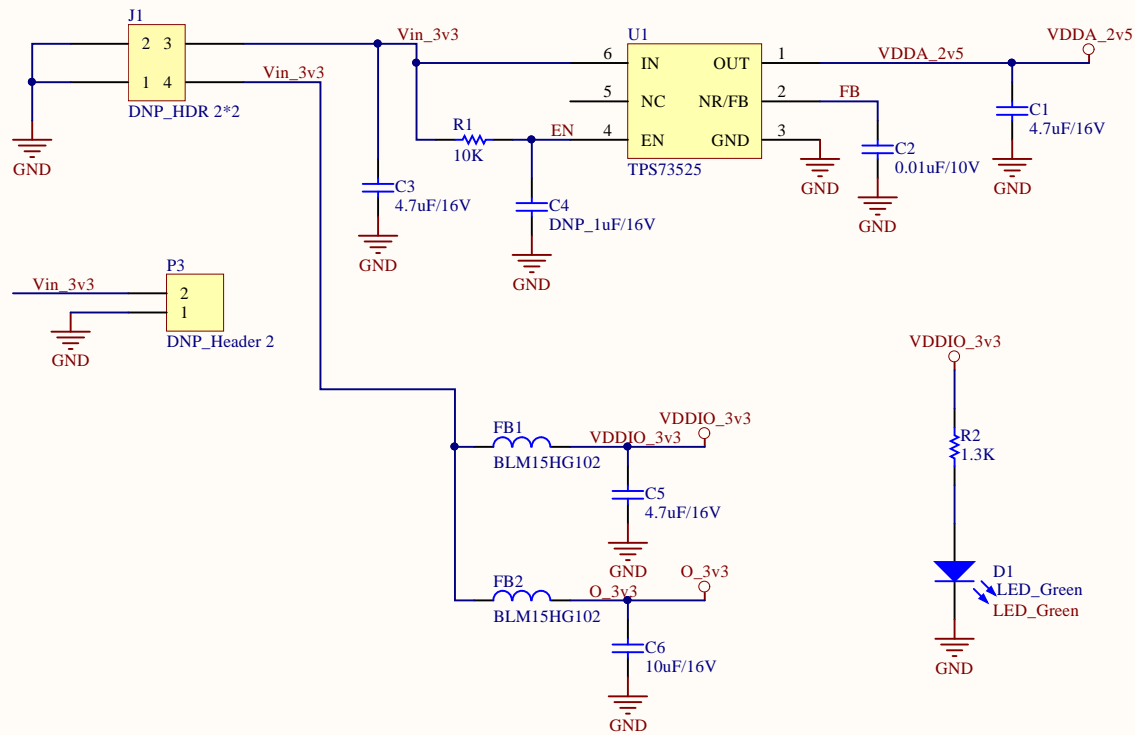
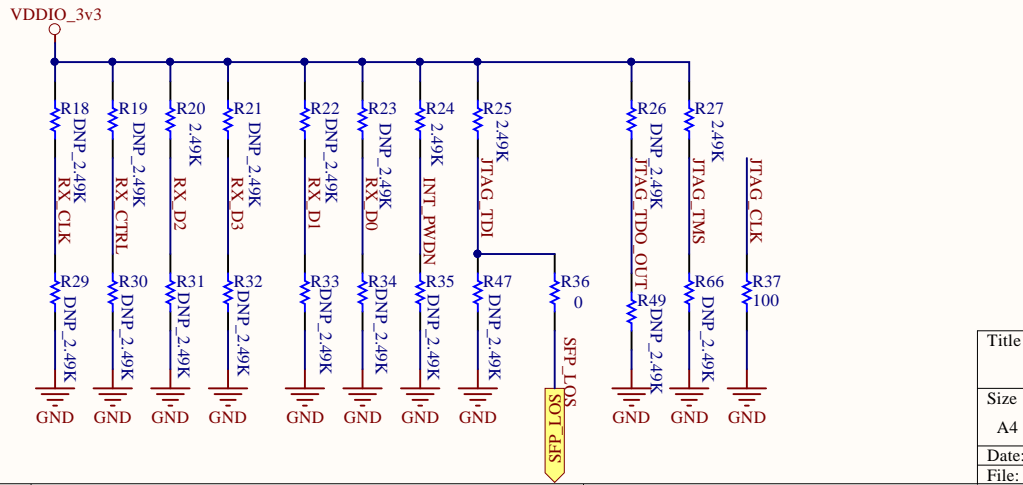
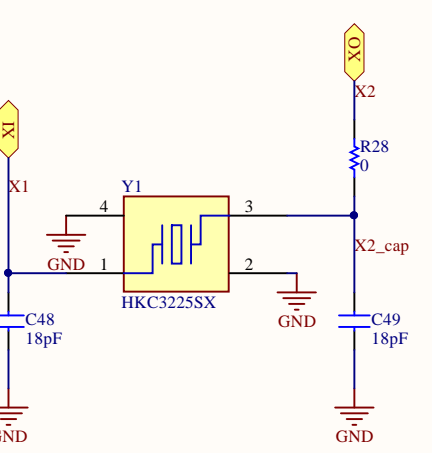
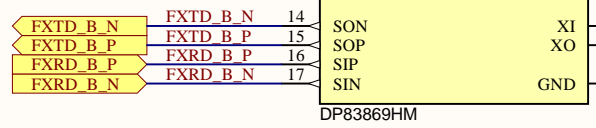
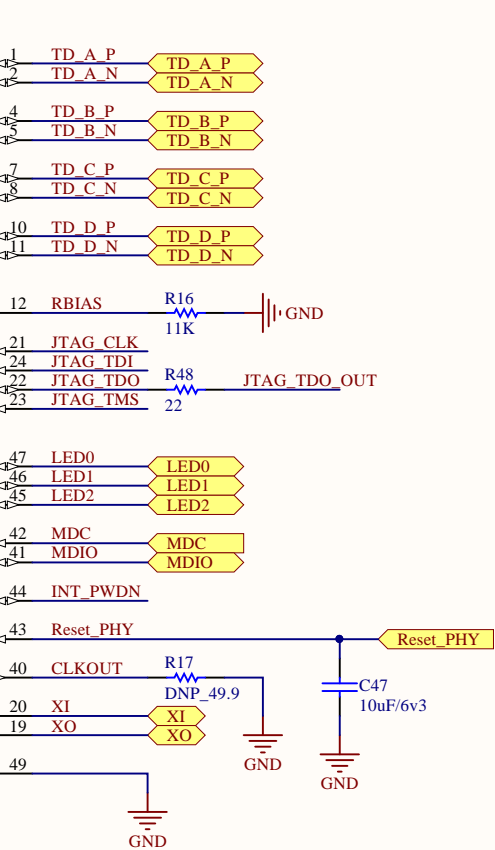
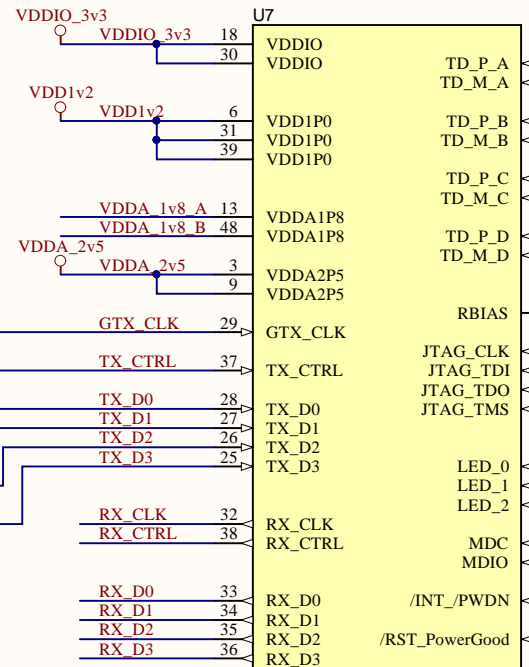
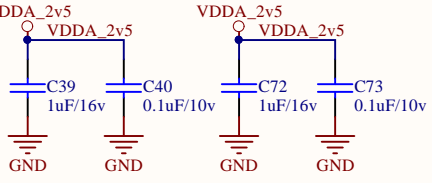
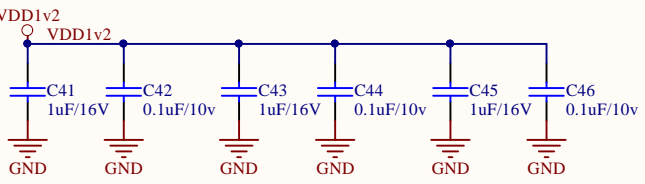
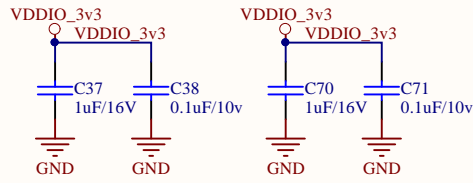
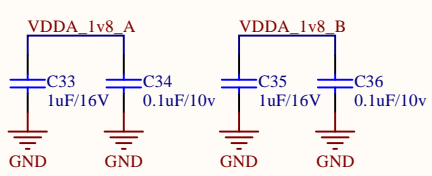


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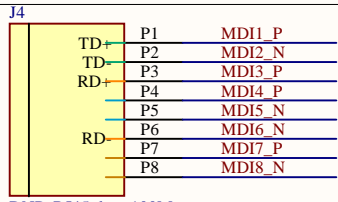


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VDDA_1v8
Unused: No cap
Ex-Used: Add cap



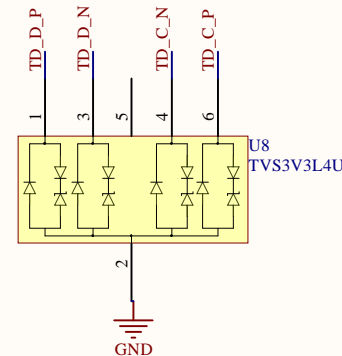
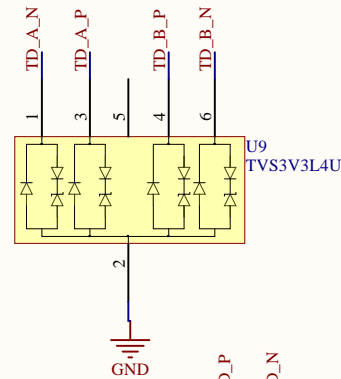
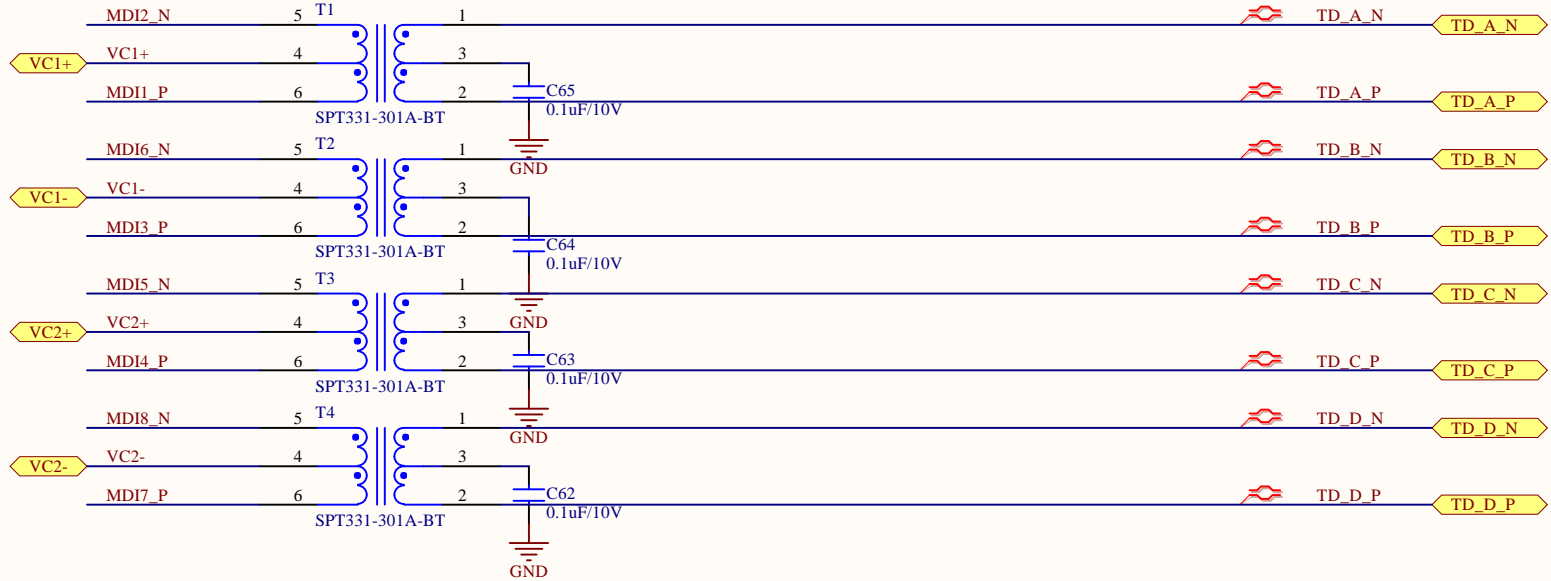
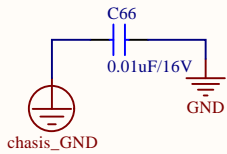
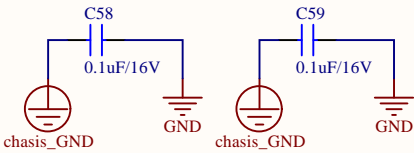
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Date:	2019/6/14	Sheet of	
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DNP_RJ45plug_100M

MDI_1/2/3/6 POE trace_20mil_0.5Oz

MDI_1/2/3/6 POE trace_10mil_1Oz



9.3.8 Mirror Mode

In some applications, the orientation of the cable connector can require Copper PMD traces to cross over each other. This complicates the board layout. The DP83869HM can resolve this issue by implementing mirroring of the ports inside the device.

In 10/100 operation, the mapping of the port mirroring is shown in Table 5.

Table 5. Mirror Port Configurations in 10/100 Operation

MDI MODE	MIRROR PORT CONFIGURATION
MDI	A → D
	B → C
MDIX	A → D
	B → C

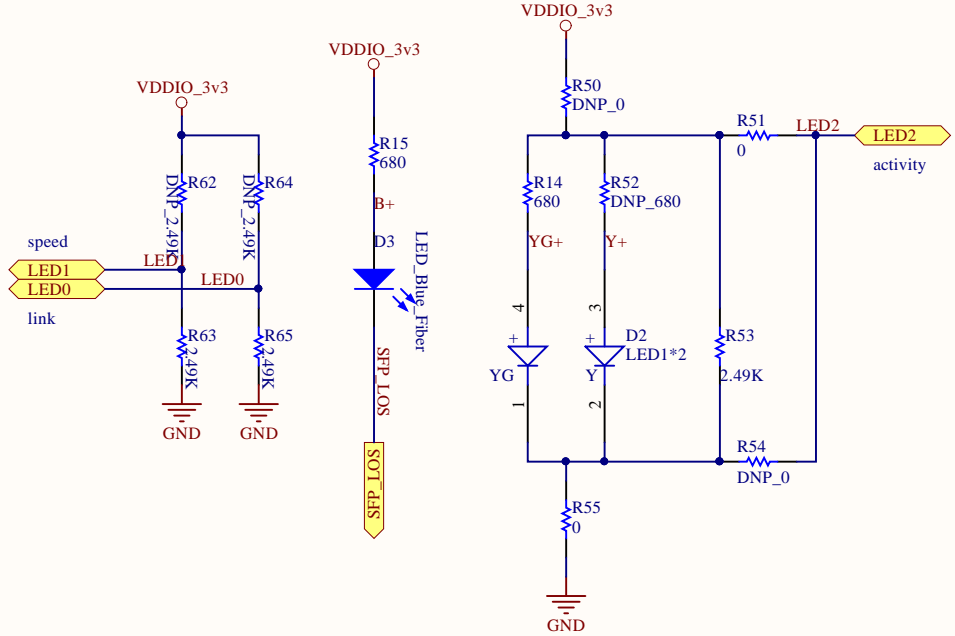
In Gigabit operation, the mapping of the port mirroring is shown in Table 6.

Table 6. Mirror Port Configurations in Gigabit Operation

MDI MODE	MIRROR PORT CONFIGURATION
MDI or MDIX	A → D
	B → C
	C → B
	D → A

Mirror mode can be enabled through strap or through register configuration using the Port Mirror Enable bit in the CFG4 register (address 0x0031). In Mirror mode, the polarity of the signals is also reversed.

Title		
Size A4	Number RJ45	Revision
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File: D:\OneDrive\...\CV4-S1-4111L-V0_RJ45_SchDocBy:		



LED2:1011b_link OK + blink on TX/RX activity

9.6.1.23 LEDS_CFG1 Register (Address = 0x18) [reset = 0x6150]

LEDS_CFG1 is shown in Figure 47 and described in Table 44.

Return to Summary Table.

Figure 47. LEDS_CFG1 Register

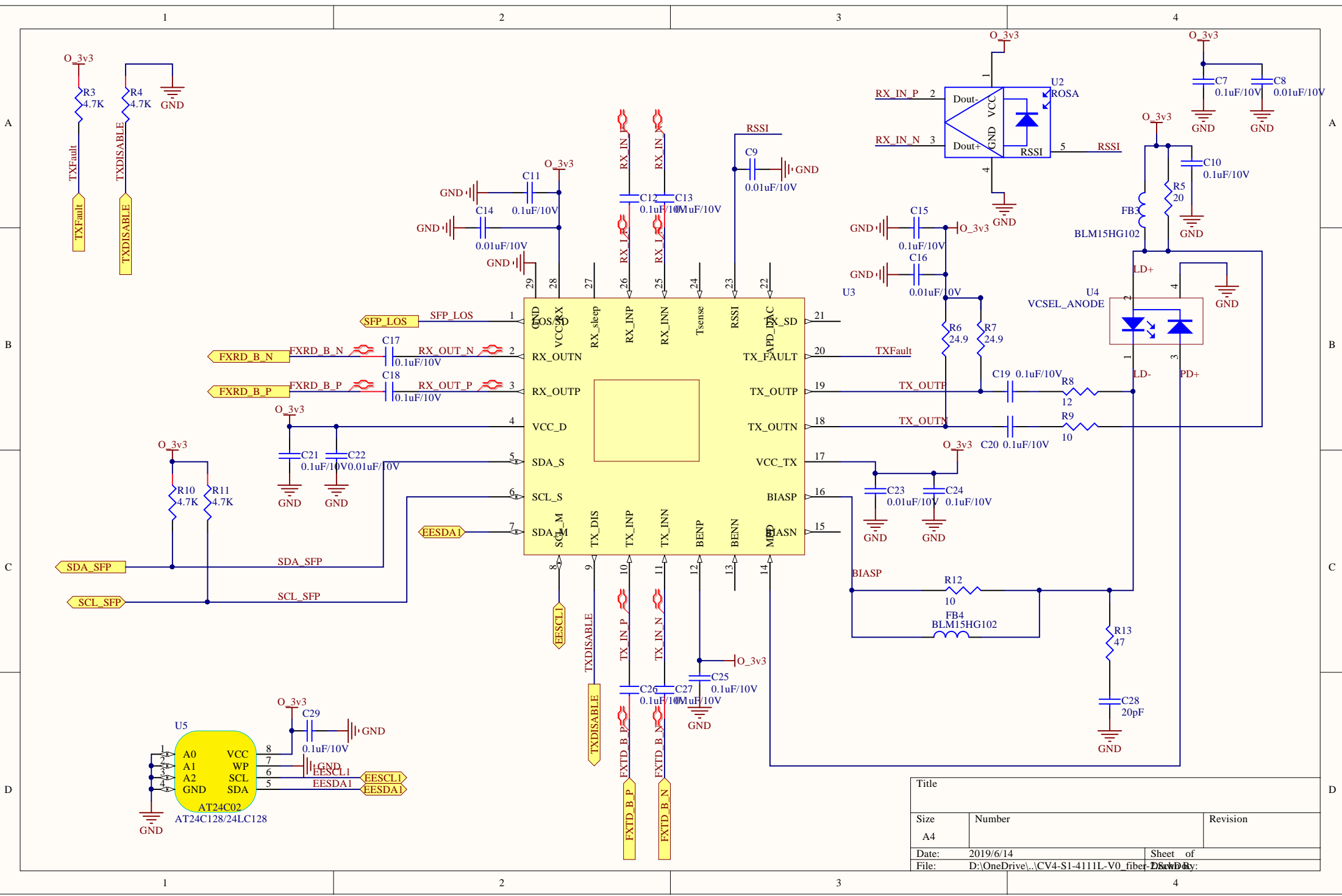
15	14	13	12	11	10	9	8
LED_GPIO_SEL				LED_ACT_SEL			
R/W-4b0110				R/W-4b0001			
7	6	5	4	3	2	1	0
LED_SPD_SEL				LED_LNK_SEL			
R/W-4b0101				R/W-4b0000			

Table 44. LEDS_CFG1 Register Field Descriptions

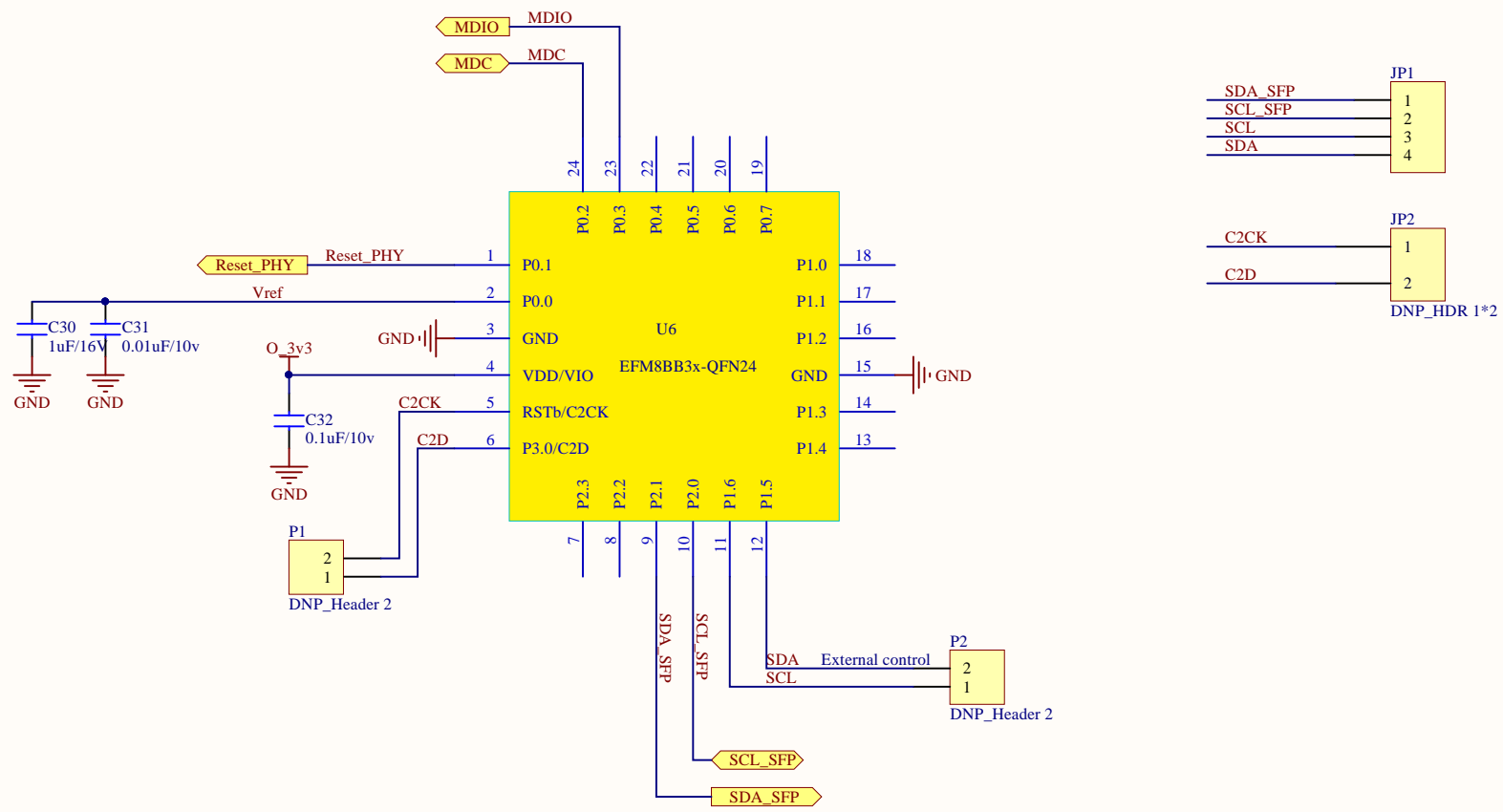
Bit	Field	Type	Reset	Description
15-12	LED_GPIO_SEL	R/W	4b0000	Source of GPIO LED, same as bits 3:0
11-8	LED_ACT_SEL	R/W	4b0000	Source of ACTIVITY LED (LED 2) , same as bits 3:0
7-4	LED_SPD_SEL	R/W	4b0000	Source of SPEED LED (LED 1) , same as bits 3:0
3-0	LED_LNK_SEL	R/W	4b0000	Source of LINK LED (LED 0) 0000b = link OK 0001b = RX/TX activity 0010b = TX activity 0011b = RX activity 0100b = collision detected 0101b = 1000BT link is up 0110b = 100 BTX link is up 0111b = 10BT link is up 1000b = 10/100BT link is up 1001b = 100/1000BT link is up 1010b = full duplex 1011b = link OK + blink on TX/RX activity 1100b = EEE mode 1101b = RX_ER or TX_ER 1110b = RX_ER

	Pin name	strap name	Pin#	Default	ANEGSEL_1	ANEGSEL_0	
					LED_2	LED_1	
100 Base-FX	LED_1	ANEGSEL_0	46	0	0	0	Copper : Auto-negotiation (100/10 Advertised), Auto MDIX
	LED_2	ANEGSEL_1	45	0	1	1	Copper : Auto Negotiation (100 Advertised), Auto MDIX
	RX_CTRL	MIRROR_EN	38	0	0	1	Copper: Mirror Disable
	RX_CLK	LINK_LOSS	32	0	0	0	Link Loss Pass Thru Enabled
					1	1	Link Loss Pass Thru Disabled
100Mbps	ITAG_TDO/GPIO_1	OPMODE_0	22	2.49K pull-up to VDDIO			
	RX_D3	OPMODE_1	36	OPEN			
	RX_D2	OPMODE_2	35	2.49K pull-up to VDDIO			
Register setting	1. Register 0x01DF will contain 0x0045 for 100 Mbps Media Converter mode. 2. Required register configuration for 100 Mbps Media Converter mode: - Write 0x1FFC to register 0x01EC (set bit [0] to 0)						
1000 Mbps media converter	LED_0	ANEG_DIS	47	0	0	0	Fiber Auto Negotiation
					1	1	Fiber Force Mode
	LED_1	ANEGSEL_0	46	0	0	0	Copper : Auto-negotiation (1000/100 Advertised), Auto MDIX
					1	1	Copper : Auto Negotiation (1000 Advertised), Auto MDIX
	1000Mbps	ITAG_TDO/GPIO_1	OPMODE_0	22	OPEN		
RX_D3		OPMODE_1	36	OPEN			
RX_D2		OPMODE_2	35	2.49K pull-up to VDDIO			
Register setting	1. Register 0x01DF will contain 0x0044 for 1000 Mbps Media Converter mode. 2. Required register configuration for 1000 Mbps Media Converter mode: - Write 0x1FFC to register 0x01EC (set bit [0] to 0)						

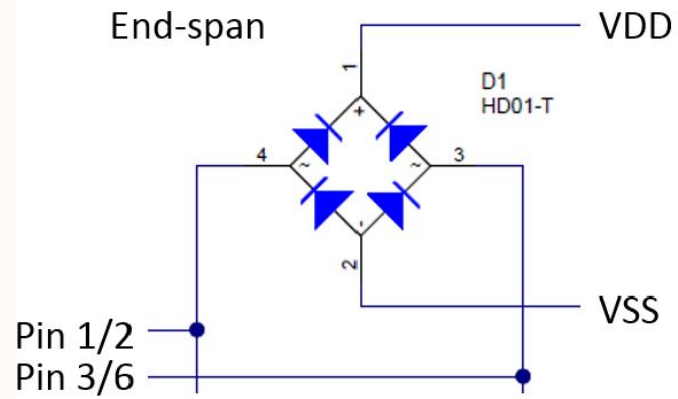
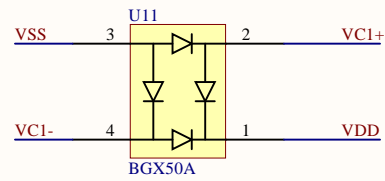
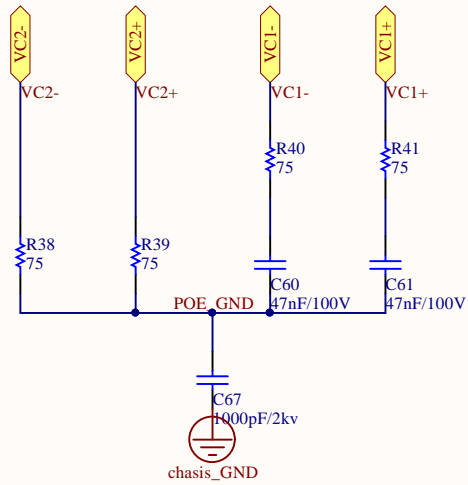
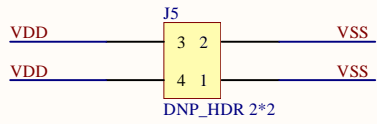
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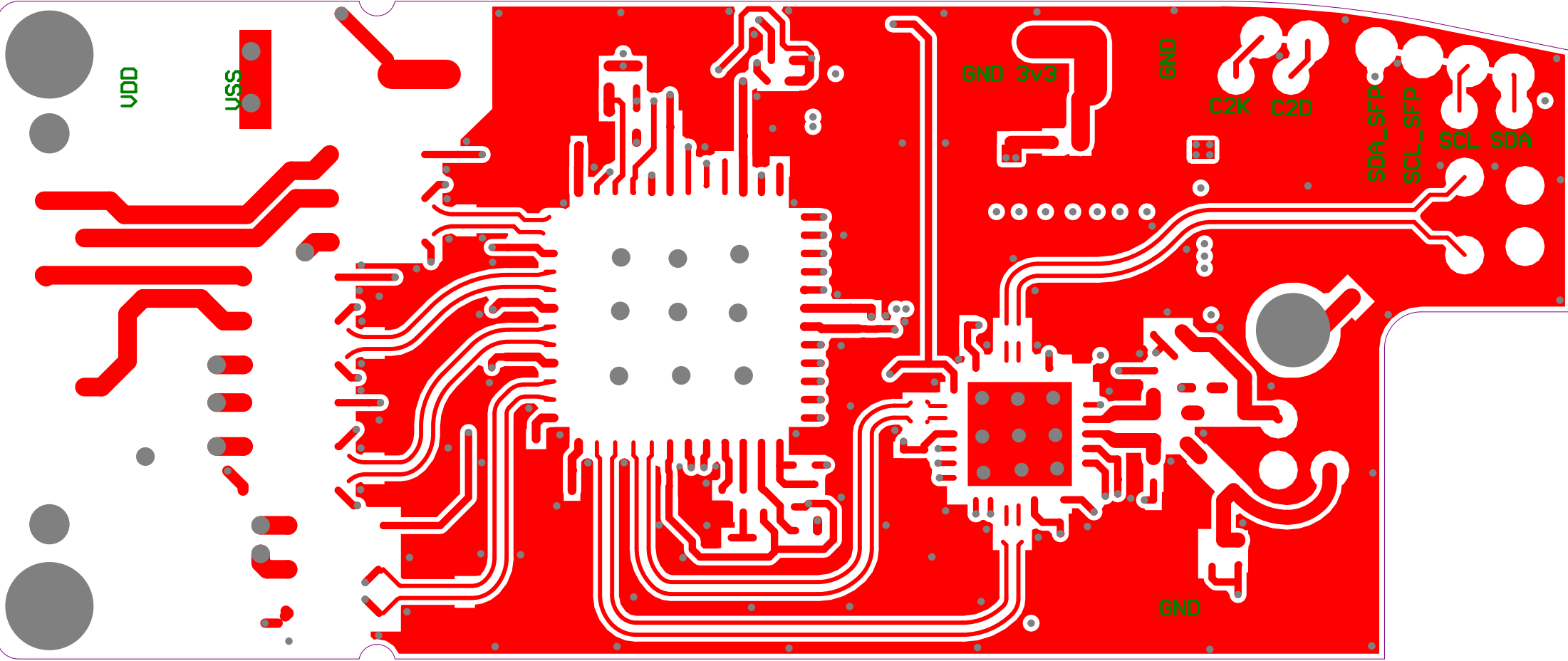
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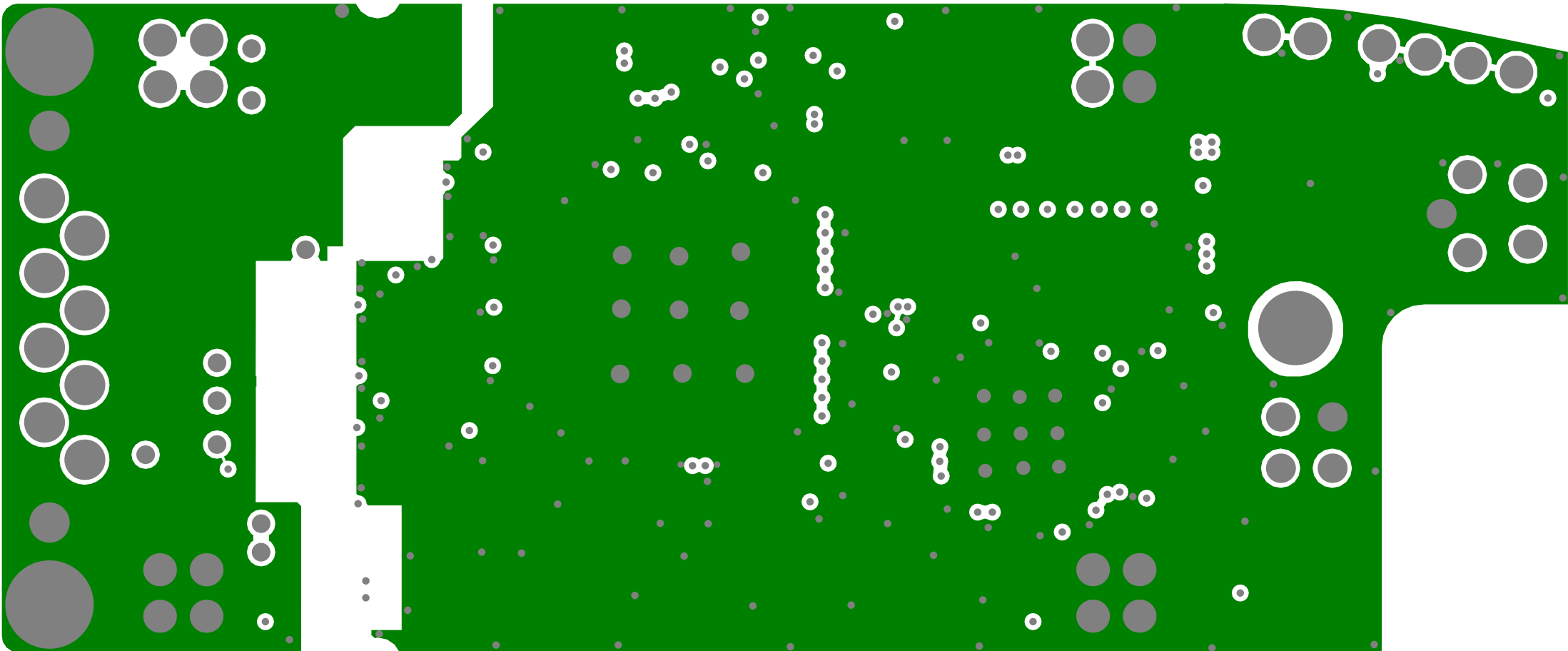


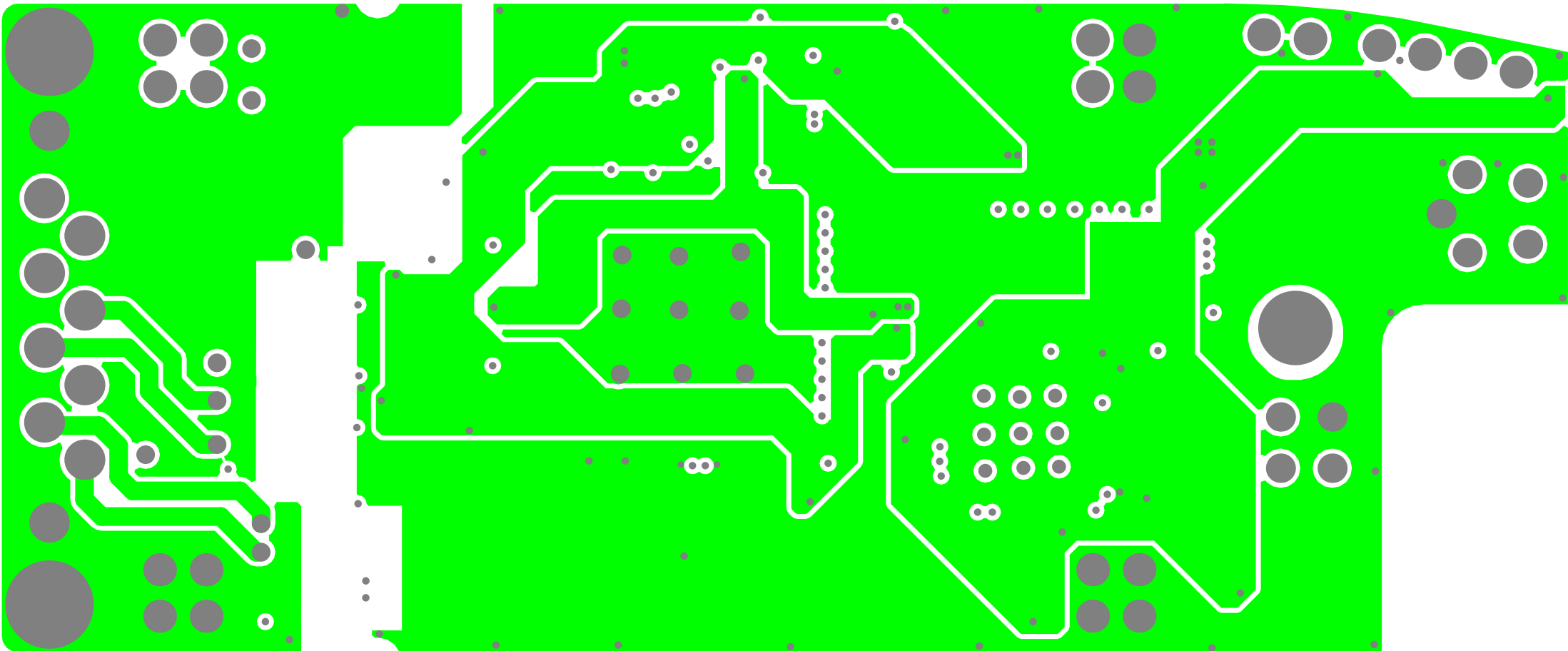
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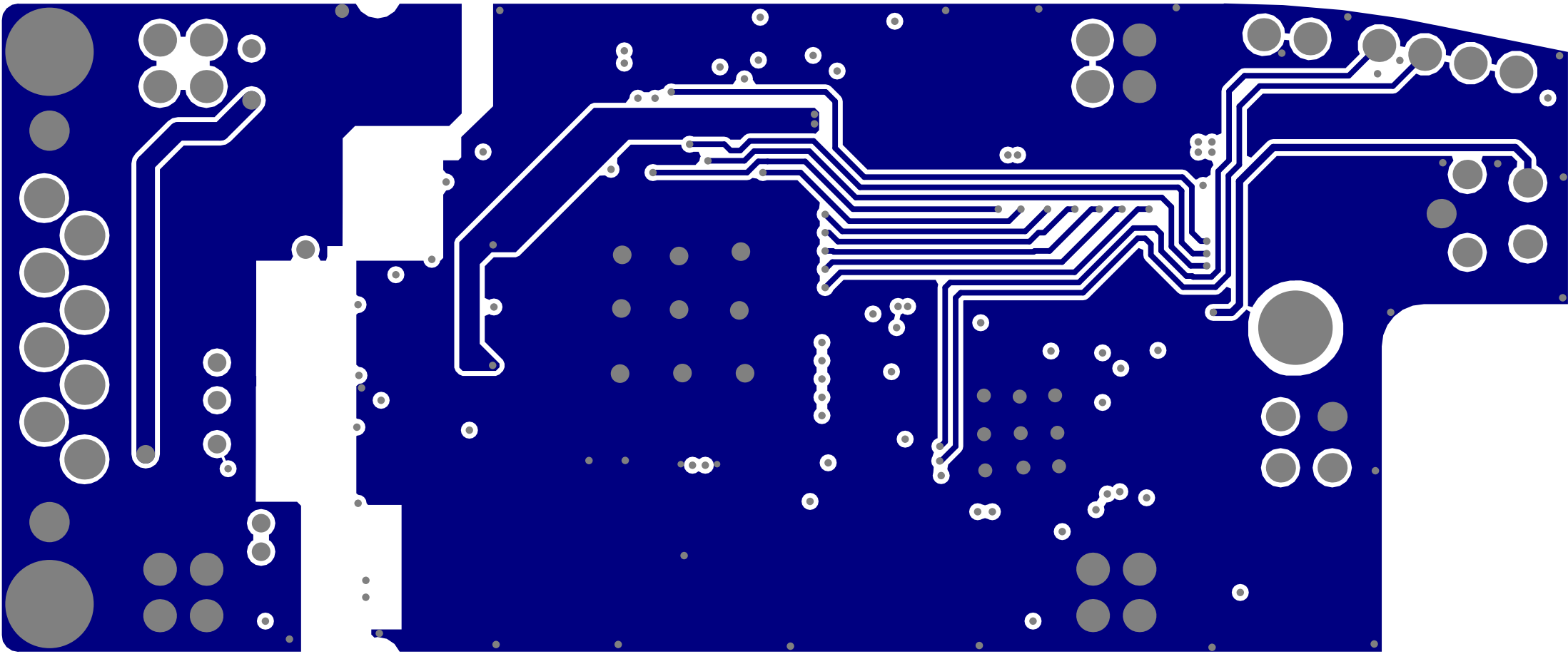


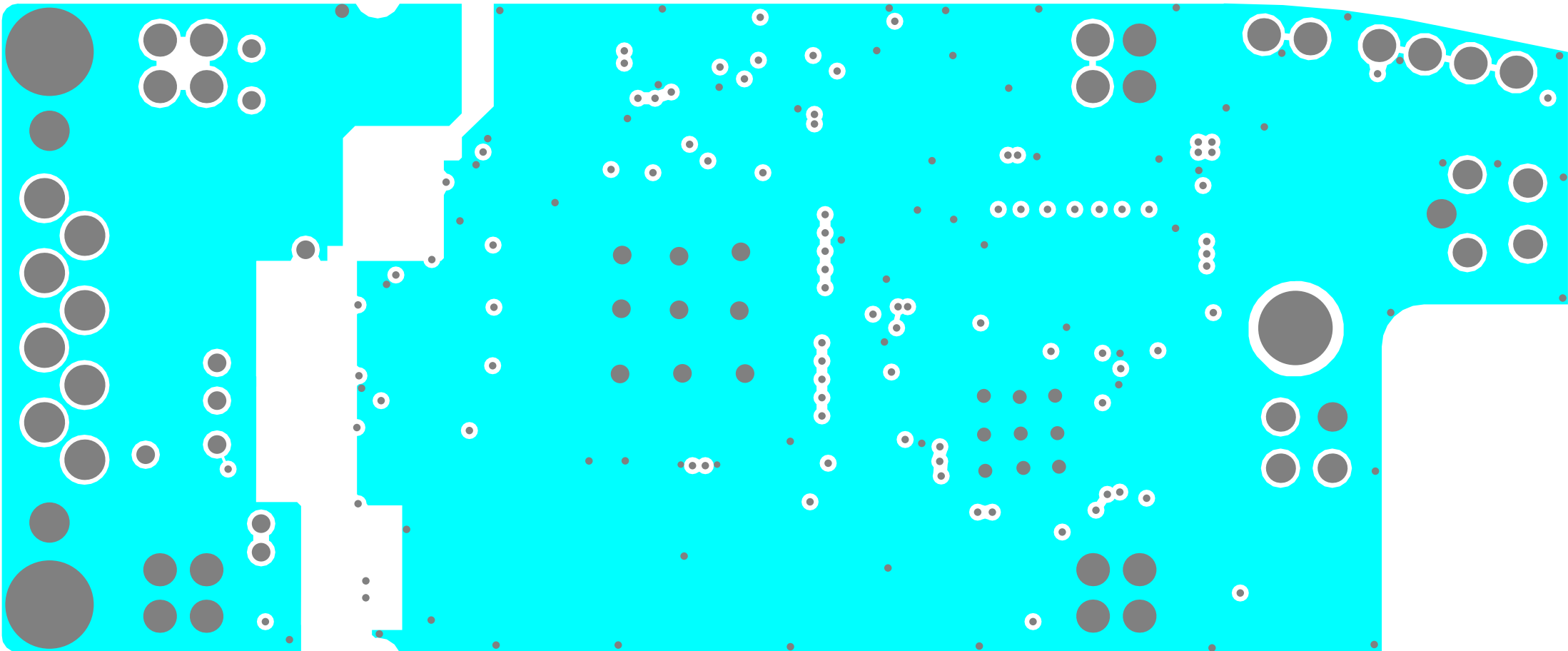
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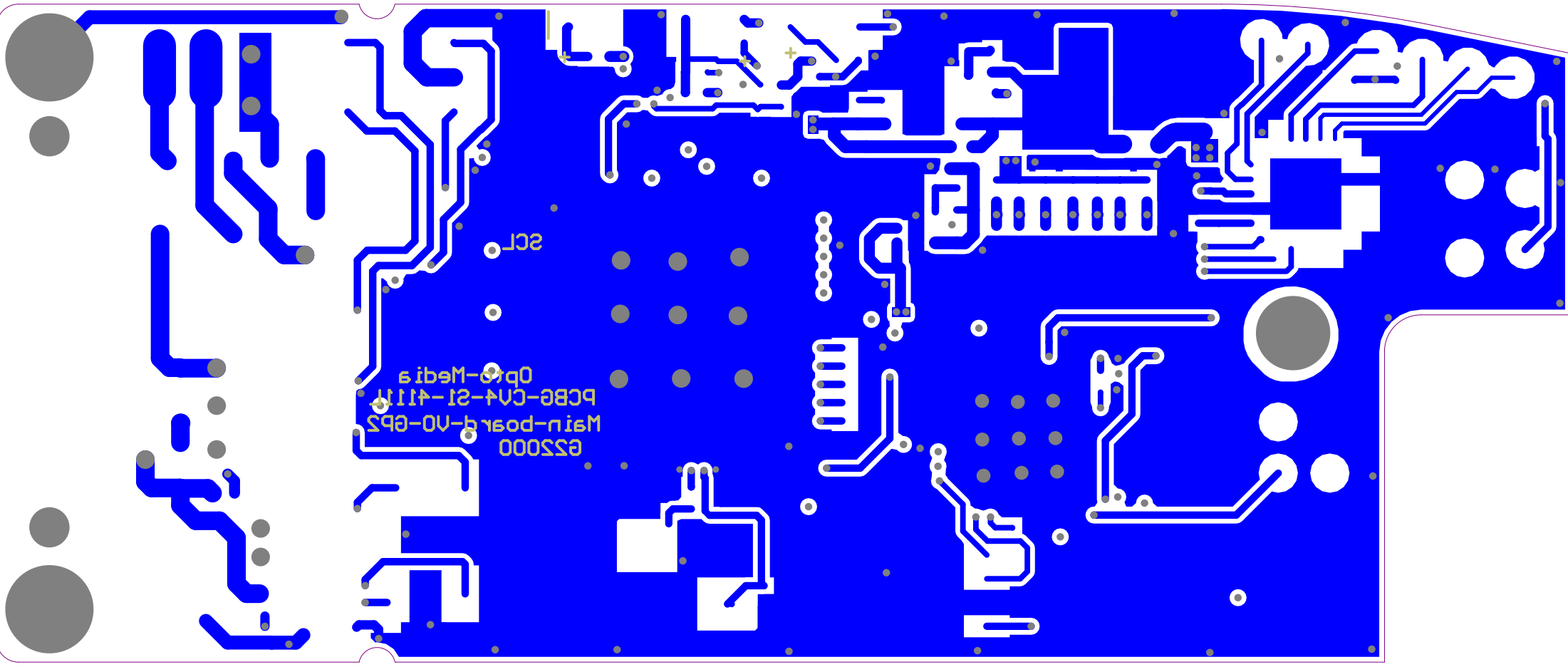












000200

Op0-Media
PCB-CV4-SI-4111
Main-board-V0-0P2
000200