

CHANNEL_STATUS_1 Register Status

Register Set		CHANNEL_STATUS_1 Register bit								
		10Gb Ethernet (optical)	15	14	13	12	11	10	9	8
Optimized	Ach	connected	0	1	0	1	1	1	0	0
		disconnected	0	1	1	1	0	0	0	0
	Bch	connected	0	1	0	1	1	1	0	1
		disconnected	0	1	0	1	1	1	0	1
Not optimized	Ach	connected	0	1	0	1	1	1	0	0
		disconnected	0	1	1	1	0	0	0	0
	Bch	connected	0	1	0	1	1	1	0	0
		disconnected	0	1	1	1	0	0	0	0

When 10Gbit Ethernet(Optical) is disconnected CHANNEL_STATUS_1 Register Bit13, Bit11, Bit10, Bit8 status value does not change.

Table 8-26. CHANNEL_STATUS_1

Device Address: 0x1E		Register Address: 0x000F	Default: 0x0000	
Bit(s)	Name	Description		Access
15	HS_TP_STATUS (XG)	Test Pattern status for High/Low/Mixed/CRPAT test patterns. Valid in 10G/1GKX modes. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10) 0 = Alignment has not been determined		RO
14	LS_ALIGN_STATUS (RXG)	Lane alignment status 1 = Lane alignment is achieved on the LS side 0 = Lane alignment is not achieved on the LS side		RO/LL
13	HS_LOS (RXG)	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs		RO/LH
12	HS_AZ_DONE (RXG)	Auto zero complete indicator. When high, indicates auto zero calibration is complete		RO/LL
11	HS_AGC_LOCKED (RXG)	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state		RO/LL
10	HS_CHANNEL_SYNC (RXG)	Channel synchronization status indicator. When high, indicates channel synchronization has achieved		RO/LL
9	RESERVED	For TI use only.		RO/LH
8	HS_DECODE_INVALID (RXG)	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)		RO/LH