

Rev	Last updated by	Date	Note
0.1	TKC	7/27/2017	First draft.
0.2	TKC	8/8/2017	Add 2G table 4
0.3	TKC	8/9/2017	update in-line connectors info
0.4	TKC	8/17/2017	preliminary
0.5	TKC	8/23/2017	correct typo on STP intrapair skew- 250 ps -> 150ps
0.6	TKC	9/21/2017	Add DS90UB933-934
0.7	TKC	10/24/2017	correct error in page 4, Table 2B, return loss
0.8	TF, LK	5/1/2018	Update S11 recommendations for coax in Table 2, 2A, 2B Change crosstalk recommendations to nominal

Operating Frequency Range - 4Gbps

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SER	DES	Clock mode	Back-channel (from DES to SER)				Forward channel (from SER to DES)			Cable reach		Comment
			Bit time (ns)	Line rate (Mbps)	f_{BCMIN} (MHz)	f_{BCMAX} (MHz)	max line rate (Mbps)	$f_{FC-NYQUIST}$ (MHz)	$f_{FC-FRAME}$ (MHz)	DACAR462 coax	DACAR535 STQ	
DS90UB953	DS90UB954	SYNC	10	50	25	50	4200	2100	105	15m	10m	Validated
DS90UB935	DS90UB936	SYNC	20	25	12.5	25	2100	1050	52.5	15m	10m	
DS90UB953	DS90UB954	EXT clock	50	10	5	10	4200	2100	105	15m	10m	
DS90UB953	DS90UB960	SYNC	10	50	25	50	4200	2100	105	15m	10m	Design target
DS90UB935	DS90UB960	SYNC	20	25	12.5	25	2100	1050	52.5	15m	10m	
DS90UB953	DS90UB960	EXT clock	50	10	5	10	4200	2100	105	15m	10m	

Table1. Frequency range of FPD-Link III DS90UB953/954 and its compatible devices (f_{BCMIN} to $f_{FC-NYQUIST}$)

How to use this Channel Requirement:

step 1: Determine the frequency range (f_{BCMIN} to $f_{FC-NYQUIST}$) from Table 1

step 2: Depends on types of testing (transmission channel, PCB, cable assembly), apply limits from the appropriate tables from f_{BCMIN} to $f_{FC-NYQUIST}$

	Testing Transmission Channel Requirement	Testing PCB Budget	Testing cable assembly Budget
Coax	Table 2	Table 2A	Table 2B
STP or STQ	Table 3	Table 3A	Table 3B

Operating Frequency Range - 2Gbps

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SER	DES	SER Clock mode	Back-channel (from DES to SER)				Forward channel (from SER to DES)			Cable reach	
			Bit time (ns)	Line rate (Mbps)	f_{BCMIN} (MHz)	f_{BCMAX} (MHz)	max line rate (Mbps)	$f_{FC-NYQUIST}$ (MHz)	$f_{FC-FRAME}$ (MHz)	DACAR462 coax	DACAR535 STQ
DS90UB953	DS90UB964	EXT clock	50	10	5	10	1870	935	46.75	15m	15m
DS90UB953	DS90UB934	EXT clock	200	2.5	1.25	2.5	1870	935	66.79	15m	15m
DS90UB933	DS90UB954	PCLK	200	2.5	1.25	2.5	1870	935	66.79	15m	15m
DS90UB913A	DS90UB954	PCLK	200	2.5	1.25	2.5	1400	700	50.00	15m	15m
DS90UB933	DS90UB934	PCLK	200	2.5	1.25	2.5	1870	935	66.79	15m	15m
DS90UB933	DS90UB960	PCLK	200	2.5	1.25	2.5	1870	935	66.79	15m	15m
DS90UB913A	DS90UB960	PCLK	200	2.5	1.25	2.5	1400	700	50.00	15m	15m

Table1. Frequency range of FPD-Link III DS90UB953/954 and its compatible devices (f_{BCMIN} to $f_{FC-NYQUIST}$)

How to use this Channel Requirement:

step 1: Determine the frequency range (f_{BC-MIN} to $f_{FC-NYQUIST}$) from Table 1

step 2: Depends on types of testing (transmission channel, PCB, cable assembly), apply limits from the appropriate tables

	Testing Transmission Channel	Testing PCB	Testing cable assembly
Coax	Table 2	Table 2A	Table 2B
STP or STQ	Table 4	Table 4A	Table 4B

			Table 2A - Recommendations			Table 2 - Requirements			Table 2B - Recommendations			
			PCB Budget (with PoC)			Total Channel Requirement			Coax cable assembly - Budget			
Parameter	C _{AC}	Frequency	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Return loss, S ₁₁		f=1 - 100 MHz			-20			-16			-20	dB
		f=0.1 to 1 GHz			-12 + 8*log(f)			-9 + 7*log(f)			-12 + 8*log(f)	dB
		f=1 - 2.1 GHz			-12			-9			-12	dB
Insertion Loss, S ₂₁		f=1MHz		>-0.35		-1.4				>-0.7		
		f=5MHz		>-0.35		-2.3				>-1.6		
		f=10MHz		>-0.35		-2.5				>-1.8		dB
		f=50MHz		>-0.35		-3.5				>-2.5		dB
		f=100MHz		>-0.35		-4.5				>-3.9		dB
		f=500 MHz		>-0.35		-9.5				>-8.7		dB
		f=1.0 GHz		>-0.6		-14				>-12.8		dB
		f=2.1 GHz		>-1.2		-21.6				>-19.2		dB
Far end crosstalk							-30			-30		dB
Near end crosstalk							-30			-30		dB
Impedance	PCB trace		45	50	55							Ω
	landing pad and component		40	50	60							Ω
	cable					45	50	55	45	50	55	Ω
	connector region					40	50	62.5	40	50	62.5	Ω
In-line connectors	< 4m						≤ 1			≤ 1		
	4-6m						≤ 2			≤ 2		
	6-15m						≤ 4			≤ 4		
Cable reach	test with DACAR462						15			15		m

Note 2: Below Nyquist frequency, the transmission channel should be free of resonance that creates sharp drops in insertion loss and abrupt changes in the channel's group delay. The maximum insertion loss of the channel is dependent on the drive capability of the SER, and the analog front end's capability of the DES.

Note 3: The total transmission channel from SER to DES is the combined contribution from the SER-board, cable assembly and the DES-board. The PCB insertion loss budget in this table assumes the use of 2-inch FR4 board trace and the associated circuit components. Higher insertion loss for the PCB is possible but with the trade-off in lower insertion loss for the cable assembly. Likewise, shorter board traces reduces PCB insertion loss, and correspondingly allow higher cable insertion loss.

Note 3. Impedance is measured with TDR launch at an edge rate equals to the nominal edge rate of SER output.

PoC Network Requirements

4Gbps PoC Network: SYNC clock mode	MIN	NOM	MAX	UNIT
Frequency range	25		2100	MHz
Total DC resistance		<1.75		Ω
Inductance ⁽¹⁾		10		μH
PoC interference pulse due to dc current change				
30/60 Hz at V_{POC} (switcher input)			500	mVpp
pulse slew rate	200			$\mu\text{s/V}$
PoC interference from switching noise				
0.5 - 50MHz sinusoidal			TBD	mVpp

Note 1. A PoC network is built with several inductors in series to form a wide band inductor. Consult TI datasheet or other literature for recommendations.

2Gbps PoC Network: EXT PCLK	MIN	NOM	MAX	UNIT
Frequency range	1.25		1000	MHz
Total DC resistance		<1.75		Ω
Inductance ⁽¹⁾		110		μH
PoC interference pulse due to dc current change				
30/60 Hz at V_{POC} (switcher input)			500	mVpp
pulse slew rate	200			V/ μs
PoC interference from switching noise				
0.5 - 50MHz sinusoidal			TBD	mVpp

Note 1. A PoC inductor is built with several inductors in series to form a wide band inductor. Consult TI datasheet or other literature for recommendations.

Table 3A - Recommendations

PCB Budget

Parameter	C _{AC}	Frequency	MIN	NOM	MAX
Return loss, SDD11		f=1 - 5MHz			-25
		f=10-100MHz			-25
		f=0.1-1 GHz			-26.4 + 14.4f
		f=1 - 2.5 GHz			-12
Insertion Loss, SDD21		f=1MHz		>-0.3	
		f=5MHz		>-0.3	
		f=10MHz		>-0.3	
		f=50MHz		>-0.3	
		f=100MHz		>-0.3	
		f=500 MHz		>-0.3	
		f=1.0 GHz		>-0.5	
		f=2.1 GHz		>-0.8	
Insertion loss to far end crosstalk ratio		f<2.1 GHz			
Near end crosstalk		f<200MHz			
Impedance	PCB trace		90	100	110
	landing pad and component		80	100	120
	cable				
	connector region				
Intra-pair skew		100-300 MHz			
		300-500 MHz			
		500 - 1.5 GHz			
		1.5 - 2.1 GHz			
in-line connectors		<6m			
		6-10m			
Cable reach	test with DACAR535-2				

Table 3 - Requirements

Transmission Channel Requirement

Frequency	MIN	NOM	MAX
f=1-5MHz			-20
f=10-100MHz			-20+20f
f=0.1 - 0.5 GHz			-20+20f
f=0.5 - 2.5 GHz			-10
f=1MHz	-1.1		
f=5MHz	-1.4		
f=10MHz	-1.6		
f=50MHz	-2.7		
f=100MHz	-3.4		
f=500 MHz	-7.8		
f=1.0 GHz	-12		
f=2.1 GHz	-19.6		
	20		
			-30
	85	100	115
	80	100	125
			250
			150
			100
			40
		0	
		≤2	
		10	

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Table 3B - Recommendations

Cable assembly- Budget

MIN	NOM	MAX	UNIT
		-20	dB
		-20+20f	dB
		-20+20f	dB
		-10	dB
	>-0.5		
	>-0.8		
	>-1.0		dB
	>-2.1		dB
	>-2.8		dB
	>-7.2		dB
	>-11		dB
	>-18		dB
20			dB
		-30	dB
			Ω
			Ω
85	100	115	Ω
80	100	125	Ω
		250	ps
		150	ps
		100	ps
		40	ps
	0		
	≤2		
	10		m

Note 1: The transmission channel after aging and mechanical stress testing should meet the Transmission Channel Requirement.

Note 2: Below Nyquist frequency, the transmission channel should be free of resonance that creates sharp drops in insertion loss and abrupt changes in the channel's group delay. The maximum insertion loss of the channel is dependent on the drive capability of the SER, and the analog front end's capability of the DES.

Note 3: The total transmission channel from SER to DES is the combined contribution from the SER-board, cable assembly and the DES-board. The PCB insertion loss budget in this table assumes the use of 2-inch FR4 board trace and the associated circuit components. Higher insertion loss for the PCB is possible but with the trade-off in lower insertion loss for the cable assembly. Likewise, shorter board traces reduces PCB insertion loss, and correspondingly allow higher cable insertion loss.

Table 4A - Recommendations

PCB Budget

Parameter	C _{AC}	Frequency	MIN	NOM	MAX
Return loss, SDD11		f=1 - 5MHz			-25
		f=10-100MHz			-25
		f=0.1-1 GHz			-26.4 + 14.4f
		f=1 - 2.5 GHz			-12
Insertion Loss, SDD21		f=1MHz		>-0.3	
		f=5MHz		>-0.3	
		f=10MHz		>-0.3	
		f=50MHz		>-0.3	
		f=100MHz		>-0.3	
		f=500 MHz		>-0.3	
		f=1.0 GHz		>-0.5	
Insertion loss to far end crosstalk ratio		f<1.0 GHz			
Near end crosstalk		f<200MHz			
Impedance	PCB trace		90	100	110
	landing pad and component		80	100	120
	cable				
	connector region				
Intra-pair skew		100-300 MHz			
		300-500 MHz			
		500 - 1.5 GHz			
in-line connectors		<6m			
		6-15m			
Cable reach	test with DACAR535-2				

Table 4 - Requirements

Transmission Channel Requirement

Frequency	MIN	NOM	MAX
f=1-5MHz			-20
f=10-100MHz			-20+20f
f=0.1 - 0.5 GHz			-20+20f
f=0.5 - 2.5 GHz			-10
f=1MHz	-1.35		
f=5MHz	-1.8		
f=10MHz	-2.1		
f=50MHz	-3.8		
f=100MHz	-4.9		
f=500 MHz	-11.3		
f=1.0 GHz	-17.3		
	20		
			-30
	85	100	115
	80	100	125
			250
			150
			100
		0	
		≤2	
		15	

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Table 4B - Recommendations

Cable assembly- Budget

MIN	NOM	MAX	UNIT
		-20	dB
		-20+20f	dB
		-20+20f	dB
		-10	dB
	>-0.75		dB
	>-1.2		dB
	>-1.5		dB
	>-3.2		dB
	>-4.3		dB
	>-10.7		dB
	>-16.3		dB
			dB
20			dB
		-30	dB
			Ω
			Ω
85	100	115	Ω
80	100	125	Ω
		250	ps
		150	ps
		100	ps
	0		
	≤2		
	15		m

Note 1: The transmission channel after aging and mechanical stress testing should meet the Transmission Channel Requirement.

Note 2: Below Nyquist frequency, the transmission channel should be free of resonance that creates sharp drops in insertion loss and abrupt changes in the channel's group delay. The maximum insertion loss of the channel is dependent on the drive capability of the SER, and the analog front end's capability of the DES.

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