

Test Report

Fail

Test Configuration Details	
Application	
Name	D9020DPHC MIPI D-PHY Test
Version	3.73.1.0
Device Description	
Fixture Setup	Auto Load Switching
High Speed Data Rate(Mbps)	800
CTS Version	v1.0
ZID	100 ohm
CLoad	50pF
Test Session Details	
Infiniium SW Version	06.55.00401
Infiniium Model Number	MS0S804A
Infiniium Serial Number	MY59290107
Debug Mode Used	No
Compliance Limits	MIPI D-PHY Test Limit v1.0 (official)
Probe (Channel 1)	Model: 1169A Serial: US44001644 Head: N5381A/B Atten: Not Calibrated, Using Default Atten (3.1496E+00) Skew: Not Calibrated, Using Default Skew
Probe (Channel 2)	Model: 1169A Serial: US44005715 Head: N5381A/B Atten: Not Calibrated, Using Default Atten (3.2041E+00) Skew: Not Calibrated, Using Default Skew
Probe (Channel 3)	Model: 1169A Serial: US44006114 Head: N5381A/B Atten: Not Calibrated, Using Default Atten (3.2331E+00) Skew: Not Calibrated, Using Default Skew
Probe (Channel 4)	Model: 1169A Serial: US44006104 Head: N5381A/B Atten: Not Calibrated, Using Default Atten (3.1348E+00) Skew: Not Calibrated, Using Default Skew
Last Test Date	2021-11-02 20:21:40 UTC +08:00

Summary of Results

Test Statistics		Margin Thresholds	
Failed	6	Warning	< 5 %
Passed	25	Critical	< 0 %
Total	31		

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	220.84 mV	29.2	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	3.51 mV	29.8	0.00000 V <= VALUE <= 5.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	4.12 mV	72.5	VALUE < 15.00 mV

✗	1	1	1.3.9 HS Data TX Common- Level Variati Between 50- 450MHz (VCMTX(	43.62 mV	-74.5	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-143.78 mV	2.9	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differe Voltage Pulse)	174.39 mV	26.5	140.00 mV <= VALUE <= 270.00 mV
✗	1	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	30.61 mV	-206.1	VALUE <= 10.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage Pulse)	302.95 mV	15.8	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (UIInst)(Max)	1.602 ns	87.2	VALUE < 12.500 ns
✗	1	1	1.3.11 HS Data TX 20%- 80% Rise Time (tR)	99.900000000000 E36s	-303E+47	DataRiseTime_LimitMin s < VALUE < DataRiseTime_LimitMax s
✓	0	1	1.3.12 HS Data TX 80%- 20% Fall Time (tF)	461 ps	5.8	DataFallTime_LimitMin s < VALUE < DataFallTime_LimitMax s
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage	207.14 mV	42.9	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.8 HS Clock TX Vcmtx Mismatch	2.18 mV	43.6	0.00000 V <= VALUE <= 5.00 mV

✓	0	1	1.4.10 HS Clock TX Common- Level Variati Above 450MHz (VCMTX(	2.59 mV	82.7	VALUE < 15.00 mV
✗	1	1	1.4.9 HS Clock TX Common- Level Variations Between 50- 450MHz (VCMTX(LF))	32.19 mV	-28.8	VALUE < 25.00 mV
✓	0	1	1.4.4 HS Clock TX Differe Voltage Pulse)	-163.10 mV	17.8	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	180.77 mV	31.4	140.00 mV <= VALUE <= 270.00 mV
✗	1	1	1.4.5 HS Clock TX Differe Voltage Mismatch (Pulse)	17.67 mV	-76.7	VALUE <= 10.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	289.97 mV	19.5	VALUE <= 360.00 mV
✓	0	1	1.4.11 HS Clock TX 20%- 80% Rise Time (tR)	233 ps	25.2	CLKRiseTime_LimitMin s < VALUE < CLKRiseTime_LimitMax s
✓	0	1	1.4.12 HS Clock TX 80%- 20% Fall Time (tF)	224 ps	22.4	CLKFallTime_LimitMin s < VALUE < CLKFallTime_LimitMax s
✓	0	1	1.4.17 HS Clock Instant (UIinst	1.597 ns	160E+01	VALUE >= UIinst_Min_Limit s
✓	0	1	1.3.1 HS Entry: DATA ILPX	127.42 ns	154.8	VALUE >= 50.00 ns

✓	0	1	1.3.2 HS Entry: DATA TX THS- PREPARE	66.94 ns	42.6	THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s
✓	0	1	1.3.3 HS Entry: DATA TX THS- PREPARE+THS- ZERO	561.41 ns	248.7	VALUE >= TXTHSPrepareTHSZero_LimitMin s
✓	0	1	1.3.13 HS Exit: DATA TX THS- TRAIL	92.74 ns	42.7	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TEOT	7.13 ns	79.6	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	99.86 ns	19.6	VALUE <= TXTEOT_LimitMax s
✓	0	1	1.3.16 HS Exit: DATA TX THS- EXIT	960.00 ns	860.0	VALUE >= 100.00 ns
✗	1	1	1.5.4 Data- to- Clock Skew (TSKEW(TX))	-192 mUIinst	-14.0	MinMaxTSkewTest_LimitMin UIinst <= VALUE <= MinMaxTSkewTest_LimitMax UIinst
✓	0	1	1.5.4 Data- to- Clock Skew (TSKEW(TX))(Mean)	-144 mUIinst	2.0	MeanTSkewTest_LimitMin UIinst <= VALUE <= MeanTSkewTest_LimitMax UIinst

Report Detail

1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)

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D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.3.7)

HS transmit static common-mode voltage.

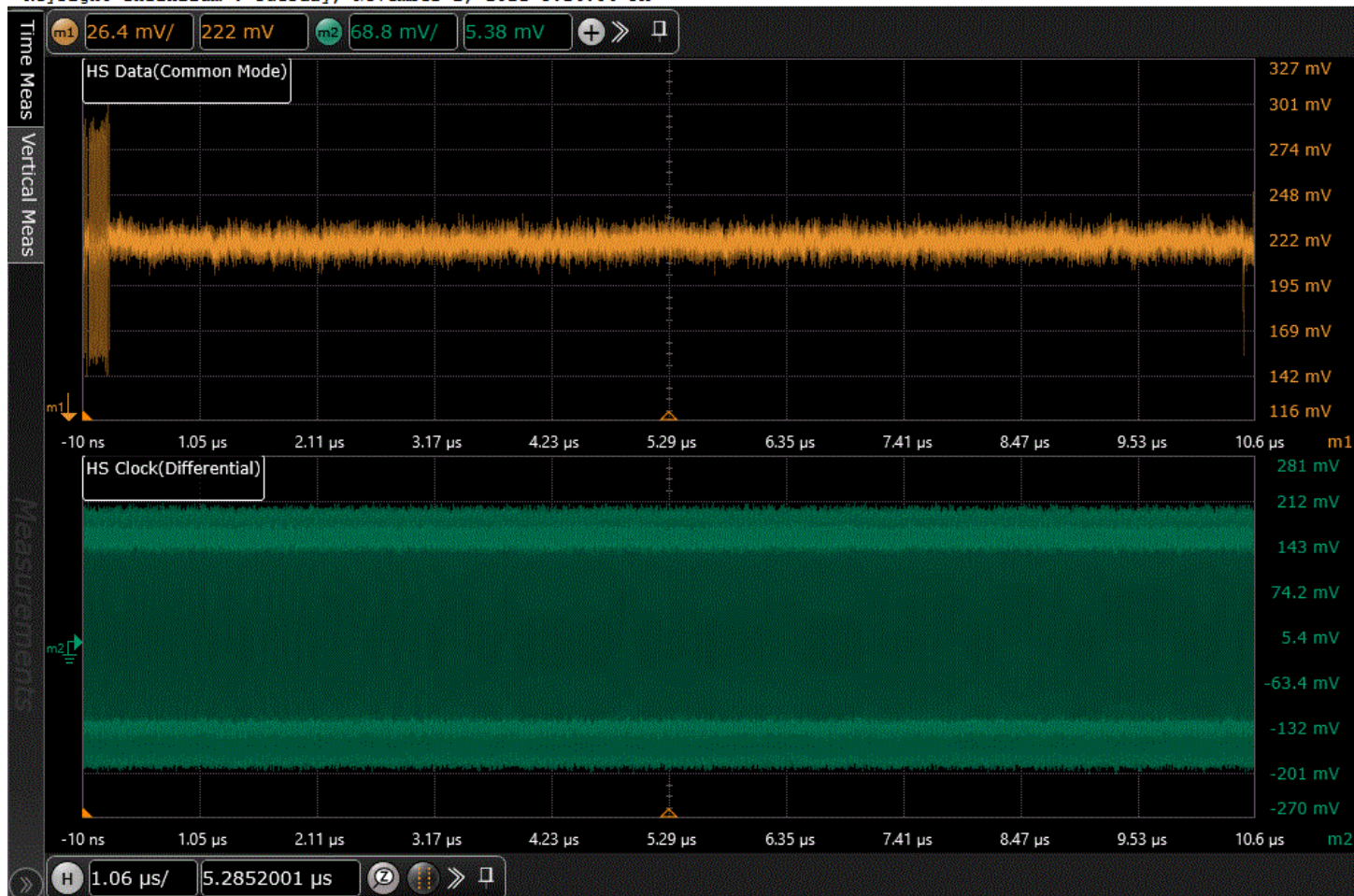
Actual Value Measurement Name: 811_Vcmtx(Worst)

Pass Limits: 150.00 mV <= VALUE <= 250.00 mV

Actual Value	Margin	HS Data TX Common Mode Voltage	Vcmtx(Differential-1)	Number of Vcmtx(Differential-1) Measured
220.84 mV	29.2	(See image)	213.83 mV	124.000

Vcmtx(Differential-0)	Number of Vcmtx(Differential-0) Measured	ZID	DataLane	Number of HS Burst
220.84 mV	6.483000 k	100 ohm	Lane0	1

HS Data TX Common Mode Voltage


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1.3.8 HS Data TX Vcmtx Mismatch

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.3.8)

VCMTX mismatch when output is Differential-1 or Differential-0.

Actual Value Measurement Name: 812_Vcmtx Mismatch

Pass Limits: 0.00000 V <= VALUE <= 5.00 mV

Actual Value	Margin	Vcmtx(Differential-1)	Vcmtx(Differential-0)	ZID	DataLane	Number of HS Burst
3.51 mV	29.8	213.83 mV	220.84 mV	100 ohm	Lane0	1

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1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))

D-PHY Specification v1.0 Section 8.1.1 Table 17, CTS v1.0(Test 1.3.10)

Common-level variations above 450MHz.

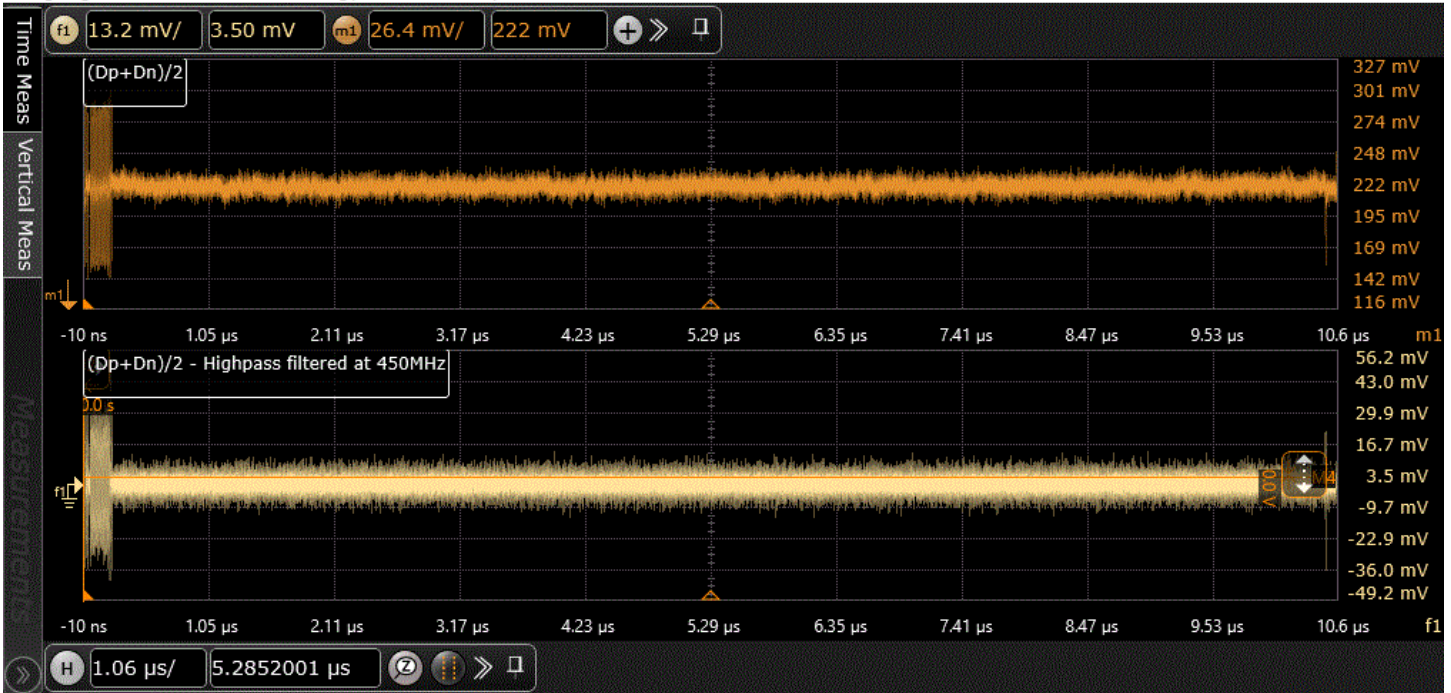
Actual Value Measurement Name: 818_Vcmtx(HF)

Pass Limits: VALUE < 15.00 mV

Actual Value	Margin	Common Level Variations(>450Mhz)	ZID	DataLane	Number of HS Burst
4.12 mV	72.5	(See image)	100 ohm	Lane0	1

Common Level Variations(>450Mhz)

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1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))

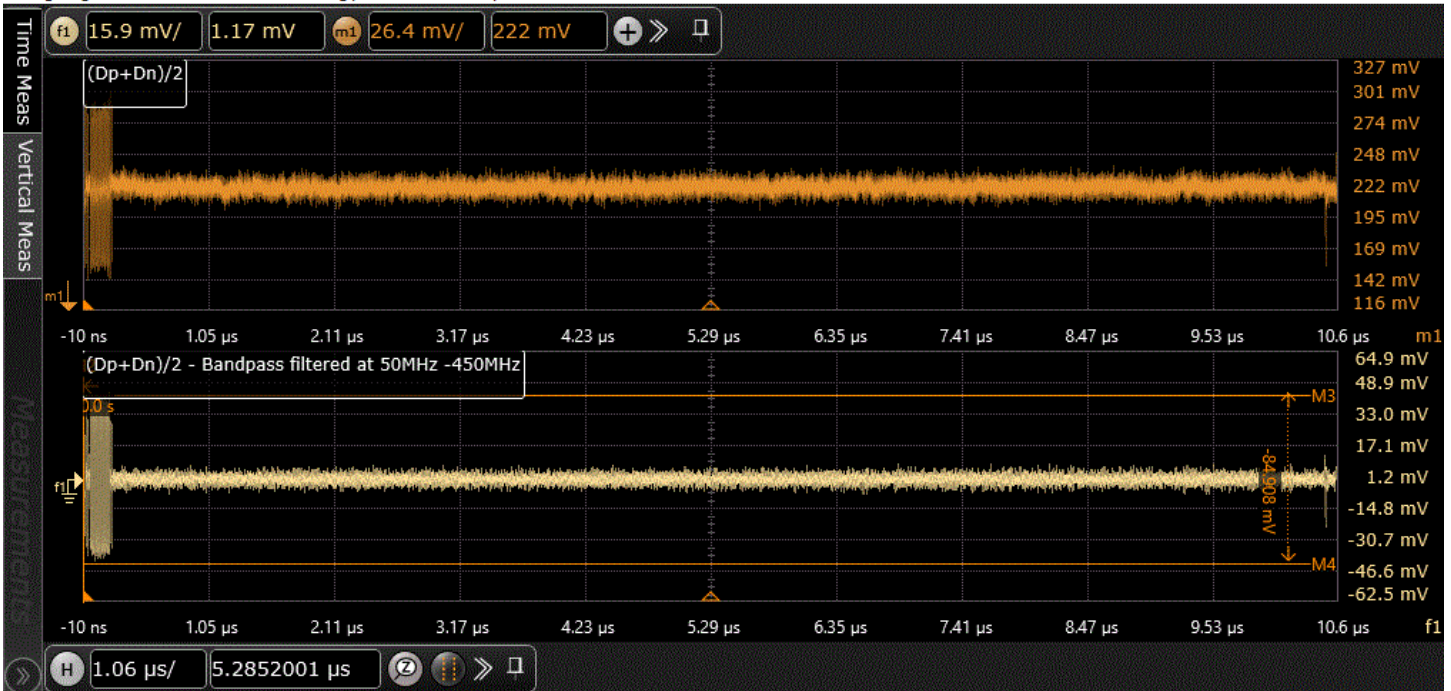
D-PHY Specification v1.0 Section 8.1.1 Table 17, CTS v1.0(Test 1.3.9)

Common-level variation between 50-450MHz.
Actual Value Measurement Name: 819_Vcmtx(LF)
Pass Limits: VALUE < 25.00 mV

Actual Value	Margin	Common Level Variations(50-450MHz)	ZID	DataLane	Number of HS Burst
43.62 mV	-74.5	(See image)	100 ohm	Lane0	1

Common Level Variations(50-450MHz)

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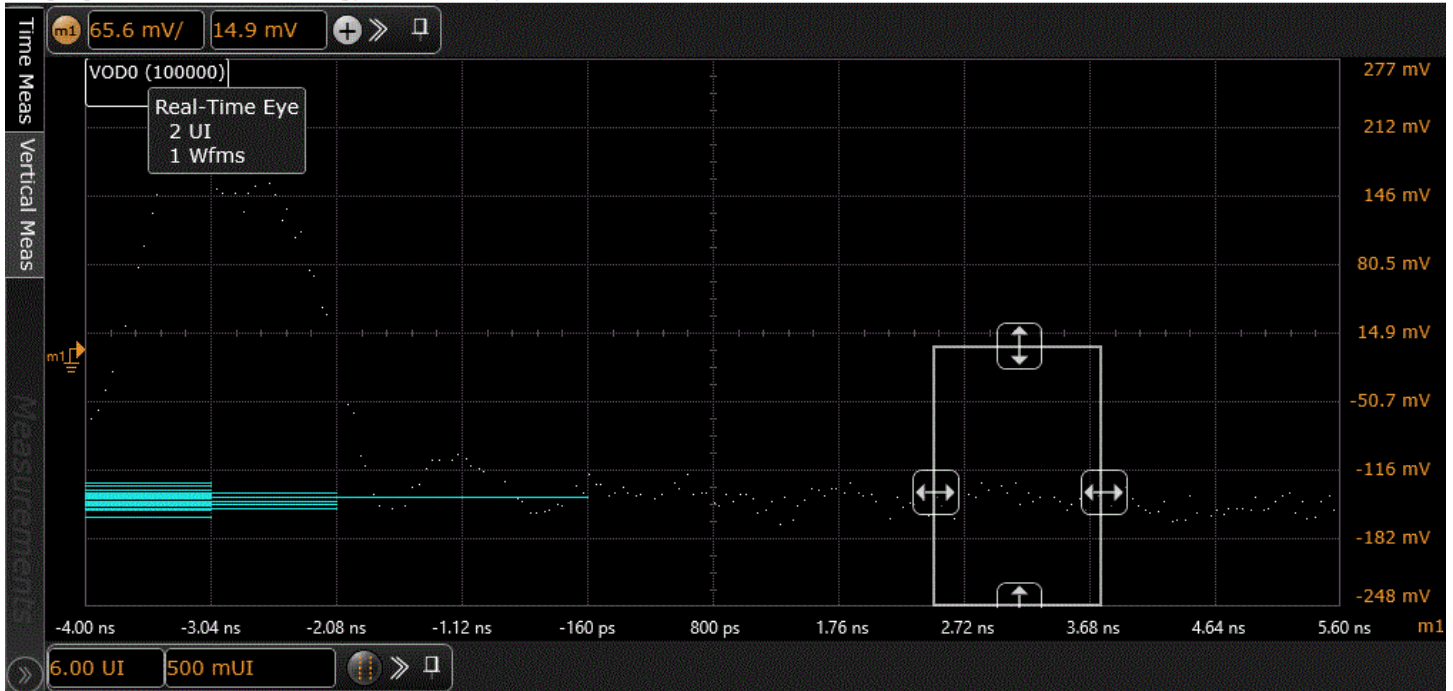
1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.3.4)

HS transmit differential voltage.
This test will measure the VOD0 based on the reference data patterns(100000) of differential signal.
Actual Value Measurement Name: 8131_Vod0(Mean)
Pass Limits: -270.00 mV <= VALUE <= -140.00 mV

Actual Value	Margin	VOD0 (100000)	Vod(Differential-0)	Number of measurement	ZID	DataLane	Number of HS Burst
-143.78 mV	2.9	(See image)	-143.78 mV	2.000	100 ohm	Lane0	1

VOD0 (100000)


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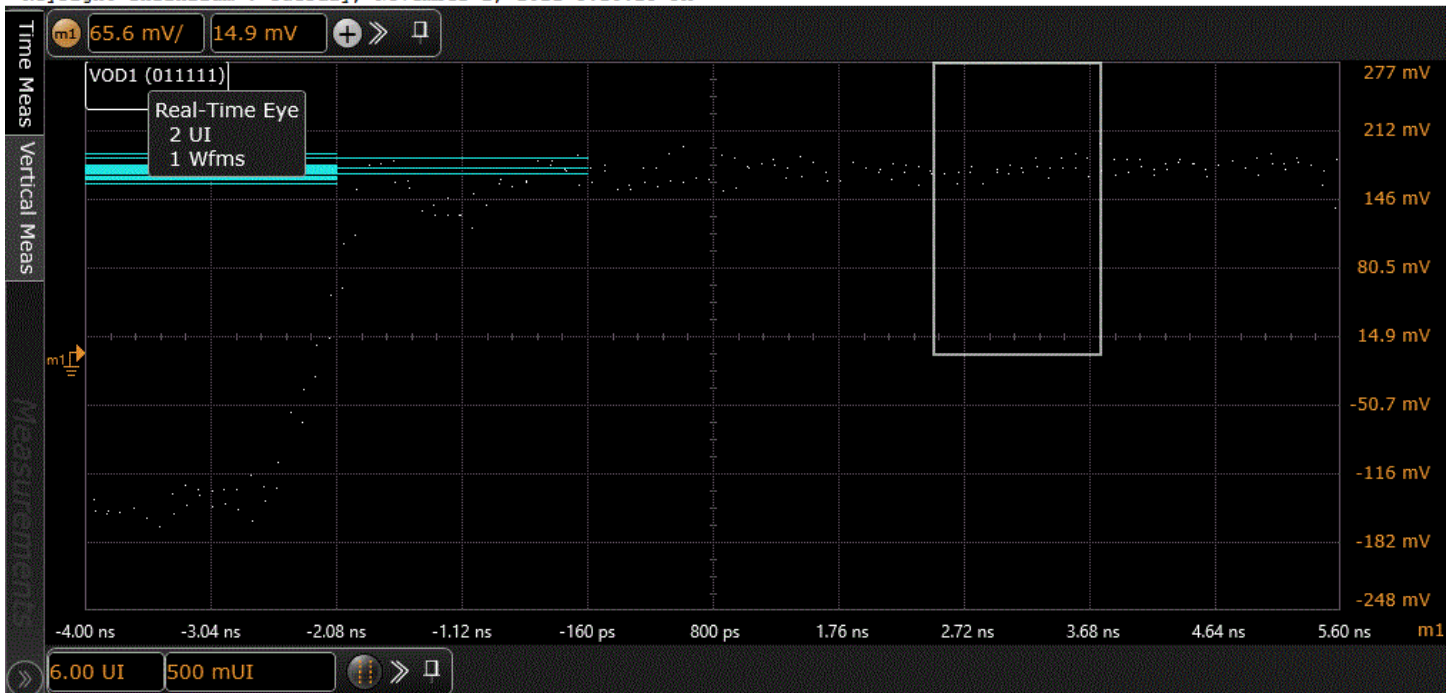

1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.3.4)

HS transmit differential voltage.
 This test will measure the VOD1 based on the reference data patterns(011111) of differential signal.
 Actual Value Measurement Name: 8132_Vod1(Mean)
 Pass Limits: 140.00 mV <= VALUE <= 270.00 mV

Actual Value	Margin	VOD1 (011111)	Vod(Differential-1)	Number of measurement	ZID	DataLane	Number of HS Burst
174.39 mV	26.5	(See image)	174.39 mV	2.000	100 ohm	Lane0	1

VOD1 (011111)


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1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.3.5)

VOD mismatch when output is Differential-1 or Differential-0.
 Actual Value Measurement Name: 8141_Vod Mismatch
 Pass Limits: VALUE <= 10.00 mV

Actual Value	Margin	Vod(Differential-1)	Vod(Differential-0)	ZID	DataLane	Number of HS Burst
30.61 mV	-206.1	174.39 mV	-143.78 mV	100 ohm	Lane0	1

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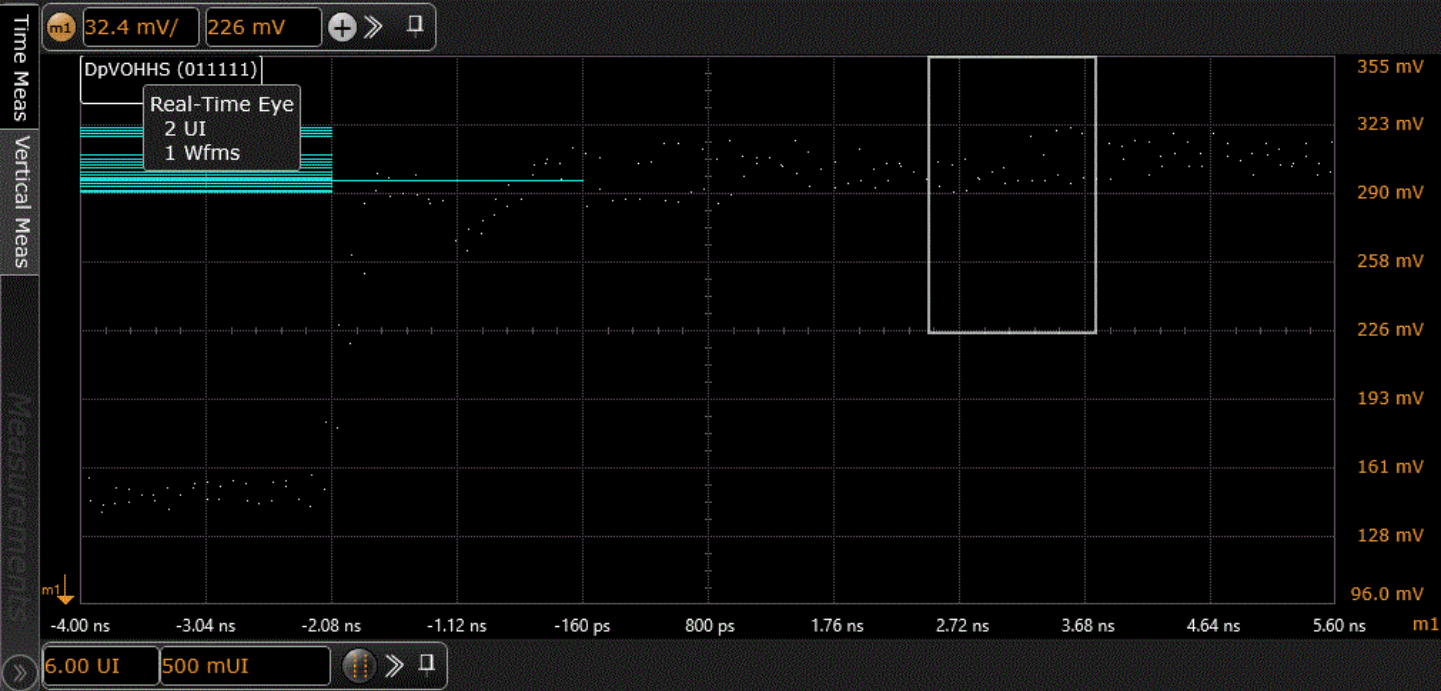

1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.3.6)

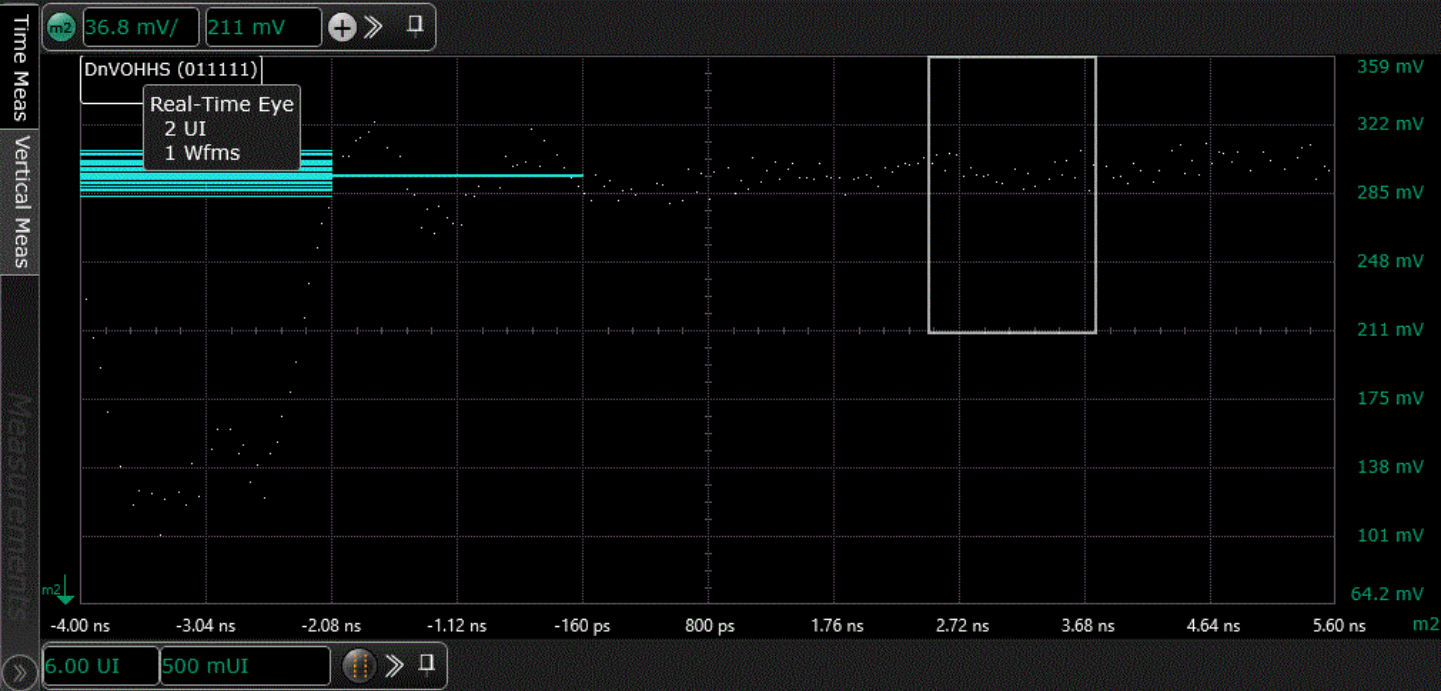
HS Single Ended output high voltage.
 This test will measure the VOHHS based on the reference pulses(100000) of single-ended Dp and Dn signals.
 Actual Value Measurement Name: 8151_Vohhs(Worst)
 Pass Limits: VALUE <= 360.00 mV

Actual Value	Margin	DpVOHHS (011111)	DnVOHHS (011111)	Vohhs(Dp)	Vohhs(Dn)	Number of measurement Vohhs(Dp)
302.95 mV	15.8	(See image)	(See image)	302.95 mV	296.57 mV	2.000
Number of measurement Vohhs(Dn)	ZID	DataLane	Number of HS Burst			
2.000	100 ohm	Lane0	1			

DpVOHHS (011111)
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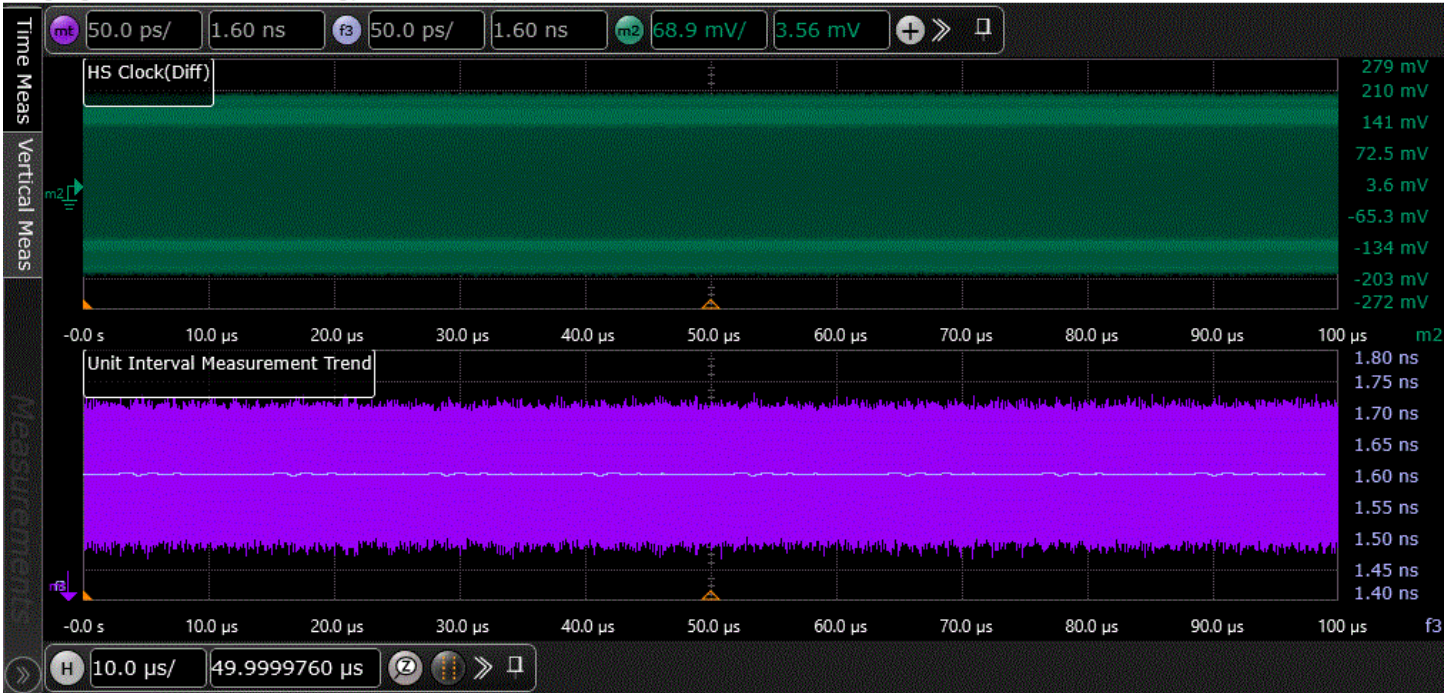


DnVOHHS (011111)
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	1.4.17 HS Clock Instantaneous (UIInst)(Max)					Summary Previous Next		
	Maximum UI instantaneous of HS Clock.					D-PHY Specification v1.0 Section 9.1 Table 26, CTS v1.0(Test 1.4.17)		
	Actual Value Measurement Name: 911_UIInst(Max)							
	Pass Limits: VALUE < 12.500 ns							
Actual Value	Margin	UIInst	UIINST(Max)	UIINST(Mean)	Number of UI	ZID	DataLane	Number of HS Burst
1.602 ns	87.2	(See image)	1.602 ns	1.600 ns	62.500000 k	100 ohm	Lane0	1

UIInst



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1.3.11 HS Data TX 20%-80% Rise Time (tR)

D-PHY Specification v1.0 Section 9.1.1 Table 17, CTS v1.0(Test 1.3.11)

This test is to verify that the 20%-80% rise time of the HS Differential signal is greater than the minimum conformance limit(DataRiseTime_LimitMin) and less than the maximum conformance limit(DataRiseTime_LimitMax).

For CTS v1.0, the minimum conformance limit(DataRiseTime_LimitMin) is 150ps and the maximum conformance limit(DataRiseTime_LimitMax) is 0.3UI.

For CTS v1.1, the minimum conformance limit(DataRiseTime_LimitMin) is 150ps for Datarate = 1Gbps, 100ps for Datarate > 1Gbps. The maximum conformance limit(DataRiseTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps.

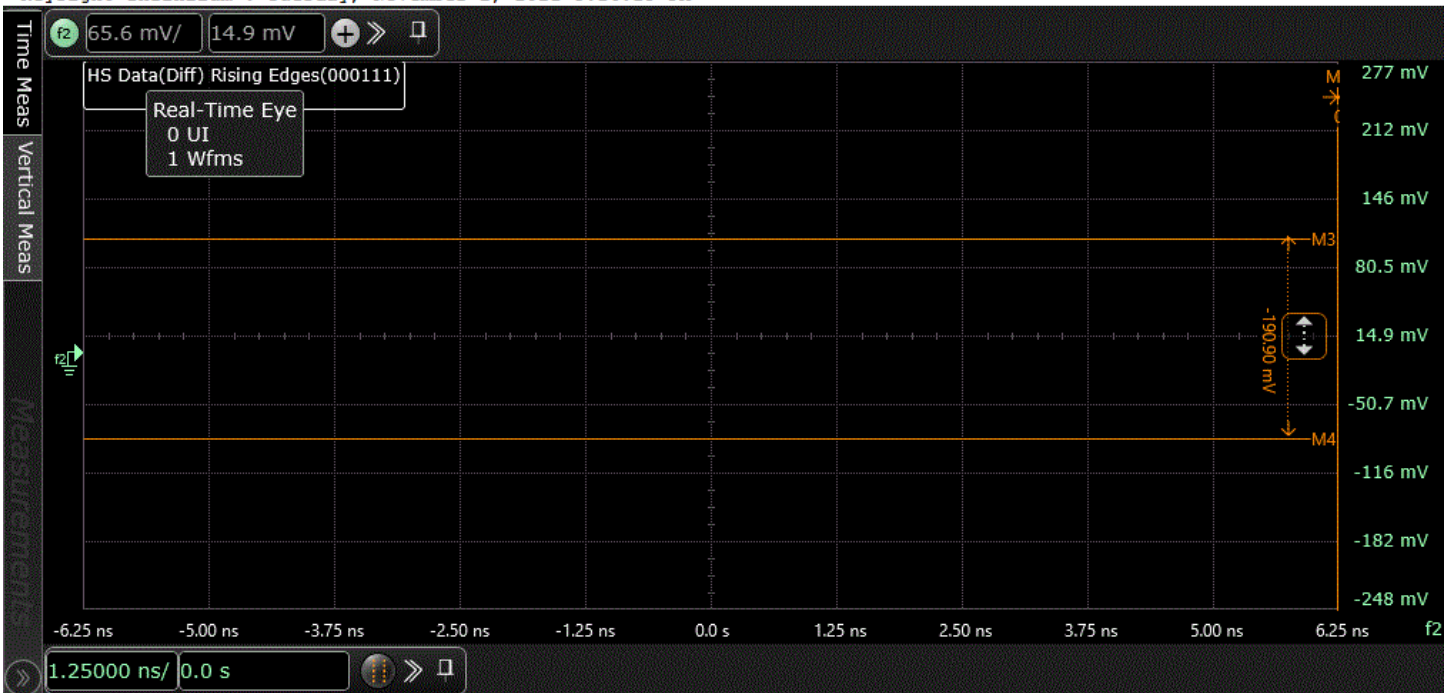
The VOD(0) and VOD(1) measured from Data Lane in Test 1.3.4 will be used to calculate 20/80% reference voltage for rise time measurement in this test.

Actual Value Measurement Name: 8110_Rise Time

Pass Limits: DataRiseTime_LimitMin s < VALUE < DataRiseTime_LimitMax s

Actual Value	Margin	HS TX Risetime	Transition Time Measurement Lower Threshold(%)		Vod(1)	Vod(0)
99.900000000000 E36s	-303E+47	(See image)	20		174.39 mV	-143.78 mV
UIINST(Mean)	Number of Measurement	ZID	DataLane	PassLimit Min (DataRiseTime_LimitMin)		
1.600 ns	0	100 ohm	Lane0	150 ps		
PassLimit Max (DataRiseTime_LimitMax)		Number of HS Burst				
480 ps		1				

HS TX Risetime



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1.3.12 HS Data TX 80%-20% Fall Time (tF)

D-PHY Specification v1.0 Section 9.1.1 Table 17, CTS v1.0(Test 1.3.12)

This test is to verify that the 80%-20% fall time of the HS Differential signal is greater than the minimum conformance limit(DataFallTime_LimitMin) and less than the maximum conformance limit(DataFallTime_LimitMax).
For CTS v1.0, the minimum conformance limit(DataFallTime_LimitMin) is 150ps and the maximum conformance limit(DataFallTime_LimitMax) is 0.3UI.
For CTS v1.1, the minimum conformance limit(DataFallTime_LimitMin) is 150ps for Datarate = 1Gbps, 100ps for Datarate > 1Gbps. The maximum conformance limit(DataFallTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps.
The VOD(0) and VOD(1) measured from Data Lane in Test 1.3.4 will be used to calculate 20/80% reference voltage for fall time measurement in this test.
Actual Value Measurement Name: 8111_Fall Time
Pass Limits: DataFallTime_LimitMin s < VALUE < DataFallTime_LimitMax s

Actual Value	Margin	HS TX Falltime	Transition Time Measurement Lower Threshold(%)	Vod(1)	Vod(0)	UIINST(Mean)
461 ps	5.8	(See image)	20	174.39 mV	-143.78 mV	1.600 ns
Number of Measurement	ZID	DataLane	PassLimit Min (DataFallTime_LimitMin)	PassLimit Max (DataFallTime_LimitMax)		
2	100 ohm	Lane0	150 ps	480 ps		
Number of HS Burst						
1						

HS TX Falltime

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1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.4.7)

HS transmit static common-mode voltage for Clock.
Actual Value Measurement Name: 1811_Vcmtx(Worst)
Pass Limits: 150.00 mV <= VALUE <= 250.00 mV

Actual Value	Margin	HS Clock TX Common Mode Voltage	Vcmtx(Differential-1)	Number of Vcmtx(Differential-1) Measured
207.14 mV	42.9	(See image)	202.78 mV	31.251000 k
Vcmtx(Differential-0)	Number of Vcmtx(Differential-0) Measured		ZID	Number of HS Burst
207.14 mV	31.250000 k		100 ohm	1

HS Clock TX Common Mode Voltage


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1.4.8 HS Clock TX Vcmtx Mismatch

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.4.8)

VCMTX mismatch when output is Differential-1 or Differential-0.

Actual Value Measurement Name: 1812_Vcmtx Mismatch

Pass Limits: 0.00000 V <= VALUE <= 5.00 mV

Actual Value	Margin	Vcmtx(Differential-1)	Vcmtx(Differential-0)	ZID	Number of HS Burst
2.18 mV	43.6	202.78 mV	207.14 mV	100 ohm	1

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1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))

D-PHY Specification v1.0 Section 8.1.1 Table 17, CTS v1.0(Test 1.4.10)

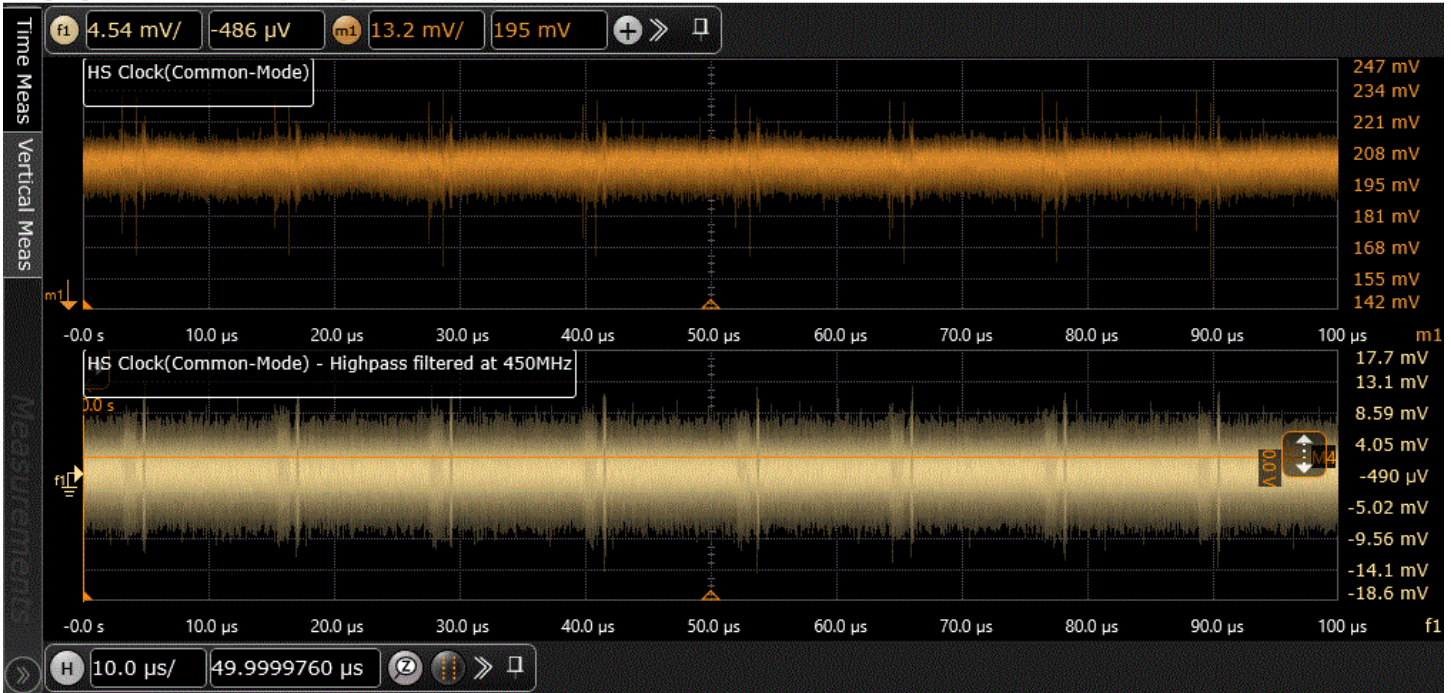
Common-level variations above 450MHz.

Actual Value Measurement Name: 1812_Vcmtx(HF)

Pass Limits: VALUE < 15.00 mV

Actual Value	Margin	Common Level Variations(>450Mhz)	ZID	Number of HS Burst
2.59 mV	82.7	(See image)	100 ohm	1

Common Level Variations(>450Mhz)



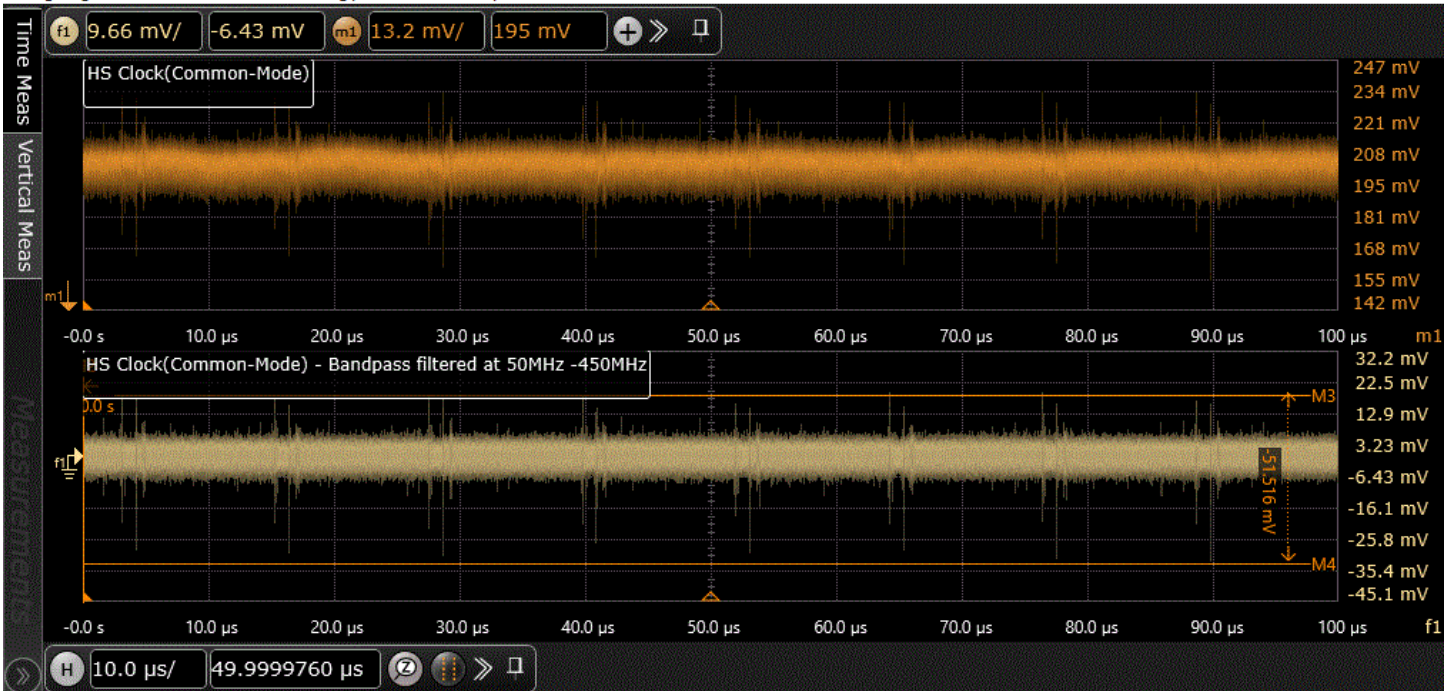
1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))

D-PHY Specification v1.0 Section 8.1.1 Table 17, CTS v1.0(Test 1.4.9)

Common-level variation between 50-450MHz.
Actual Value Measurement Name: 1819_Vcmbx(LF)
Pass Limits: VALUE < 25.00 mV

Actual Value	Margin	Common Level Variations(50-450MHz)	ZID	Number of HS Burst
32.19 mV	-28.8	(See image)	100 ohm	1

Common Level Variations(50-450MHz)



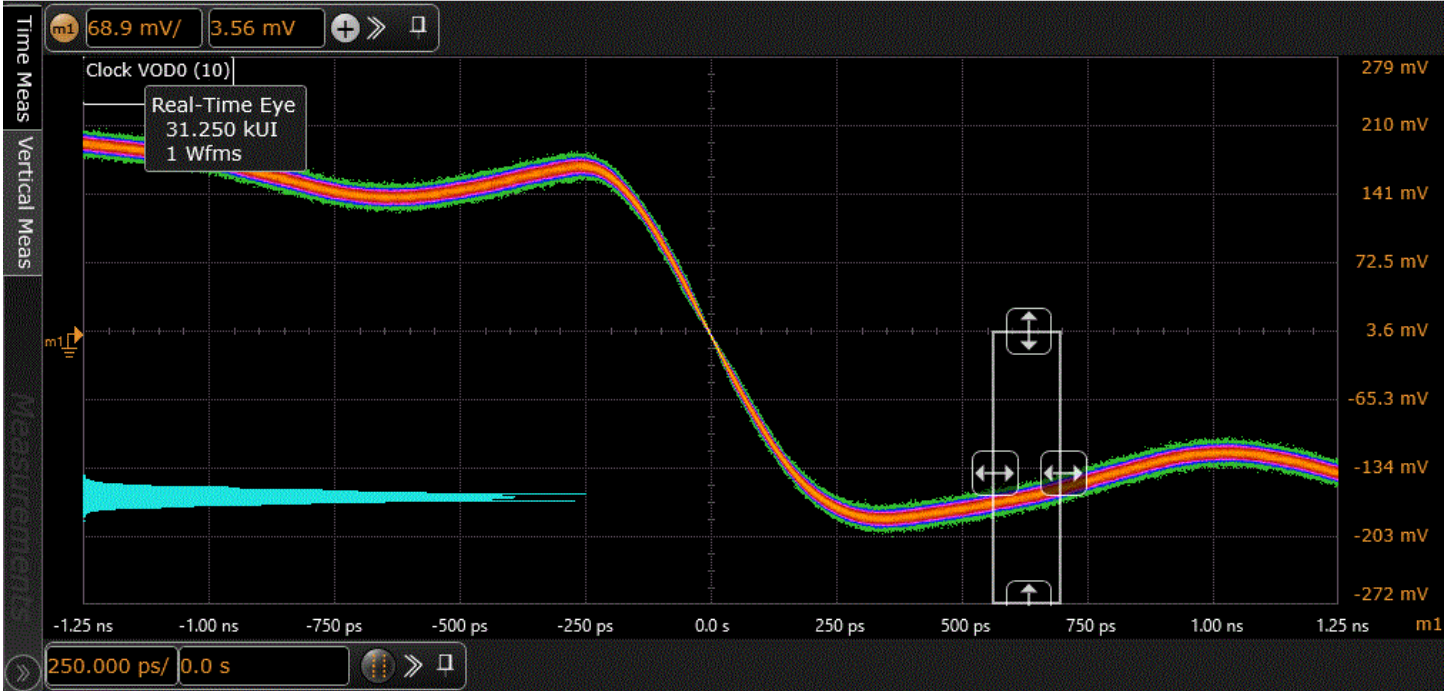
1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.4.4)

HS clock transmitter differential voltage.
Actual Value Measurement Name: 18131_Vod0(Mean)
Pass Limits: -270.00 mV <= VALUE <= -140.00 mV

Actual Value	Margin	Clock VOD0 (10)	Vod(Differential-0)	Number of measurement	ZID	Number of HS Burst
-163.10 mV	17.8	(See image)	-163.10 mV	31.250000 k	100 ohm	1

Clock VOD0 (10)


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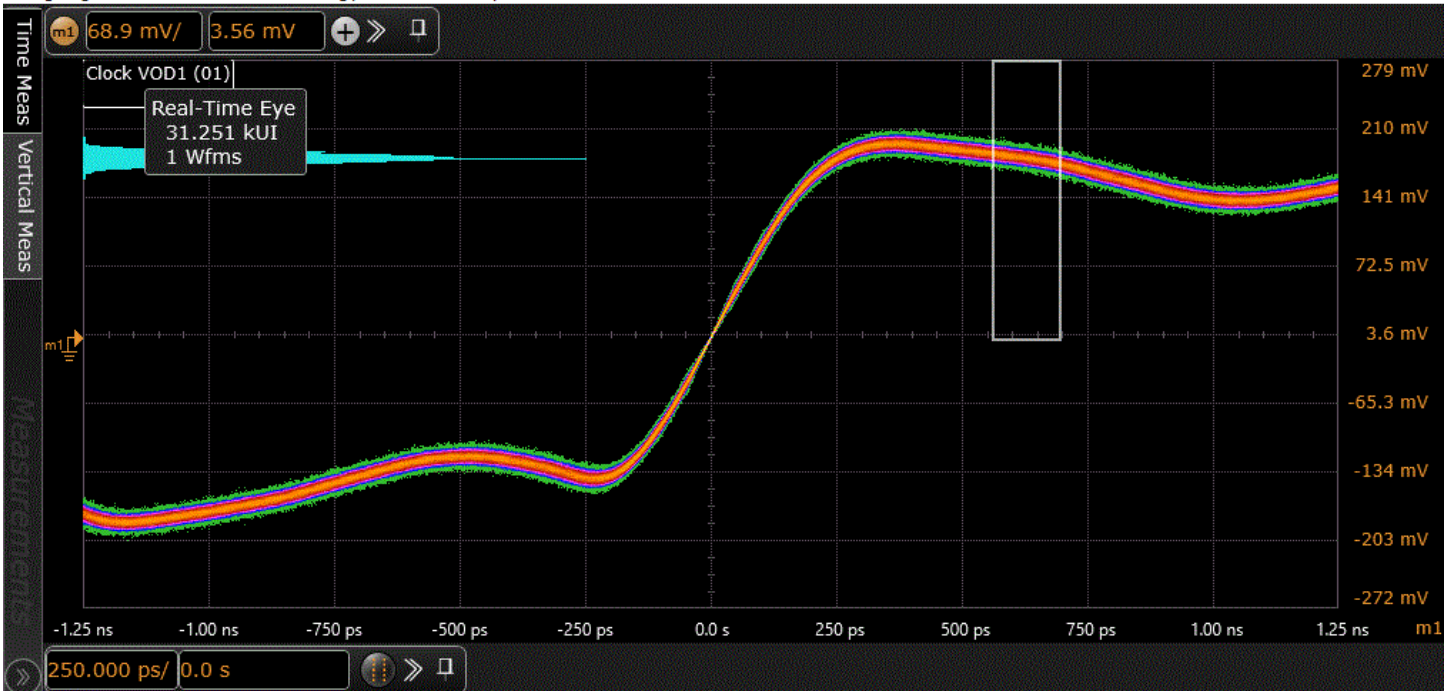

1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.4.4)

HS clock transmitter differential voltage.
Actual Value Measurement Name: 18132_Vod1(Mean)
Pass Limits: 140.00 mV <= VALUE <= 270.00 mV

Actual Value	Margin	Clock VOD1 (01)	Vod(Differential-1)	Number of measurement	ZID	Number of HS Burst
180.77 mV	31.4	(See image)	180.77 mV	31.251000 k	100 ohm	1

Clock VOD1 (01)


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1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.4.5)

VOD mismatch when output is Differential-1 or Differential-0.
Actual Value Measurement Name: 18141_Vod Mismatch
Pass Limits: VALUE <= 10.00 mV

Actual Value	Margin	Vod(Differential-1)	Vod(Differential-0)	ZID	Number of HS Burst
17.67 mV	-76.7	180.77 mV	-163.10 mV	100 ohm	1

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1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)

D-PHY Specification v1.0 Section 8.1.1 Table 16, CTS v1.0(Test 1.4.6)

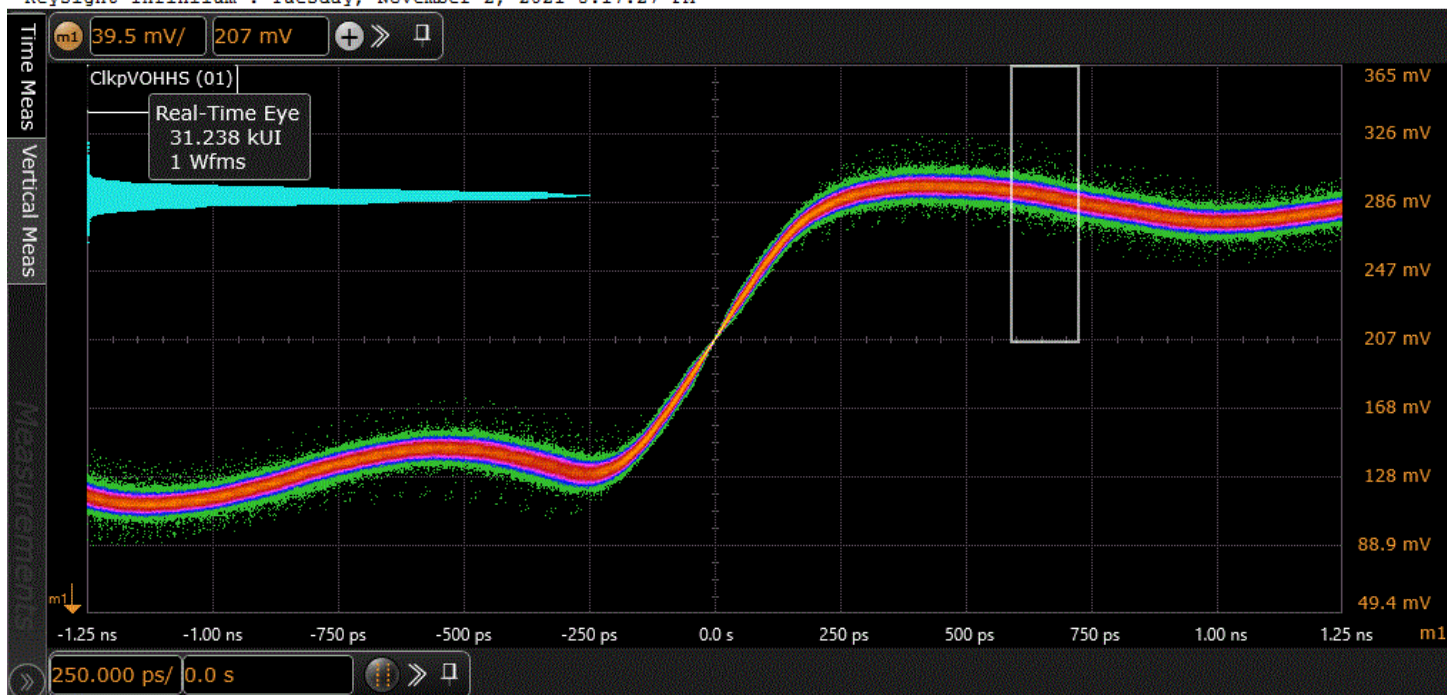
HS Single Ended output high voltage.
Actual Value Measurement Name: 18151_Vohhs(Worst)
Pass Limits: VALUE <= 360.00 mV

Actual Value	Margin	ClkpVOHHS (01)	ClknVOHHS (01)	Vohhs(Clkp)	Vohhs(Clkn)	Number of measurement Vohhs(Clkp)
289.97 mV	19.5	(See image)	(See image)	289.97 mV	286.57 mV	31.238000 k

Number of measurement Vohhs(Clkkn)	ZID	Number of HS Burst
31.230000 k	100 ohm	1

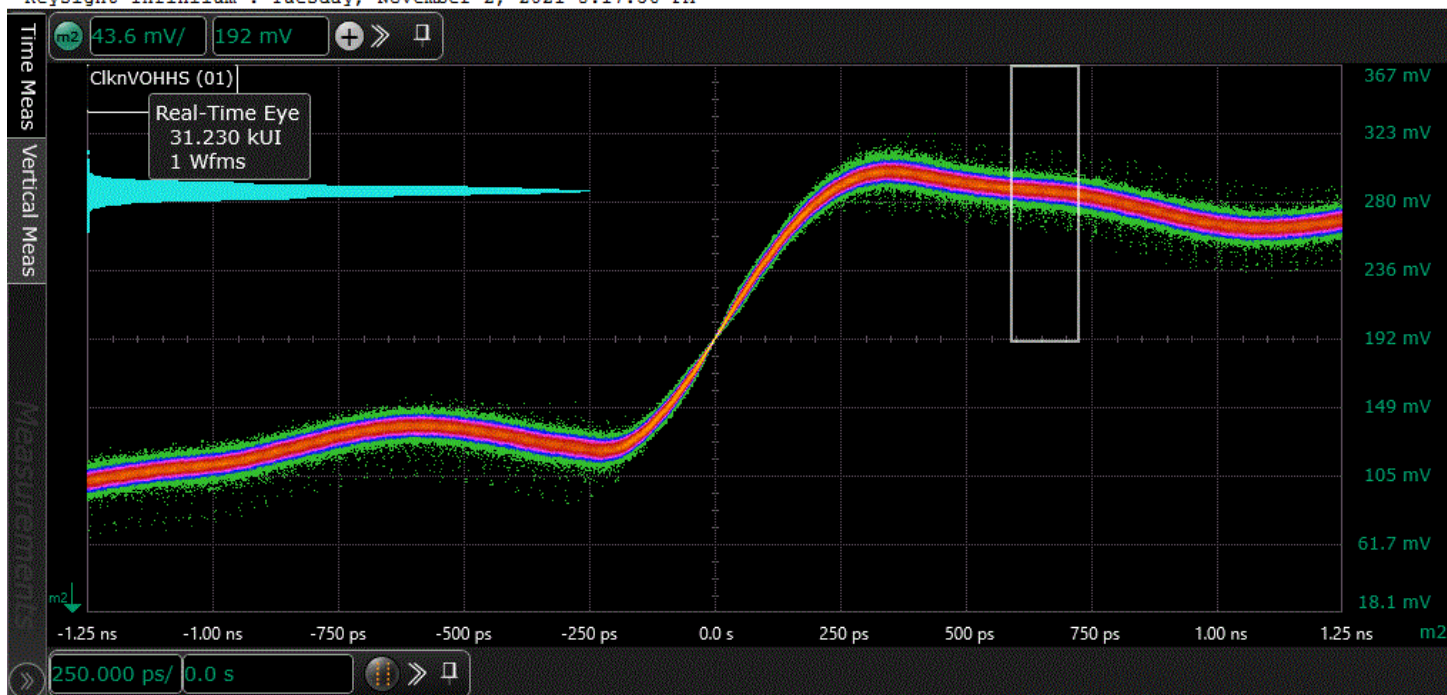
ClkpVOHHS (01)

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ClknVOHHS (01)

Keysight Infiniium : Tuesday, November 2, 2021 8:17:36 PM



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1.4.11 HS Clock TX 20%-80% Rise Time (tR)

D-PHY Specification v1.0 Section 9.1.1 Table 17, CTS v1.0(Test 1.4.11)

This test is to verify that the 20%-80% rise time of the HS Differential signal is greater than the minimum conformance limit(CLK RiseTime_LimitMin) and less than the maximum conformance limit(CLK RiseTime_LimitMax).

For CTS v1.0, the minimum conformance limit(CLK RiseTime_LimitMin) is 150ps and the maximum conformance limit(CLK RiseTime_LimitMax) is 0.3UI.

For CTS v1.1, the minimum conformance limit(CLK RiseTime_LimitMin) is 150ps for Datarate = 1Gbps, 100ps for Datarate > 1Gbps. The maximum conformance limit(CLK RiseTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps.

The VOD(0) and VOD(1) measured from Clock Lane in Test 1.4.4 will be used to calculate 20/80% reference voltage for rise time measurement in this test.

Actual Value Measurement Name: 18110_RiseTime

Pass Limits: CLK RiseTime_LimitMin s < VALUE < CLK RiseTime_LimitMax s

Actual Value	Margin	HS Clock TX Risetime	Transition Time Measurement Lower Threshold(%)	Vod(1)	Vod(0)	UIINST(Mean)
233 ps	25.2	(See image)	20	180.77 mV	-163.10 mV	1.600 ns
Number of Measurement	ZID	PassLimit Min (CLK RiseTime_LimitMin)	PassLimit Max (CLK RiseTime_LimitMax)	Number of HS Burst		
31.251 k	100 ohm	150 ps	480 ps	1		

HS Clock TX Risetime

1.4.12 HS Clock TX 80%-20% Fall Time (tF) D-PHY Specification v1.0 Section 9.1.1 Table 17, CTS v1.0 (Test 1.4.12)

Pass Limits: CLKFallTime_LimitMin s < V_{VALUE} < CLKFallTime_LimitMax s

Number of Measurement	ZID	PassLimit Min (CLKFallTime_LimitMin)	PassLimit Max (CLKFallTime_LimitMax)	Number of HS Burst
31.250 k	100 ohm	150 ps	480 ps	1

Time Meas: 68.9 mV/ 3.56 mV

Vertical Meas: 3.56 mV

HS Clock(Diff) Falling Edges(10)

Real-Time Eye
31.250 kUI
1 Wfms

279 mV
210 mV
141 mV
72.5 mV
3.6 mV
-65.3 mV
-134 mV
-203 mV
-272 mV

-1.25 ns -1.00 ns -750 ps -500 ps -250 ps 0.0 s 250 ps 500 ps 750 ps 1.00 ns 1.25 ns

250.000 ps/ 0.0 s


1.4.17 HS Clock Instantaneous (Ulinst)(Min)
D-PHY Specification v1.0 Section 9.1 Table 26, CTS v1.0 (Test 1.4.17)

Pass Limits: VALUE >= Ulinst Min Limit s

Number of HS Burst
1



1.3.1 HS Entry: DATA TLPX

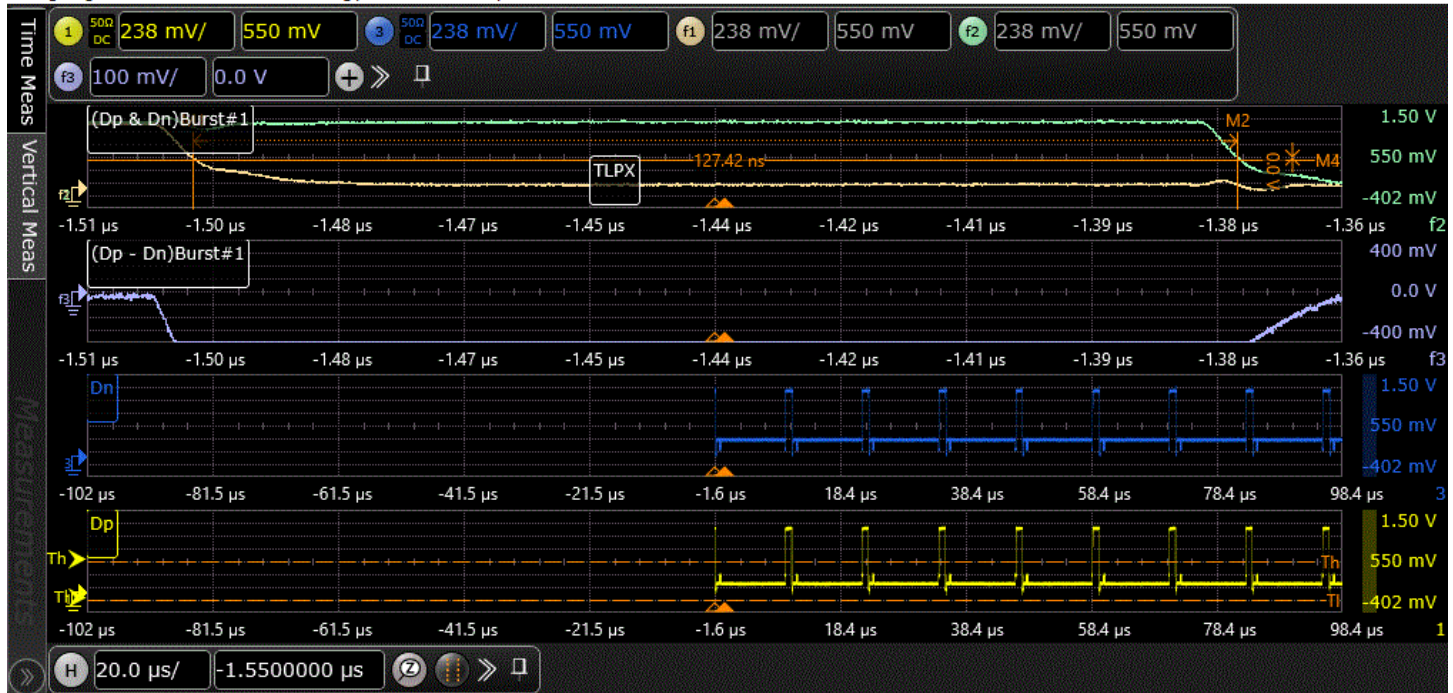
D-PHY Specification v1.0 Section 5.9 Table 14, CTS v1.0(Test 1.3.1)

Length of any Low-Power state period.
Actual Value Measurement Name: 511_TLPX
Pass Limits: VALUE >= 50.00 ns

Actual Value	Margin	TLPX	ZID	DataLane	Number of HS burst
127.42 ns	154.8	(See image)	100 ohm	Lane0	1

TLPX

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1.3.2 HS Entry: DATA TX THS-PREPARE

D-PHY Specification v1.0 Section 5.9 Table 14, CTS v1.0(Test 1.3.2)

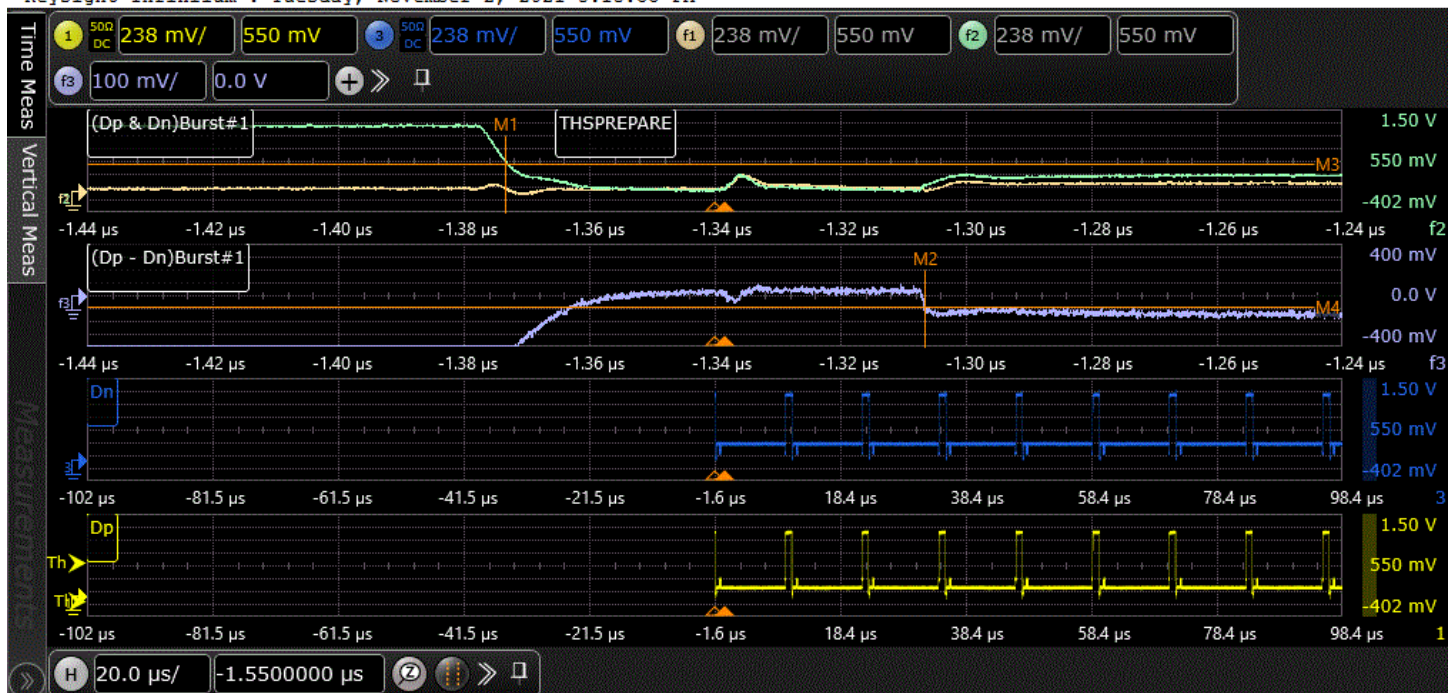
Time to drive LP-00 to prepare for HS Transmission.
THSPrepare_LimitMin is based on $40\text{ns} + 4 \cdot \text{UI}$.
THSPrepare_LimitMax is based on $85\text{ns} + 6 \cdot \text{UI}$.
Actual Value Measurement Name: 557_THS-PREPARE
Pass Limits: THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s

Actual Value	Margin	THSPREPRE	UIINST(Mean)	ZID	DataLane	PassLimit Min (THSPrepare_LimitMin)
66.94 ns	42.6	(See image)	1.600 ns	100 ohm	Lane0	46.40 ns

PassLimit Max (THSPrepare_LimitMax)	Number of HS burst
94.60 ns	1

THSPREPRE

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1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO

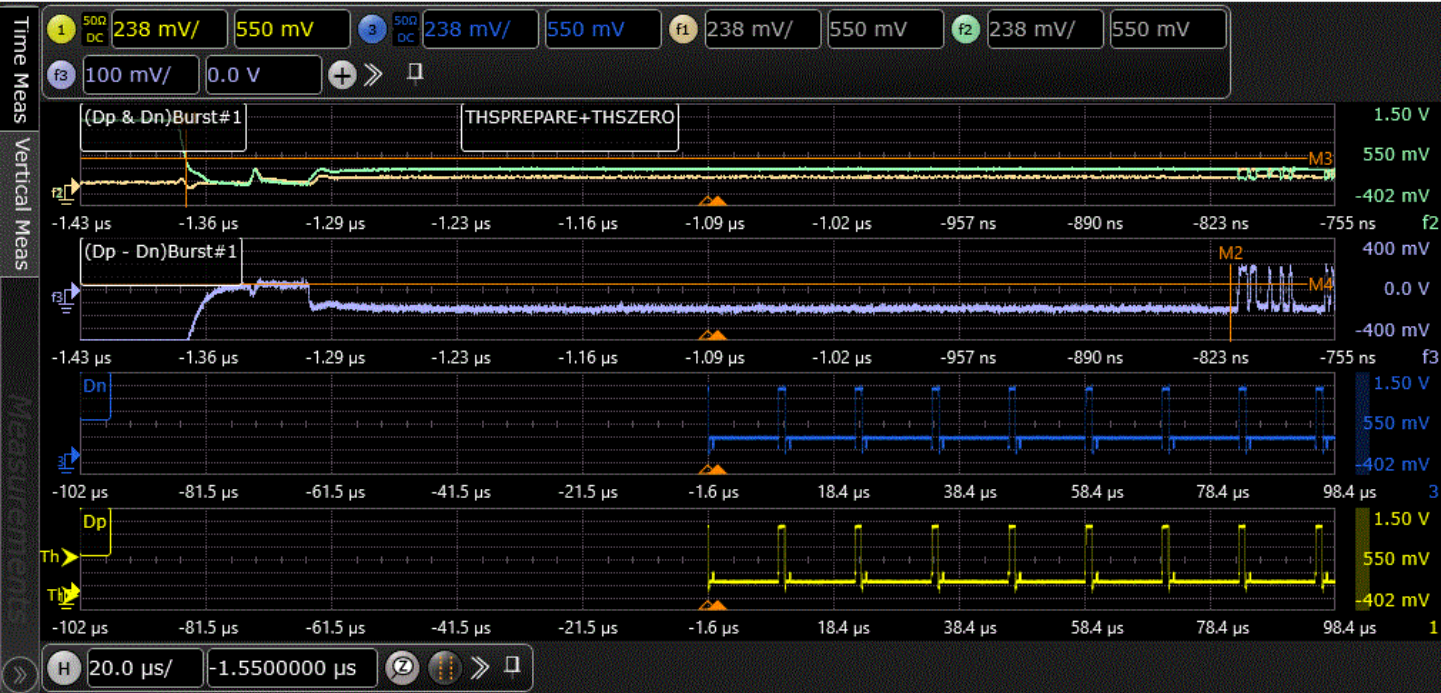
D-PHY Specification v1.0 Section 5.9 Table 14, CTS v1.0(Test 1.3.3)

THS-PREPARE+Time to drive HS-0 before Sync sequence.
TXTHSPrepareTHSZero_LimitMin is based on 145ns+10*U1.
Actual Value Measurement Name: 558_THS-PREPARE+THS-ZERO
Pass Limits: VALUE >= TXTHSPrepareTHSZero_LimitMin s

Actual Value	Margin	THSPREPRE THSZERO	UIINST(Mean)	VHS_ZERO	ZID	DataLane
561.41 ns	248.7	(See image)	1.600 ns	-148.02 mV	100 ohm	Lane0

PassLimit Min (TXTHSPrepareTHSZero_LimitMin)	Number of HS burst
161.00 ns	1

THSPREPRE_THSZERO
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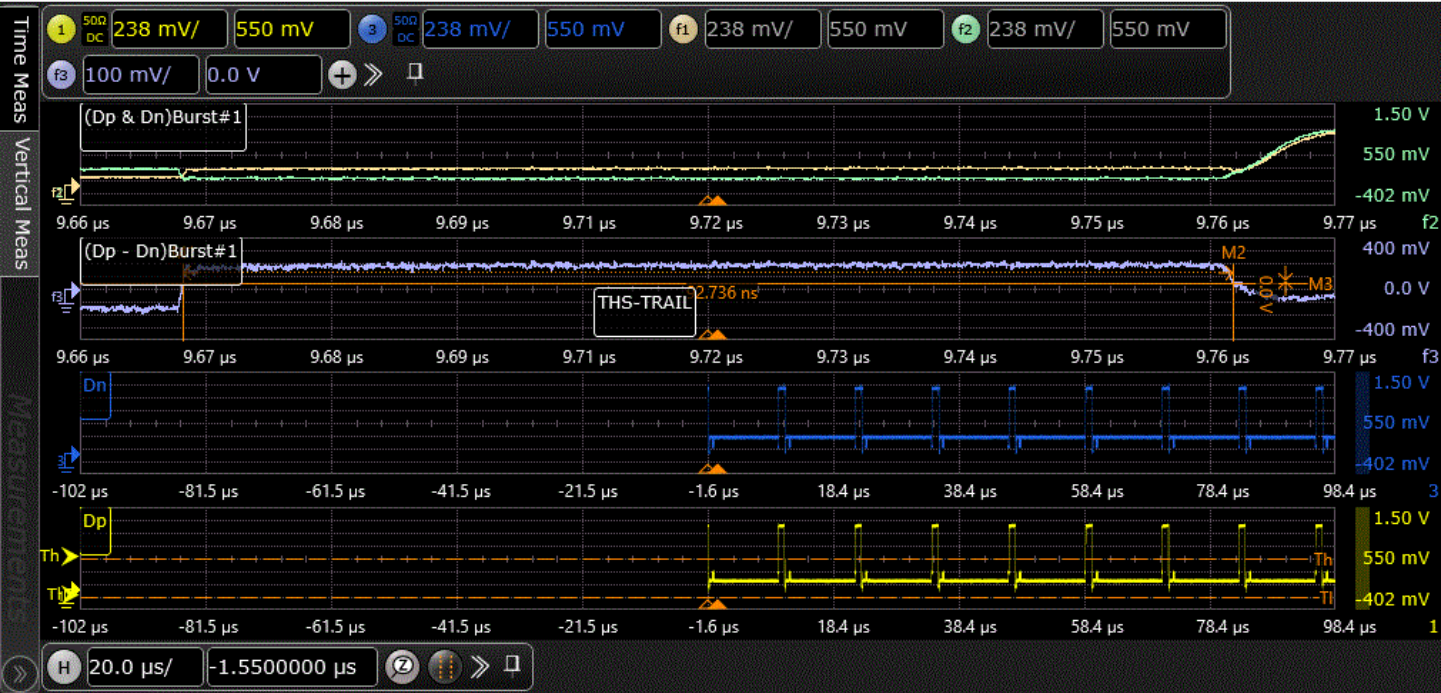
1.3.13 HS Exit: DATA TX THS-TRAIL

D-PHY Specification v1.0 Section 5.9 Table 14, CTS v1.0 (Test 1.3.13)

Time to drive flipped differential state after last payload data bit of a HS transmission burst.
 TTXHSTrail_LimitMin is based on $60ns + n * 4 * UI$.
 The THS-SKIP parameter is useful to avoid glitch problem during THS-TRAIL measurement.
 Any transition on the Data Lane in THS-SKIP time interval will be ignored when finding last payload data bit of HS transmission burst.
 The default value of THS-SKIP is set to 0s to prevent invalid THS-TRAIL measurement.
 Actual Value Measurement Name: 546_THS-TRAIL
 Pass Limits: VALUE >= TTXHSTrail_LimitMin s

Actual Value	Margin	THSTRAIL	THS-SKIP(s)	ZID	DataLane	PassLimit Min (TXTHSTrail_LimitMin)	Number of HS burst
92.74 ns	42.7	(See image)	0.0000000000000 s	100 ohm	Lane0	65.00 ns	1

THSTRAIL
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1.3.14 HS Exit: DATA TX TREOT

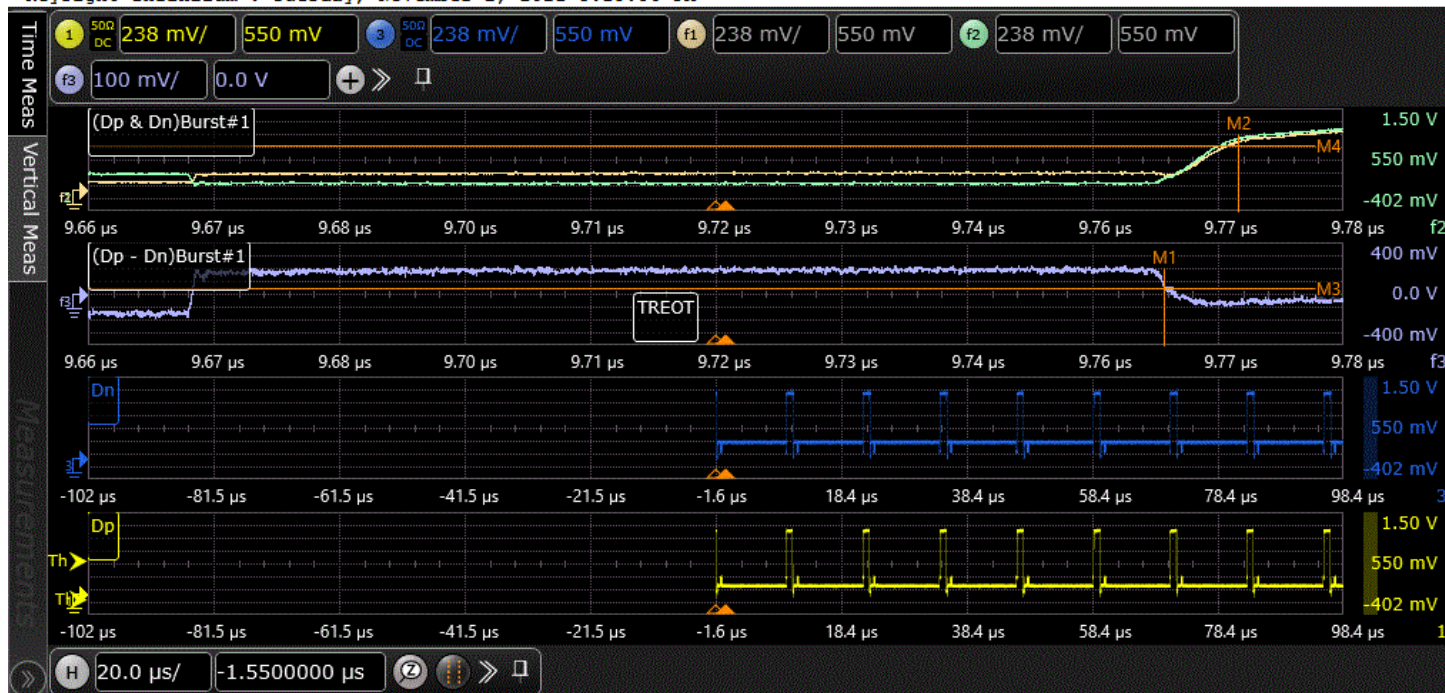
D-PHY Specification v1.0 Section 8.1.2 Table 19, CTS v1.0(Test 1.3.14)

30%-85% rise time and fall time
Actual Value Measurement Name: 549_TREOT
Pass Limits: VALUE <= 35.00 ns

Actual Value	Margin	TREOT	ZID	DataLane	Number of HS burst
7.13 ns	79.6	(See image)	100 ohm	Lane0	1

TREOT

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1.3.15 HS Exit: DATA TX TEOT

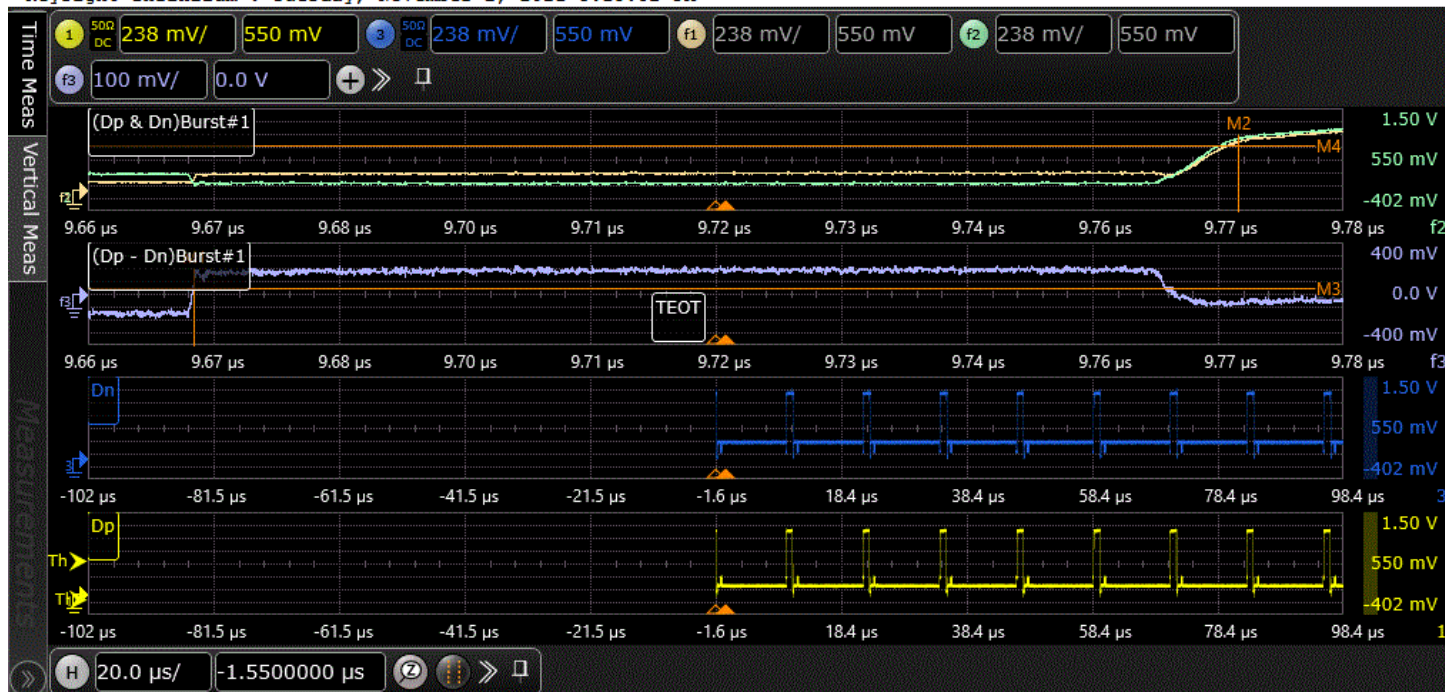
D-PHY Specification v1.0 Section 5.9 Table 14, CTS v1.0(Test 1.3.15)

Time from start of THS-TRAIL period to start of LP-11 state.
TXTEOT_LimitMax is based on $105ns + n \cdot 12 \cdot UI$.
Actual Value Measurement Name: 547_TEOT
Pass Limits: VALUE <= TXTEOT_LimitMax s

Actual Value	Margin	TEOT	UIINST(Mean)	ZID	DataLane	PassLimit Max (TXTEOT_LimitMax)	Number of HS burst
99.86 ns	19.6	(See image)	1.600 ns	100 ohm	Lane0	124.20 ns	1

TEOT

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1.3.16 HS Exit: DATA TX THS-EXIT

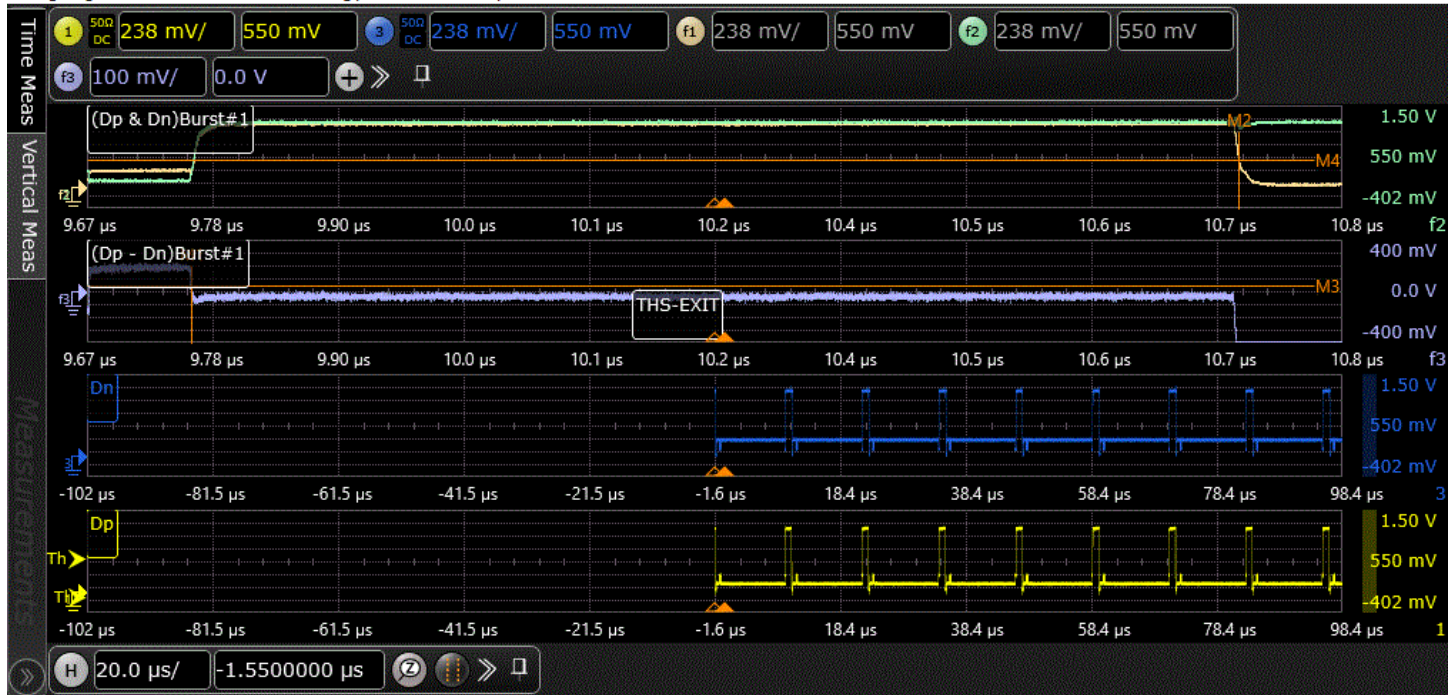
D-PHY Specification v1.0 Section 5.9 Table 14, CTS v1.0(Test 1.3.16)

Time to drive LP-11 after HS burst.
Actual Value Measurement Name: 548_THS-EXIT
Pass Limits: VALUE >= 100.00 ns

Actual Value	Margin	THSEXIT	Notes:	ZID	DataLane	Number of HS burst
960.00 ns	860.0	(See image)		100 ohm	Lane0	1

THSEXIT

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1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)

D-PHY Specification v1.0 Section 9.2.1 Table 27, CTS v1.0(Test 1.5.4)

Data to Clock Skew [measured at transmitter].

Actual Value Measurement Name: 913_Tskew(Worst)

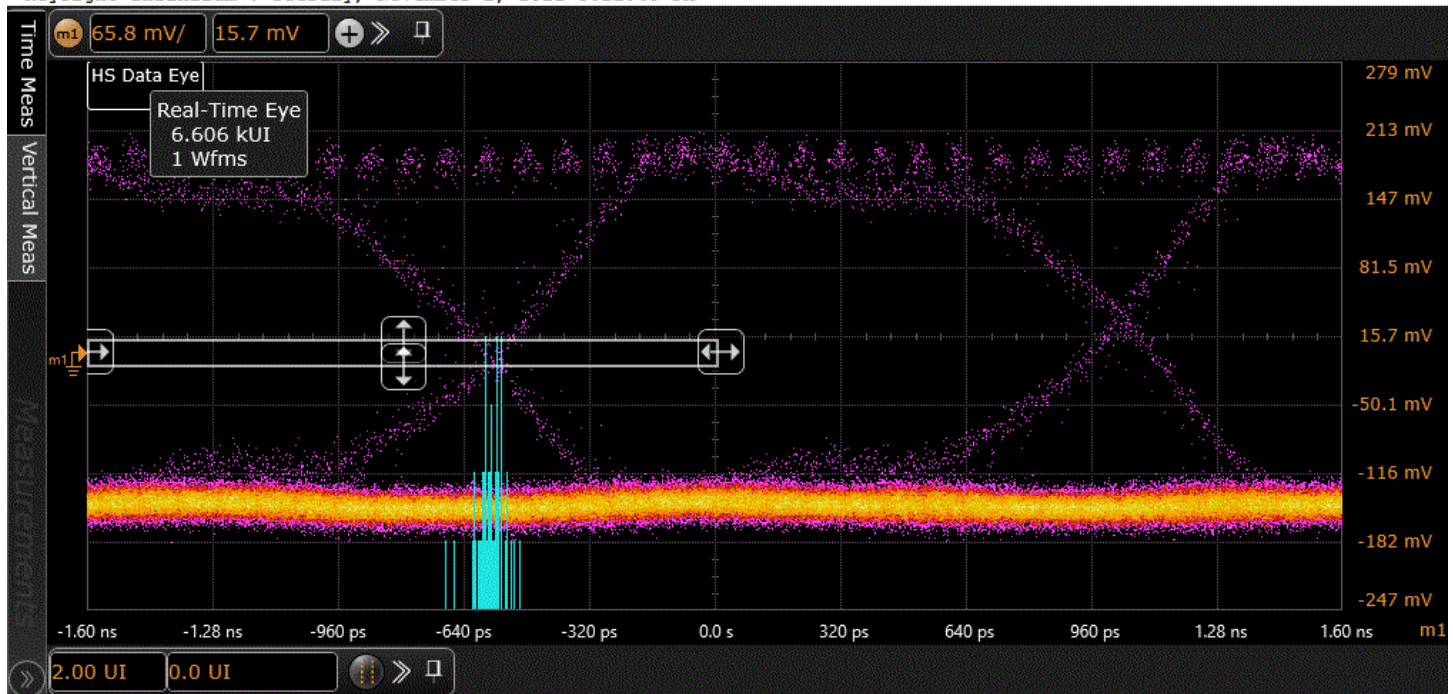
Pass Limits: MinMaxTSkewTest LimitMin UIinst <= VALUE <= MinMaxTSkewTest LimitMax UIinst

Actual Value	Margin	LeftCrossing	UIINST(Mean)	TSkew(Min)	TSkew(Max)	No Of Measurement	ZID	DataLane
-192 mUIinst	-14.0	(See image)	1.6000 ns	-307.5 ps	-115.0 ps	6.606000 k	100 ohm	Lane0

PassLimit Min (MinMaxTSkewTest_LimitMin)	PassLimit Max (MinMaxTSkewTest_LimitMax)	Number of HS Burst
-150 mUIinst	150 mUIinst	1

LeftCrossing

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1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean)

D-PHY Specification v1.0 Section 9.2.1 Table 27, CTS v1.0(Test 1.5.4)

Data to Clock Skew [measured at transmitter].

Actual Value Measurement Name: 9131_Tskew(Mean)

Pass Limits: MeanTSkewTest LimitMin UIinst <= VALUE <= MeanTSkewTest LimitMax UIinst

Actual Value	Margin	UIINST(Mean)	TSkew(Mean)	No Of Measurement	ZID	DataLane	PassLimit Min (MeanTSkewTest_LimitMin)
-144 mUIinst	2.0	1.6000 ns	-230.5 ps	6.606000 k	100 ohm	Lane0	-150 mUIinst

PassLimit Max (MeanTSkewTest_LimitMax)	Number of HS Burst
150 mUIinst	1