



# DisplayPort Test Report

Overall Result: FAIL

Test Configuration Details	
Device Description	
Test Specification	1.2b
Test Session Details	
Fixture Type	Agilent W2641B
Infiniium SW Version	04.60.0023
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY52260152
Application SW Version	3.40
Debug Mode Used	No
Probe (Channel 1)	Model: 1169A Serial: US55012851 Head: N5380A/B Atten: Calibrated (20 MAR 2017 21:04:14), Using Cal Atten (2.0430E+000) Skew: Calibrated (20 MAR 2017 21:04:21), Using Cal Skew
Probe (Channel 2)	Model: 1169A Serial: US49413004 Head: N5380A/B Atten: Calibrated (17 MAR 2017 19:06:59), Using Cal Atten (1.9949E+000) Skew: Calibrated (17 MAR 2017 19:07:05), Using Cal Skew
Probe (Channel 3)	Model: 1169A Serial: US49413002 Head: N5380A/B Atten: Calibrated (17 MAR 2017 19:07:42), Using Cal Atten (2.0137E+000) Skew: Calibrated (17 MAR 2017 19:07:48), Using Cal Skew
Probe (Channel 4)	Model: 1169A Serial: US49413755 Head: N5380A/B Atten: Calibrated (17 MAR 2017 19:08:20), Using Cal Atten (2.1402E+000) Skew: Calibrated (17 MAR 2017 19:08:26), Using Cal Skew
Last Test Date	2017-03-21 20:51:01 UTC +08:00

## Summary of Results

Test Statistics	
Failed	15
Passed	151
Total	166

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	1	Lane 0/ Lane 1 - Inter Pair Skew Test	20.0117 UI	49.9 %	13.3000 UI <= VALUE <= 26.7000 UI
✓	0	1	Lane 0/ Lane 2 - Inter Pair Skew Test	39.8551 UI	48.9 %	33.3000 UI <= VALUE <= 46.7000 UI
✓	0	1	Lane 0/ Lane 3 - Inter Pair Skew Test	59.9906 UI	49.9 %	53.3000 UI <= VALUE <= 66.7000 UI
✓	0	1	Lane 1/ Lane 2 - Inter Pair Skew Test	19.8471 UI	48.9 %	13.3000 UI <= VALUE <= 26.7000 UI
✓	0	1	Lane 1/ Lane 3 - Inter Pair Skew Test	39.9957 UI	50.0 %	33.3000 UI <= VALUE <= 46.7000 UI
✓	0	1	Lane 2/ Lane 3 - Inter Pair Skew Test	20.1414 UI	48.9 %	13.3000 UI <= VALUE <= 26.7000 UI
✓	0	1	Lane 0 - D10.2 Total Jitter Test (TP3 EQ)	108.700 mUI	72.8 %	VALUE <= 400.000 mUI
✓	0	1	Lane 1 - D10.2 Total Jitter Test (TP3 EQ)	95.500 mUI	76.1 %	VALUE <= 400.000 mUI
✓	0	1	Lane 2 - D10.2 Total Jitter Test (TP3 EQ)	100.000 mUI	75.0 %	VALUE <= 400.000 mUI
✓	0	1	Lane 3 - D10.2 Total Jitter Test (TP3 EQ)	102.600 mUI	74.4 %	VALUE <= 400.000 mUI
✓	0	1	Lane 0 - D10.2 Deterministic Jitter (TP3 EQ)	43.800 mUI	82.5 %	VALUE <= 250.000 mUI
✓	0	1	Lane 1 - D10.2 Deterministic Jitter (TP3 EQ)	32.200 mUI	87.1 %	VALUE <= 250.000 mUI
✓	0	1	Lane 2 - D10.2 Deterministic Jitter (TP3 EQ)	36.300 mUI	85.5 %	VALUE <= 250.000 mUI
✓	0	1	Lane 3 - D10.2 Deterministic Jitter (TP3 EQ)	37.800 mUI	84.9 %	VALUE <= 250.000 mUI
✓	0	1	Lane 0 - D10.2 Random Jitter (TP3 EQ)	5.300 mUI	97.7 %	VALUE <= 230.000 mUI
✓	0	1	Lane 1 - D10.2 Random Jitter (TP3 EQ)	5.200 mUI	97.7 %	VALUE <= 230.000 mUI
✓	0	1	Lane 2 - D10.2 Random Jitter (TP3 EQ)	5.200 mUI	97.7 %	VALUE <= 230.000 mUI
✓	0	1	Lane 3 - D10.2 Random Jitter (TP3 EQ)	5.300 mUI	97.7 %	VALUE <= 230.000 mUI
✓	0	3	Lane 0 - Main Link Frequency Compliance	5.457 ppm	5.3 %	-5.300000 kppm <= VALUE <= 300.000 ppm
✓	0	3	Lane 1 - Main Link Frequency Compliance	-2.778 ppm	5.4 %	-5.300000 kppm <= VALUE <= 300.000 ppm
✓	0	3	Lane 2 - Main Link Frequency Compliance	5.861 ppm	5.3 %	-5.300000 kppm <= VALUE <= 300.000 ppm
✓	0	3	Lane 3 - Main Link Frequency Compliance	6.049 ppm	5.2 %	-5.300000 kppm <= VALUE <= 300.000 ppm
✓	0	1	Lane 0 - HBR2CPAT Eye Diagram Test (TP3 EQ)	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	Lane 1 - HBR2CPAT Eye Diagram Test (TP3 EQ)	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	Lane 2 - HBR2CPAT Eye Diagram Test (TP3 EQ)	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	Lane 3 - HBR2CPAT Eye Diagram Test (TP3 EQ)	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	Lane 0 - HBR2CPAT Total Jitter Test (TP3 EQ)	262.600 mUI	54.7 %	VALUE <= 580.000 mUI
✓	0	1	Lane 1 - HBR2CPAT Total Jitter Test (TP3 EQ)	286.700 mUI	50.6 %	VALUE <= 580.000 mUI
✓	0	1	Lane 2 - HBR2CPAT Total Jitter Test (TP3 EQ)	300.000 mUI	48.3 %	VALUE <= 580.000 mUI
✓	0	1	Lane 3 - HBR2CPAT Total Jitter Test (TP3 EQ)	289.700 mUI	50.1 %	VALUE <= 580.000 mUI
✓	0	1	Lane 0 - HBR2CPAT Deterministic Jitter Test (TP3 EQ)	168.200 mUI	65.7 %	VALUE <= 490.000 mUI
✓	0	1	Lane 1 - HBR2CPAT Deterministic Jitter Test (TP3 EQ)	191.500 mUI	60.9 %	VALUE <= 490.000 mUI
✓	0	1	Lane 2 - HBR2CPAT Deterministic Jitter Test (TP3 EQ)	205.100 mUI	58.1 %	VALUE <= 490.000 mUI
✓	0	1	Lane 3 - HBR2CPAT Deterministic Jitter Test (TP3 EQ)	194.500 mUI	60.3 %	VALUE <= 490.000 mUI
✓	0	9	Lane 0 - PLTPAT - Peak to Peak Voltage Test	1.081 V	21.7 %	VALUE <= 1.380 V
✓	0	10	Lane 1 - PLTPAT - Peak to Peak Voltage Test	1.093 V	20.8 %	VALUE <= 1.380 V
✓	0	10	Lane 2 - PLTPAT - Peak to Peak Voltage Test	1.091 V	20.9 %	VALUE <= 1.380 V
✓	0	10	Lane 3 - PLTPAT - Peak to Peak Voltage Test	1.099 V	20.4 %	VALUE <= 1.380 V
✓	0	1	Lane 0 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	5.7342 dB	31.4 %	5.2000 dB <= VALUE <= 6.9000 dB
✓	0	1	Lane 0 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.6962 dB	42.3 %	1.6000 dB <= VALUE <= 3.5000 dB
✓	0	1	Lane 1 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	5.6800 dB	28.2 %	5.2000 dB <= VALUE <= 6.9000 dB
✓	0	1	Lane 1 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.6135 dB	46.7 %	1.6000 dB <= VALUE <= 3.5000 dB
✓	0	1	Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	5.4931 dB	17.2 %	5.2000 dB <= VALUE <= 6.9000 dB
✓	0	1	Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.5816 dB	48.3 %	1.6000 dB <= VALUE <= 3.5000 dB
✓	0	1	Lane 3 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	5.9114 dB	41.8 %	5.2000 dB <= VALUE <= 6.9000 dB
✓	0	1	Lane 3 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.7417 dB	39.9 %	1.6000 dB <= VALUE <= 3.5000 dB
✓	0	4	Lane 0 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0)	-2.285 dB	101E+01 %	VALUE <= 250 mdB
✓	0	4	Lane 1 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0)	-1.541 dB	716.4 %	VALUE <= 250 mdB
✓	0	4	Lane 2 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0)	-1.789 dB	815.6 %	VALUE <= 250 mdB
✓	0	4	Lane 3 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0)	-1.785 dB	814.0 %	VALUE <= 250 mdB
✓	0	3	Lane 0 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	5.464 dB	173.2 %	VALUE >= 2.000 dB
✗	3	3	Lane 1 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	.53 mdB	-102.7 %	VALUE >= 2.000 dB
✓	0	3	Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	3.622 dB	81.1 %	VALUE >= 2.000 dB
✗	3	3	Lane 3 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	-109 mdB	-105.5 %	VALUE >= 2.000 dB
✓	0	1	Lane 0 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2)	744 m	5.1 %	VALUE >= 708 m
✓	0	1	Lane 1 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2)	1.134	60.2 %	VALUE >= 708 m
✓	0	1	Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2)	900 m	27.1 %	VALUE >= 708 m
✓	0	1	Lane 3 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2)	1.124	58.8 %	VALUE >= 708 m
✗	2	2	Lane 0 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	-2.523 dB	-257.7 %	VALUE >= 1.600 dB
✓	0	2	Lane 1 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	3.337 dB	108.6 %	VALUE >= 1.600 dB
✓	0	2	Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	2.109 dB	31.8 %	VALUE >= 1.600 dB
✗	2	2	Lane 3 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	155 mdB	-90.3 %	VALUE >= 1.600 dB
✓	0	1	Lane 0 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)	835 m	17.9 %	VALUE >= 708 m
✓	0	1	Lane 1 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)	1.151	62.6 %	VALUE >= 708 m
✓	0	1	Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)	947 m	33.8 %	VALUE >= 708 m
✓	0	1	Lane 3 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)	1.229	73.6 %	VALUE >= 708 m
✓	0	1	Lane 0 - D10.2 Total Jitter Test with No Cable Model (TP3 EQ)	104.600 mUI	73.9 %	VALUE <= 400.000 mUI
✓	0	1	Lane 1 - D10.2 Total Jitter Test with No Cable Model (TP3 EQ)	85.200 mUI	78.7 %	VALUE <= 400.000 mUI
✓	0	1	Lane 2 - D10.2 Total Jitter Test with No Cable Model (TP3 EQ)	96.300 mUI	75.9 %	VALUE <= 400.000 mUI
✓	0	1	Lane 3 - D10.2 Total Jitter Test with No Cable Model (TP3 EQ)	100.400 mUI	74.9 %	VALUE <= 400.000 mUI
✓	0	1	Lane 0 - D10.2 Deterministic Jitter with No Cable (TP3 EQ)	33.700 mUI	86.5 %	VALUE <= 250.000 mUI

✓	0	1	Lane 1 - D10.2 Deterministic Jitter with No Cable (TP3_EQ)	17.100 mUI	93.2%	VALUE <= 250.000 mUI
✓	0	1	Lane 2 - D10.2 Deterministic Jitter with No Cable (TP3_EQ)	28.100 mUI	88.8%	VALUE <= 250.000 mUI
✓	0	1	Lane 3 - D10.2 Deterministic Jitter with No Cable (TP3_EQ)	33.000 mUI	86.8%	VALUE <= 250.000 mUI
✓	0	1	Lane 0 - D10.2 Random Jitter with No Cable (TP3_EQ)	5.800 mUI	97.5%	VALUE <= 230.000 mUI
✓	0	1	Lane 1 - D10.2 Random Jitter with No Cable (TP3_EQ)	5.600 mUI	97.6%	VALUE <= 230.000 mUI
✓	0	1	Lane 2 - D10.2 Random Jitter with No Cable (TP3_EQ)	5.600 mUI	97.6%	VALUE <= 230.000 mUI
✓	0	1	Lane 3 - D10.2 Random Jitter with No Cable (TP3_EQ)	5.500 mUI	97.6%	VALUE <= 230.000 mUI
✓	0	1	Lane 0 - HBR2CPAT Eye Diagram Test with No Cable (TP3_EQ)	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	1	Lane 1 - HBR2CPAT Eye Diagram Test with No Cable (TP3_EQ)	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	1	Lane 2 - HBR2CPAT Eye Diagram Test with No Cable (TP3_EQ)	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	1	Lane 3 - HBR2CPAT Eye Diagram Test with No Cable (TP3_EQ)	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	1	Lane 0 - HBR2CPAT Total Jitter Test with No Cable (TP3_EQ)	275.300 mUI	52.5%	VALUE <= 580.000 mUI
✓	0	1	Lane 1 - HBR2CPAT Total Jitter Test with No Cable (TP3_EQ)	277.600 mUI	52.1%	VALUE <= 580.000 mUI
✓	0	1	Lane 2 - HBR2CPAT Total Jitter Test with No Cable (TP3_EQ)	282.200 mUI	51.3%	VALUE <= 580.000 mUI
✓	0	1	Lane 3 - HBR2CPAT Total Jitter Test with No Cable (TP3_EQ)	301.300 mUI	48.1%	VALUE <= 580.000 mUI
✓	0	1	Lane 0 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3_EQ)	172.500 mUI	64.8%	VALUE <= 490.000 mUI
✓	0	1	Lane 1 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3_EQ)	166.600 mUI	66.0%	VALUE <= 490.000 mUI
✓	0	1	Lane 2 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3_EQ)	177.400 mUI	63.8%	VALUE <= 490.000 mUI
✓	0	1	Lane 3 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3_EQ)	202.600 mUI	58.7%	VALUE <= 490.000 mUI
✗	1	1	Lane 0 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	-87 mdB	-105.4%	VALUE >= 1.600 dB
✗	1	1	Lane 1 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	-3.393 dB	-312.1%	VALUE >= 1.600 dB
✗	1	1	Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	-6.295 dB	-493.4%	VALUE >= 1.600 dB
✓	0	1	Lane 3 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	3.230 dB	101.9%	VALUE >= 1.600 dB
✓	0	1	Lane 0 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0)	1.164	36.9%	VALUE >= 850 m
✓	0	1	Lane 1 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0)	1.160	36.5%	VALUE >= 850 m
✓	0	1	Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0)	957 m	12.6%	VALUE >= 850 m
✓	0	1	Lane 3 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0)	1.439	69.3%	VALUE >= 850 m
✓	0	1	Lane 0 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.9634 dB	28.3%	1.0000 dB <= VALUE <= 4.4000 dB
✓	0	1	Lane 1 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.9420 dB	27.7%	1.0000 dB <= VALUE <= 4.4000 dB
✓	0	1	Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.8821 dB	25.9%	1.0000 dB <= VALUE <= 4.4000 dB
✓	0	1	Lane 3 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	2.0353 dB	30.5%	1.0000 dB <= VALUE <= 4.4000 dB
✓	0	20	Lane 0 - Peak to Peak Voltage Test	1.172 V	15.1%	VALUE <= 1.380 V
✓	0	20	Lane 1 - Peak to Peak Voltage Test	1.180 V	14.5%	VALUE <= 1.380 V
✓	0	20	Lane 2 - Peak to Peak Voltage Test	1.176 V	14.8%	VALUE <= 1.380 V
✓	0	20	Lane 3 - Peak to Peak Voltage Test	1.154 V	16.4%	VALUE <= 1.380 V
✓	0	2	Lane 0 - Eye Diagram Test	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	2	Lane 1 - Eye Diagram Test	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	2	Lane 2 - Eye Diagram Test	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	2	Lane 3 - Eye Diagram Test	0.000	50.0%	-500 m <= VALUE <= 500 m
✓	0	4	Lane 0 - Total Jitter Test (High BitRate)	118.700 mUI	71.7%	VALUE <= 420.000 mUI
✓	0	4	Lane 1 - Total Jitter Test (High BitRate)	114.100 mUI	72.8%	VALUE <= 420.000 mUI
✓	0	4	Lane 2 - Total Jitter Test (High BitRate)	122.700 mUI	70.8%	VALUE <= 420.000 mUI
✓	0	4	Lane 3 - Total Jitter Test (High BitRate)	111.800 mUI	73.4%	VALUE <= 420.000 mUI
✓	0	4	Lane 0 - Non-ISI Jitter Test (High BitRate)	78.2000 mUI	71.7%	VALUE <= 276.0000 mUI
✓	0	4	Lane 1 - Non-ISI Jitter Test (High BitRate)	70.2000 mUI	74.6%	VALUE <= 276.0000 mUI
✓	0	4	Lane 2 - Non-ISI Jitter Test (High BitRate)	69.5000 mUI	74.8%	VALUE <= 276.0000 mUI
✓	0	4	Lane 3 - Non-ISI Jitter Test (High BitRate)	73.3000 mUI	73.4%	VALUE <= 276.0000 mUI
✓	0	2	Lane 0 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.6131 dB	49.7%	100.0 mdB <= VALUE <= 5.1000 dB
✓	0	2	Lane 1 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.5650 dB	49.3%	100.0 mdB <= VALUE <= 5.1000 dB
✓	0	2	Lane 2 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.5002 dB	48.0%	100.0 mdB <= VALUE <= 5.1000 dB
✓	0	2	Lane 3 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.6964 dB	48.1%	100.0 mdB <= VALUE <= 5.1000 dB
✓	0	8	Lane 0 - Pre-Emphasis Level Test (Pre-emphasis 0)	-546 mdB	318.4%	VALUE <= 250 mdB
✓	0	8	Lane 1 - Pre-Emphasis Level Test (Pre-emphasis 0)	-514 mdB	305.6%	VALUE <= 250 mdB
✓	0	8	Lane 2 - Pre-Emphasis Level Test (Pre-emphasis 0)	-641 mdB	356.4%	VALUE <= 250 mdB
✓	0	8	Lane 3 - Pre-Emphasis Level Test (Pre-emphasis 0)	-727 mdB	390.8%	VALUE <= 250 mdB
✓	0	6	Lane 0 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	5.253 dB	162.7%	VALUE >= 2.000 dB
✗	6	6	Lane 1 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	15 mdB	-99.3%	VALUE >= 2.000 dB
✓	0	6	Lane 2 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	3.021 dB	51.1%	VALUE >= 2.000 dB
✗	6	6	Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	-600 µdB	-100.1%	VALUE >= 2.000 dB
✓	0	2	Lane 0 - Non-Transition Voltage Range Measurement (Swing 2)	726 m	2.5%	VALUE >= 708 m
✓	0	2	Lane 1 - Non-Transition Voltage Range Measurement (Swing 2)	1.113	57.2%	VALUE >= 708 m
✓	0	2	Lane 2 - Non-Transition Voltage Range Measurement (Swing 2)	885 m	25.0%	VALUE >= 708 m
✓	0	2	Lane 3 - Non-Transition Voltage Range Measurement (Swing 2)	1.123	58.6%	VALUE >= 708 m
✓	0	2	Lane 0 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	3.0355 dB	43.0%	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	2	Lane 1 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	3.0377 dB	43.0%	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	2	Lane 2 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	2.9466 dB	41.3%	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	2	Lane 3 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	3.1453 dB	45.1%	800.0 mdB <= VALUE <= 6.0000 dB
✗	4	4	Lane 0 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	-2.424 dB	-251.5%	VALUE >= 1.600 dB
✓	0	4	Lane 1 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	3.026 dB	89.1%	VALUE >= 1.600 dB
✓	0	4	Lane 2 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	2.133 dB	33.3%	VALUE >= 1.600 dB
✗	4	4	Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	25 mdB	-98.4%	VALUE >= 1.600 dB
✓	0	2	Lane 0 - Non-Transition Voltage Range Measurement (Swing 1)	818 m	15.5%	VALUE >= 708 m
✓	0	2	Lane 1 - Non-Transition Voltage Range Measurement (Swing 1)	1.118	57.9%	VALUE >= 708 m
✓	0	2	Lane 2 - Non-Transition Voltage Range Measurement (Swing 1)	900 m	27.1%	VALUE >= 708 m
✓	0	2	Lane 3 - Non-Transition Voltage Range Measurement (Swing 1)	1.222	72.6%	VALUE >= 708 m
✓	0	2	Lane 0 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	-235 mdB	-114.7%	VALUE >= 1.600 dB
✗	2	2	Lane 1 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	-3.200 dB	-300.0%	VALUE >= 1.600 dB
✗	2	2	Lane 2 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	-5.641 dB	-452.6%	VALUE >= 1.600 dB
✓	0	2	Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	3.149 dB	96.8%	VALUE >= 1.600 dB
✗	2	2	Lane 0 - Non-Transition Voltage Range Measurement (Swing 0)	814 m	-4.2%	VALUE >= 850 m
✓	0	2	Lane 1 - Non-Transition Voltage Range Measurement (Swing 0)	1.140	34.1%	VALUE >= 850 m

✓	0	2	Lane 2 - Non-Transition Voltage Range Measurement (Swing 0)	945 m	11.2 %	VALUE >= 850 m
✓	0	2	Lane 3 - Non-Transition Voltage Range Measurement (Swing 0)	1.231	44.8 %	VALUE >= 850 m
✓	0	2	Lane 0 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.8316 dB	19.8 %	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	2	Lane 1 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.8212 dB	19.6 %	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	2	Lane 2 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.6330 dB	16.0 %	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	2	Lane 3 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	1.8759 dB	20.7 %	800.0 mdB <= VALUE <= 6.0000 dB
✓	0	4	Lane 0 - Total Jitter Test (Low BitRate)	99.200 mUI	63.3 %	VALUE <= 270.000 mUI
✓	0	4	Lane 1 - Total Jitter Test (Low BitRate)	108.100 mUI	60.0 %	VALUE <= 270.000 mUI
✓	0	4	Lane 2 - Total Jitter Test (Low BitRate)	101.200 mUI	62.5 %	VALUE <= 270.000 mUI
✓	0	4	Lane 3 - Total Jitter Test (Low BitRate)	93.600 mUI	65.3 %	VALUE <= 270.000 mUI
✓	0	4	Lane 0 - Non-ISI Jitter Test (Low BitRate)	80.9000 mUI	61.5 %	VALUE <= 210.0000 mUI
✓	0	4	Lane 1 - Non-ISI Jitter Test (Low BitRate)	80.8000 mUI	61.5 %	VALUE <= 210.0000 mUI
✓	0	4	Lane 2 - Non-ISI Jitter Test (Low BitRate)	76.3000 mUI	63.7 %	VALUE <= 210.0000 mUI
✓	0	4	Lane 3 - Non-ISI Jitter Test (Low BitRate)	76.9000 mUI	63.4 %	VALUE <= 210.0000 mUI



### Report Detail

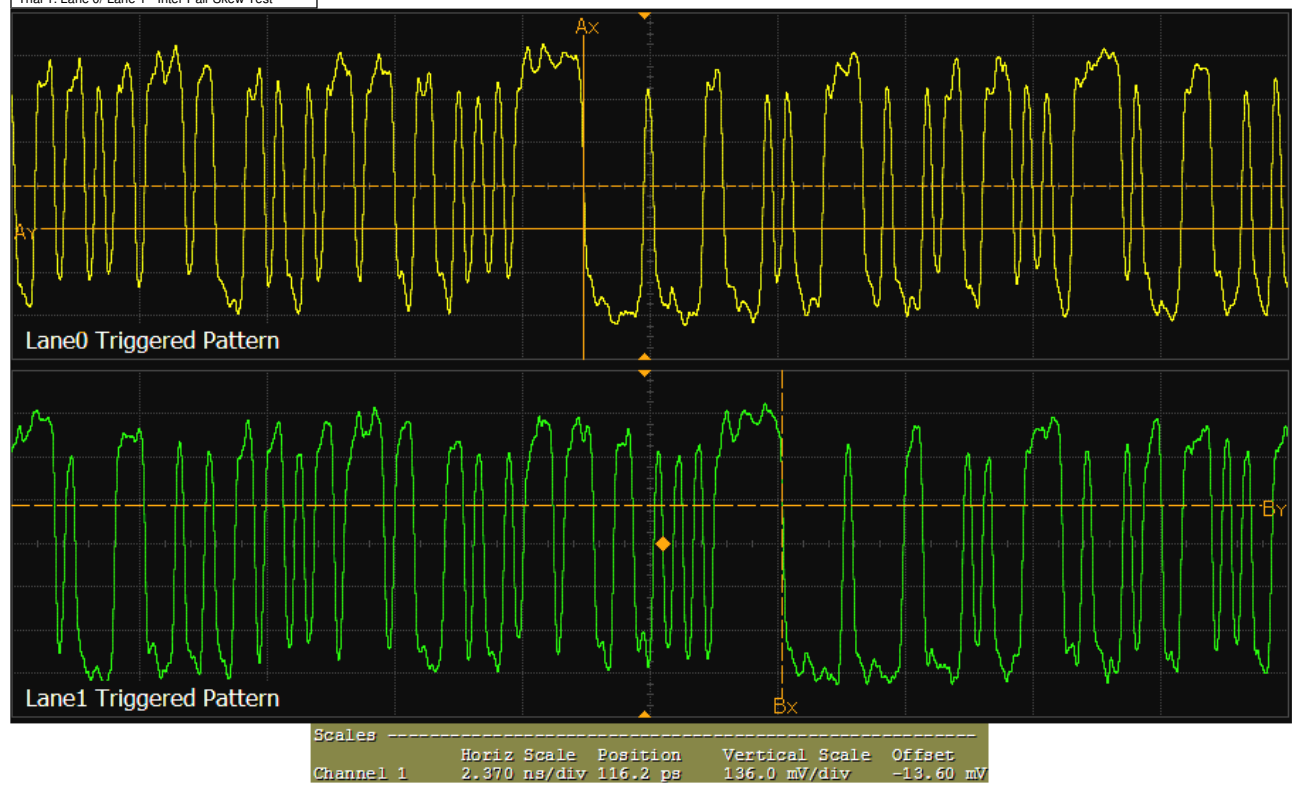
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#### ✓ Lane 0/ Lane 1 - Inter Pair Skew Test Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.  
Pass Limits: [13.3000 UI to 26.7000 UI] Lane 0/ Lane 1 - Inter Pair Skew Test 20.0117 UI

**Result Details**  
Lane 0/ Lane 1 - Inter Pair Skew Test (See image) Inter-Pair Skew Edges 100 VTop 288.900 mV VBase -391.100 mV VSwing 680.000 mV Test Mode Compliance  
Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2  
PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1  
Trial 1: Lane 0/ Lane 1 - Inter Pair Skew Test



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#### ✓ Lane 0/ Lane 2 - Inter Pair Skew Test Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.  
Pass Limits: [33.3000 UI to 46.7000 UI] Lane 0/ Lane 2 - Inter Pair Skew Test 39.8551 UI

**Result Details**  
Lane 0/ Lane 2 - Inter Pair Skew Test (See image) Inter-Pair Skew Edges 100 VTop 288.900 mV VBase -391.100 mV VSwing 680.000 mV Test Mode Compliance  
Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2  
PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0



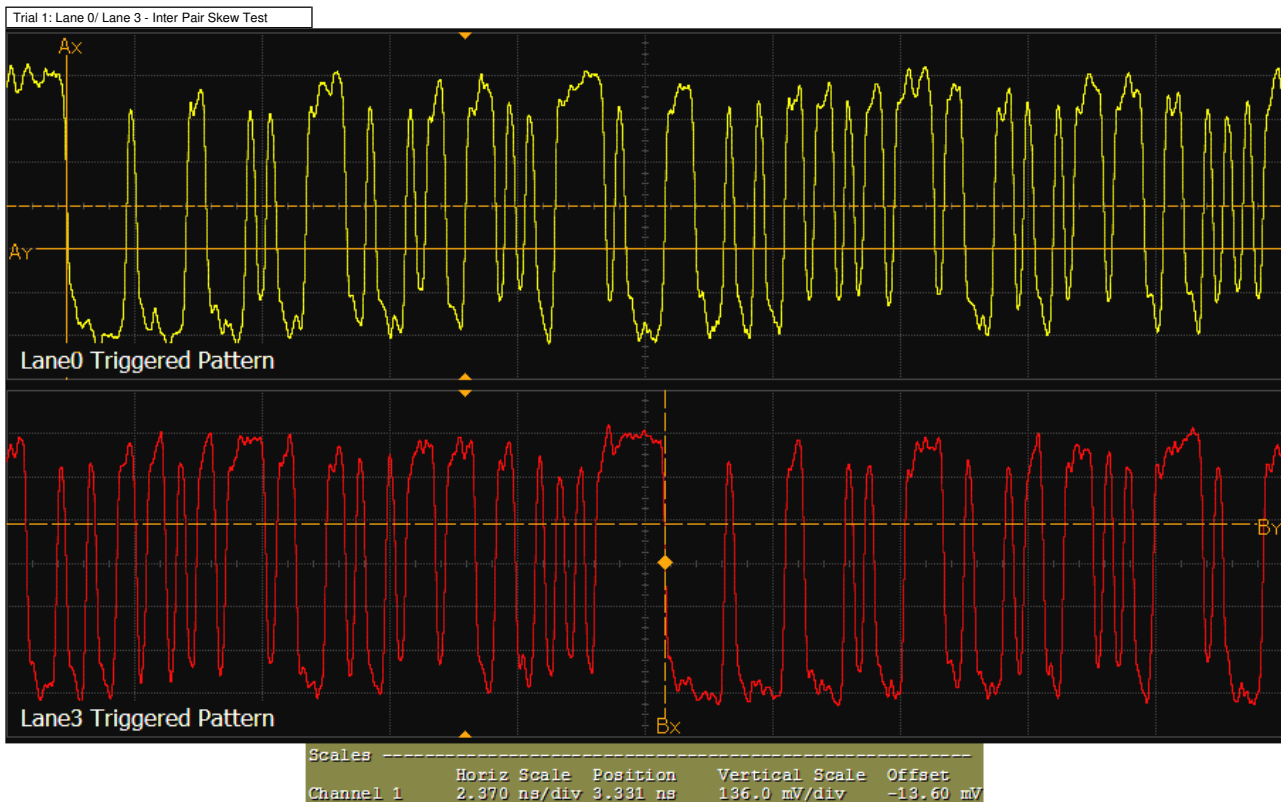
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#### ✓ Lane 0/ Lane 3 - Inter Pair Skew Test Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.  
Pass Limits: [53.3000 UI to 66.7000 UI] Lane 0/ Lane 3 - Inter Pair Skew Test 59.9906 UI

**Result Details**  
Lane 0/ Lane 3 - Inter Pair Skew Test (See image) Inter-Pair Skew Edges 100 VTop 288.900 mV VBase -391.100 mV VSwing 680.000 mV Test Mode Compliance  
Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2  
PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1



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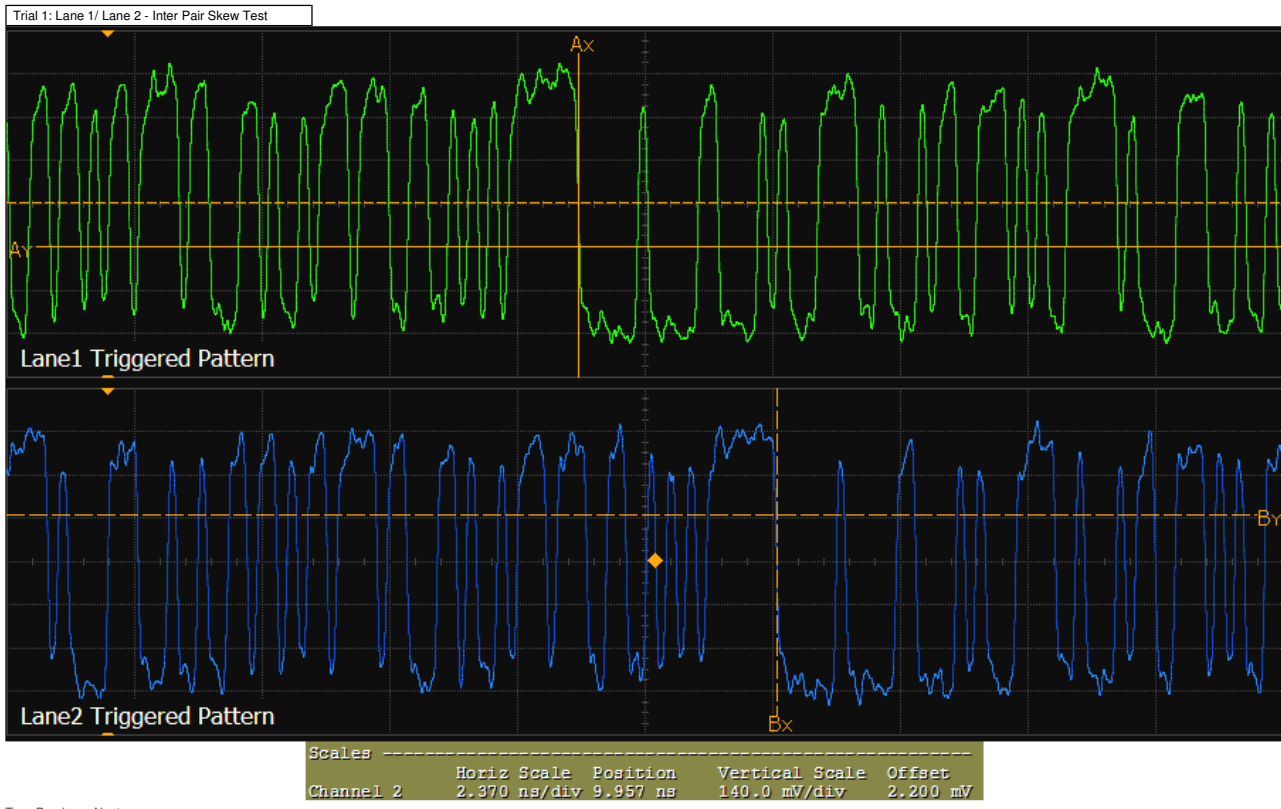
✓ Lane 1/ Lane 2 - Inter Pair Skew Test Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.  
 Pass Limits: [13.3000 UI to 26.7000 UI] Lane 1/ Lane 2 - Inter Pair Skew Test 19.8471 UI

Result Details

Lane 1/ Lane 2 - Inter Pair Skew Test (See image) Inter-Pair Skew Edges 100 VTop 360.410 mV VBase -396.370 mV VSwing 756.780 mV Test Mode Compliance  
 Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2  
 PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1



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✓ Lane 1/ Lane 3 - Inter Pair Skew Test Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.

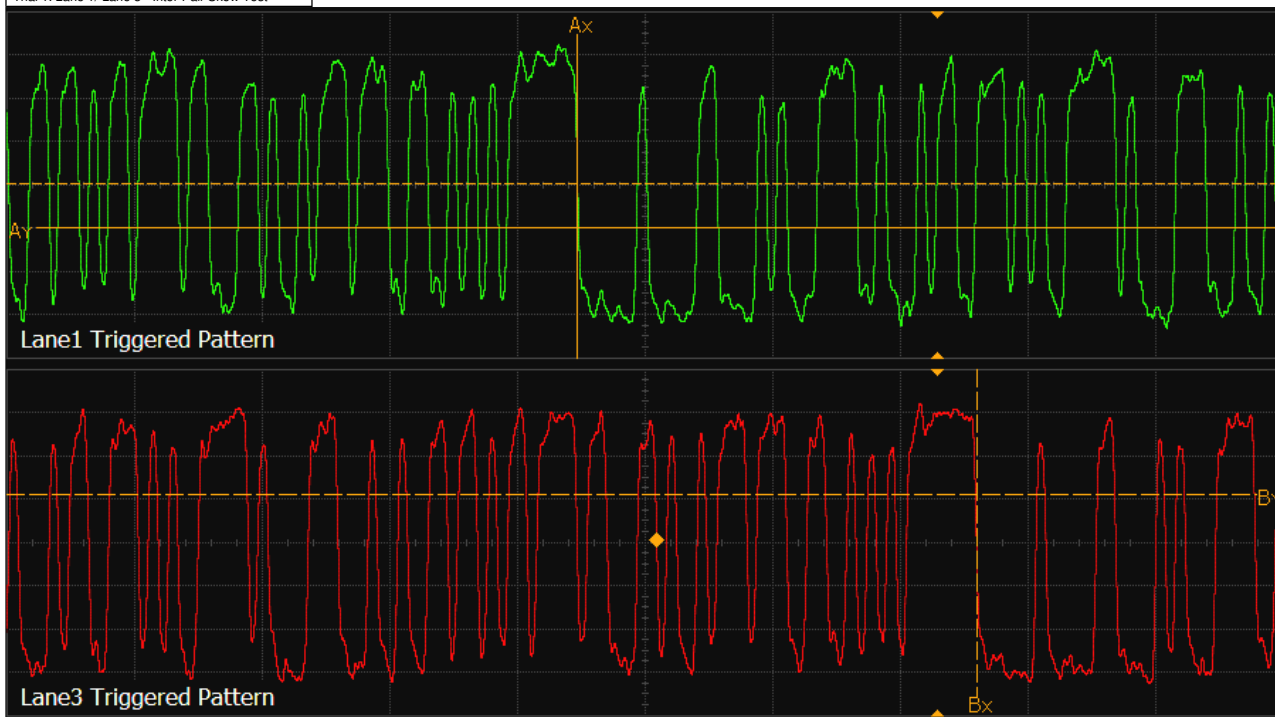
Pass Limits: [33.3000 UI to 46.7000 UI] Lane 1/ Lane 3 - Inter Pair Skew Test 39.9957 UI

Result Details

Lane 1/ Lane 3 - Inter Pair Skew Test (See image) Inter-Pair Skew Edges 100 VTop 360.410 mV VBase -396.370 mV VSwing 756.780 mV Test Mode Compliance
Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1

Trial 1: Lane 1/ Lane 3 - Inter Pair Skew Test



Scales table with columns: Channel, Horiz Scale, Position, Vertical Scale, Offset. Values: Channel 2, 2.370 ns/div, -5.413 ns, 140.0 mV/div, 2.200 mV.

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Lane 2/ Lane 3 - Inter Pair Skew Test

Reference: DisplayPort CTS Sec. 3.4; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.

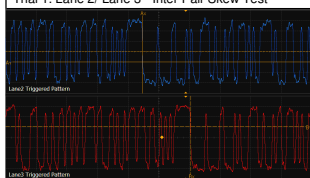
Pass Limits: [13.3000 UI to 26.7000 UI] Lane 2/ Lane 3 - Inter Pair Skew Test 20.1414 UI

Result Details

Lane 2/ Lane 3 - Inter Pair Skew Test (See image) Inter-Pair Skew Edges 100 VTop 363.460 mV VBase -365.170 mV VSwing 728.630 mV Test Mode Compliance
Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1

Trial 1: Lane 2/ Lane 3 - Inter Pair Skew Test



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Lane 0 - D10.2 Total Jitter Test (TP3\_EQ)

Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 400.000 mUI D10.2 Total Jitter Test (TP3\_EQ) 108.700 mUI

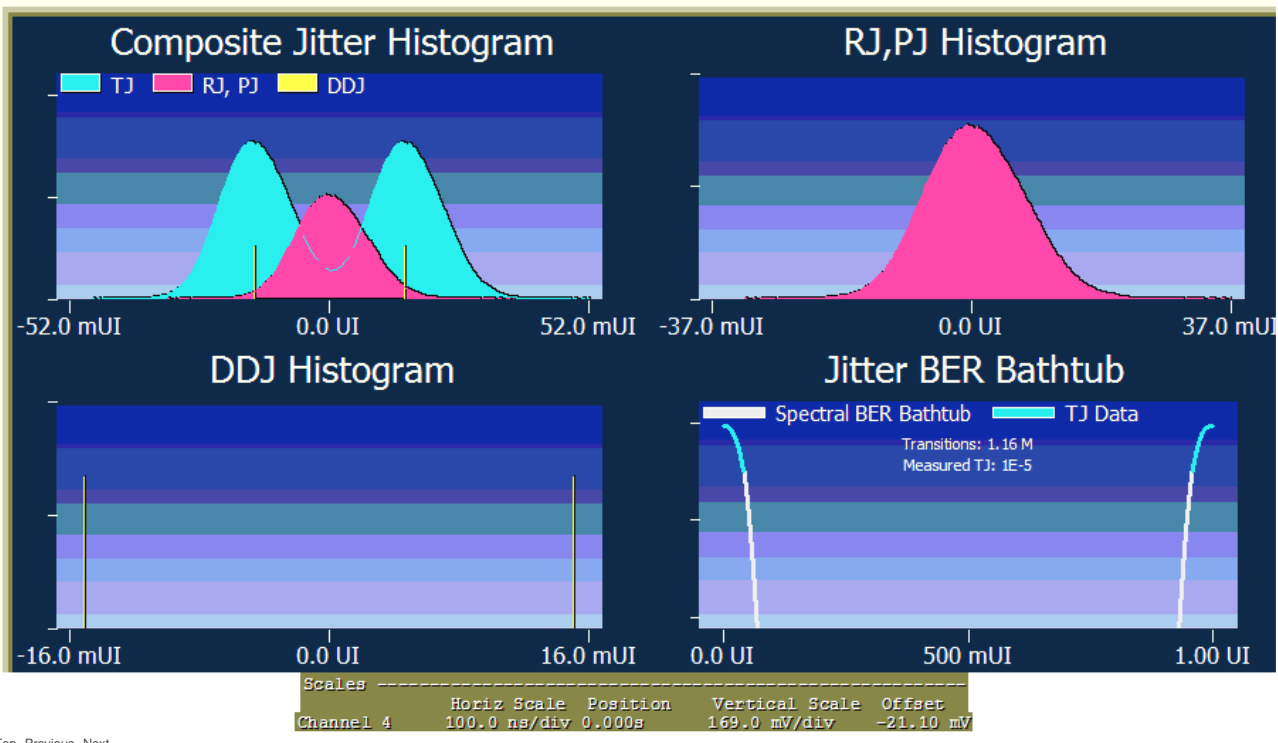
Result Details

Jitter Separation Image (See image) Edges 1.0000000 M Total Jitter (TJ) 108.7 mUI Total Jitter (TJ) in ps 20.1298 ps Periodic Jitter (PJ rms) 4.5 mUI Periodic Jitter (PJ p-p) 15.3 mUI
Deterministic Jitter (DJ) 43.8 mUI Random Jitter (RJ) 5.3 mUI ISI Jitter (ISI) 0.0000 UI Data Dependent Jitter (DDJ) 30.3 mUI Bit Error Rate (BER) E9 Test Mode Compliance
Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1

Trial 1: Jitter Separation Image

Jitter



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✓ Lane 1 - D10.2 Total Jitter Test (TP3\_EQ) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 400.000 mUI D10.2 Total Jitter Test (TP3\_EQ) 95.500 mUI

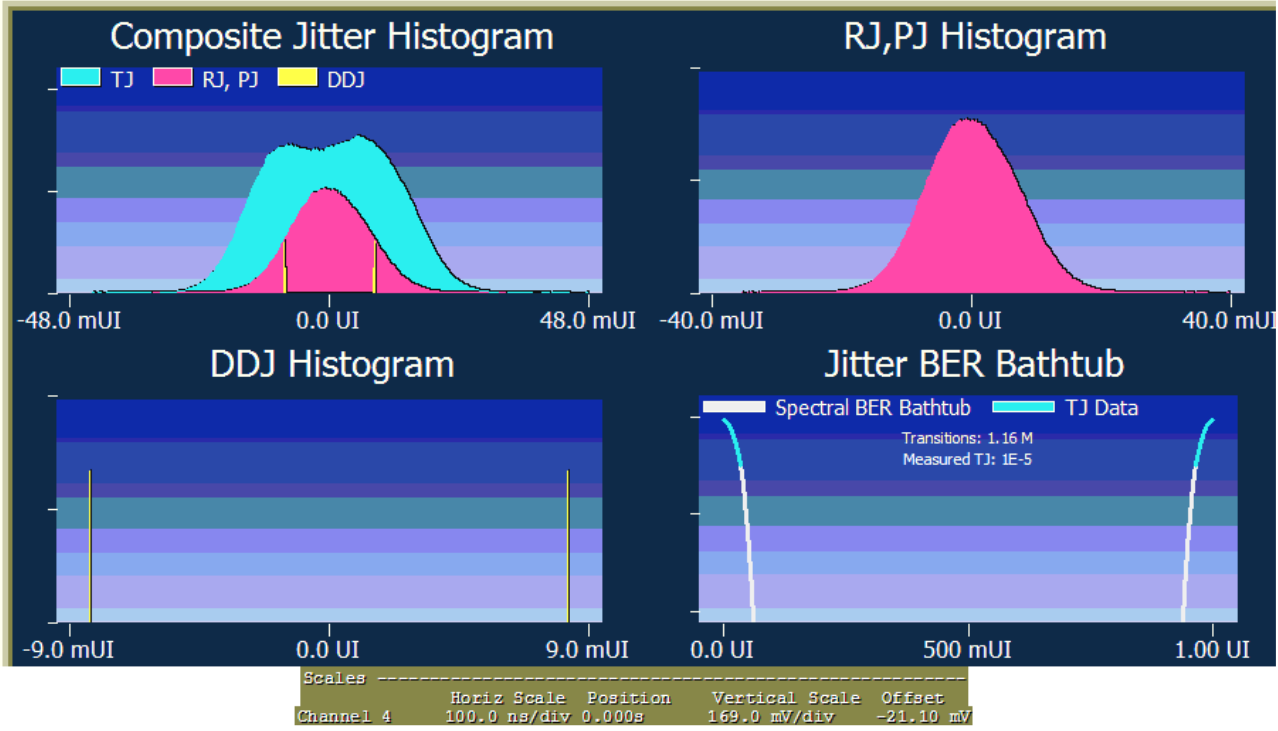
**Result Details**

Jitter Separation Image (See image)	Edges 1.00000000 M	Total Jitter (TJ) 95.5 mUI	Total Jitter (TJ) in ps 17.6852 ps	Periodic Jitter (PJ rms) 4.5 mUI	Periodic Jitter (PJ p-p) 17.4 mUI
Deterministic Jitter (DJ) 32.2 mUI	Random Jitter (RJ) 5.2 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 16.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image

Jitter



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✓ Lane 2 - D10.2 Total Jitter Test (TP3\_EQ)

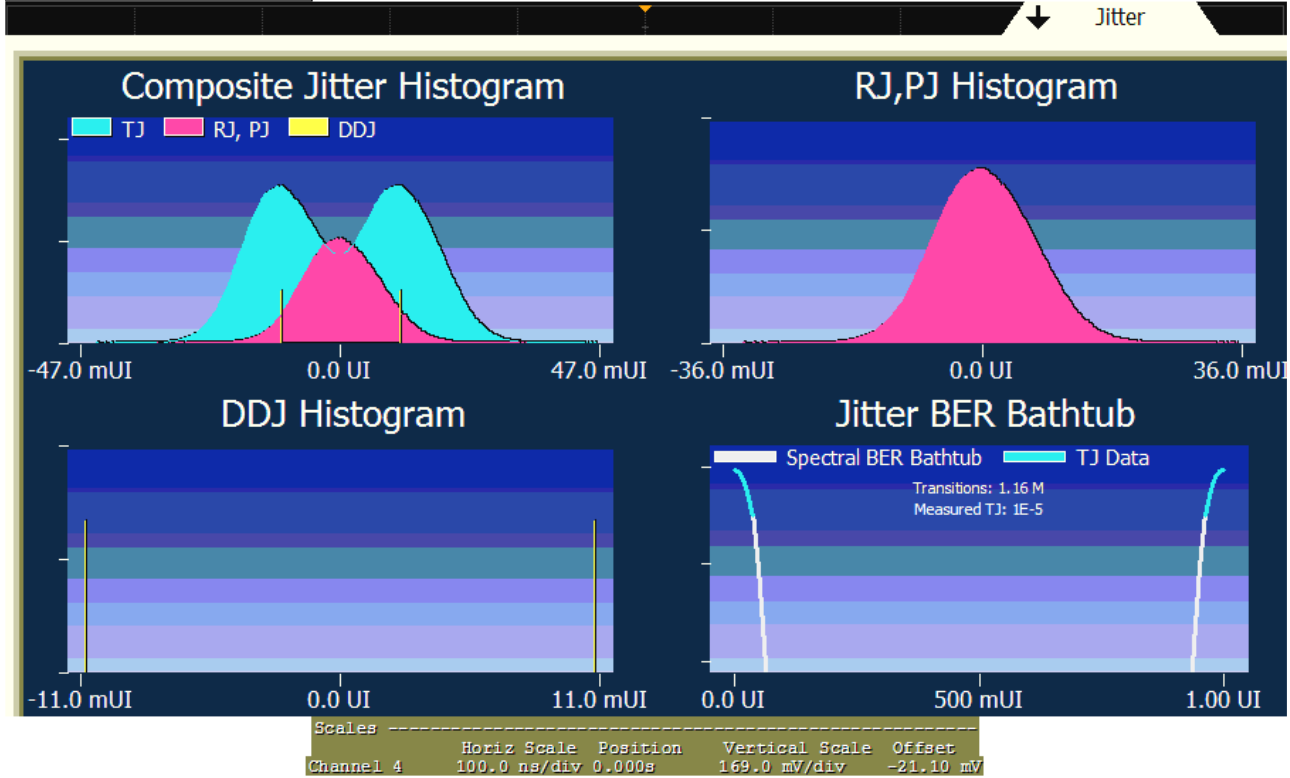
Test Summary: Pass Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 400.000 mUI Lane 2 D10.2 Total Jitter Test (TP3\_EQ) 100.000 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.00000000 M	Total Jitter (TJ) 100.0 mUI	Total Jitter (TJ) in ps 18.5185 ps	Periodic Jitter (PJ rms) 4.3 mUI	Periodic Jitter (PJ p-p) 16.4 mUI
Deterministic Jitter (DJ) 36.3 mUI	Random Jitter (RJ) 5.2 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 21.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 3 - D10.2 Total Jitter Test (TP3\_EQ)

Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

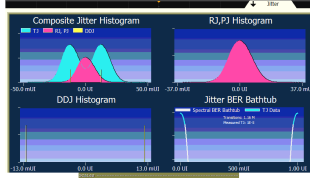
Test Summary: Pass Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 400.000 mUI D10.2 Total Jitter Test (TP3\_EQ) 102.600 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.00000000 M	Total Jitter (TJ) 102.6 mUI	Total Jitter (TJ) in ps 19.0001 ps	Periodic Jitter (PJ rms) 4.1 mUI	Periodic Jitter (PJ p-p) 14.7 mUI
Deterministic Jitter (DJ) 37.8 mUI	Random Jitter (RJ) 5.3 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 24.9 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 0 - D10.2 Deterministic Jitter (TP3\_EQ)

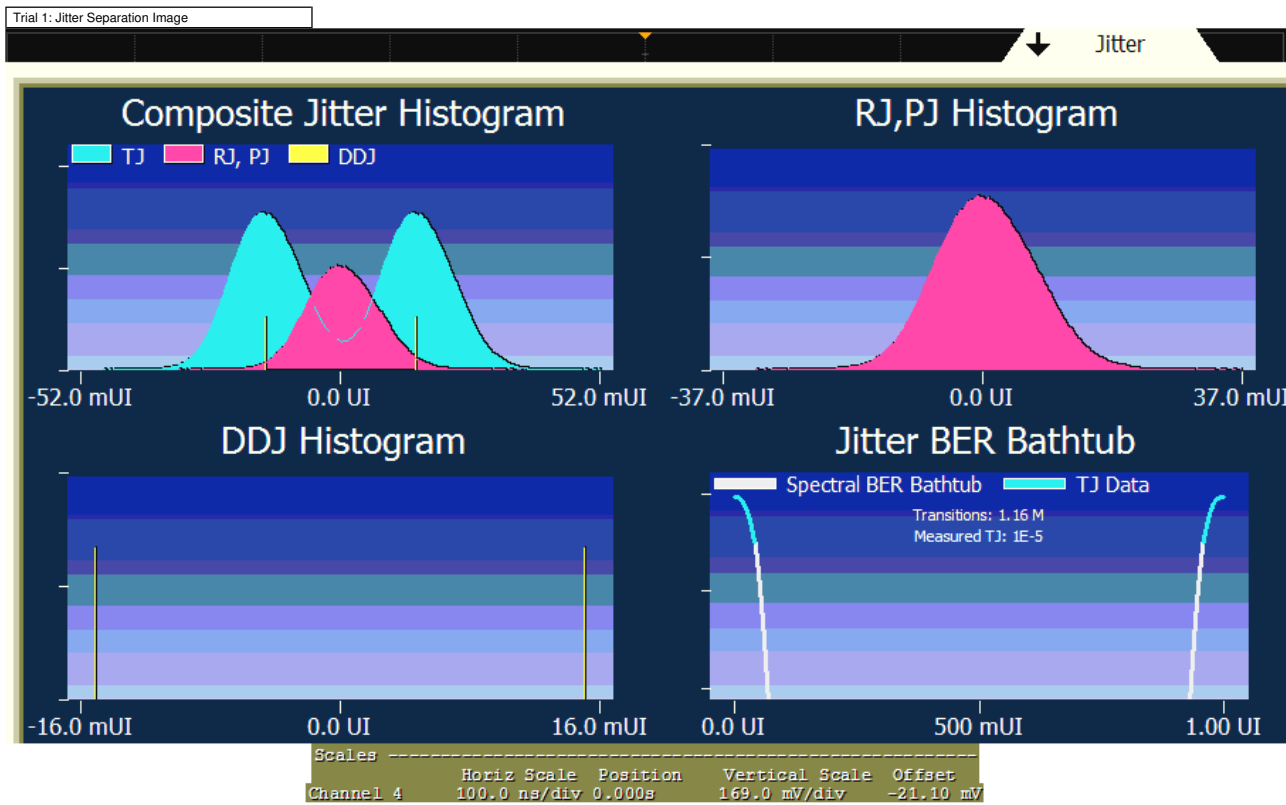
Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 250.000 mUI D10.2 Deterministic Jitter (TP3\_EQ) 43.800 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.000000000 M	Total Jitter (TJ) 108.7 mUI	Total Jitter (TJ) in ps 20.1298 ps	Periodic Jitter (PJ rms) 4.5 mUI	Periodic Jitter (PJ p-p) 15.3 mUI
Deterministic Jitter (DJ) 43.8 mUI	Random Jitter (RJ) 5.3 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 30.3 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1



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✓ Lane 1 - D10.2 Deterministic Jitter (TP3\_EQ) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

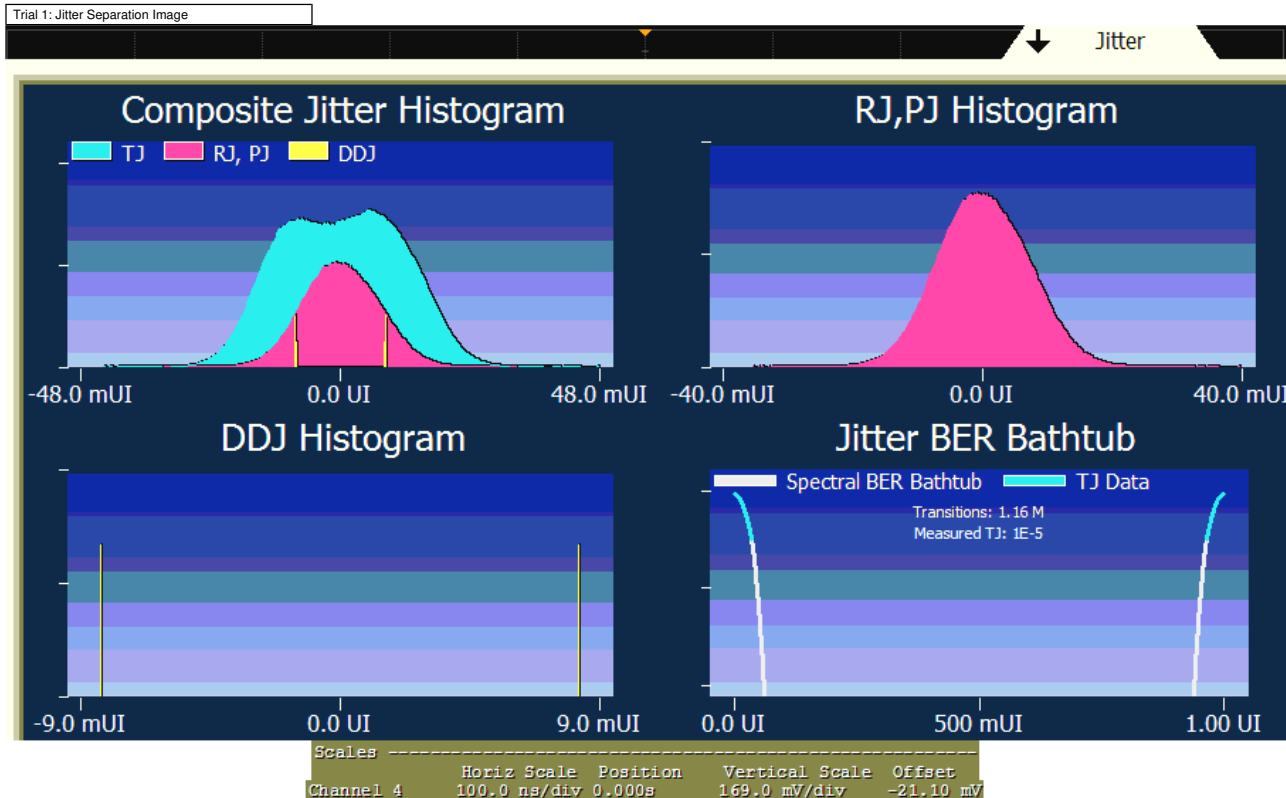
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 250.000 mUI **D10.2 Deterministic Jitter (TP3\_EQ)** 32.200 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 95.5 mUI	Total Jitter (TJ) in ps 17.6852 ps	Periodic Jitter (PJ rms) 4.5 mUI	Periodic Jitter (PJ p-p) 17.4 mUI
Deterministic Jitter (DJ) 32.2 mUI	Random Jitter (RJ) 5.2 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 16.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

**Trial 1**



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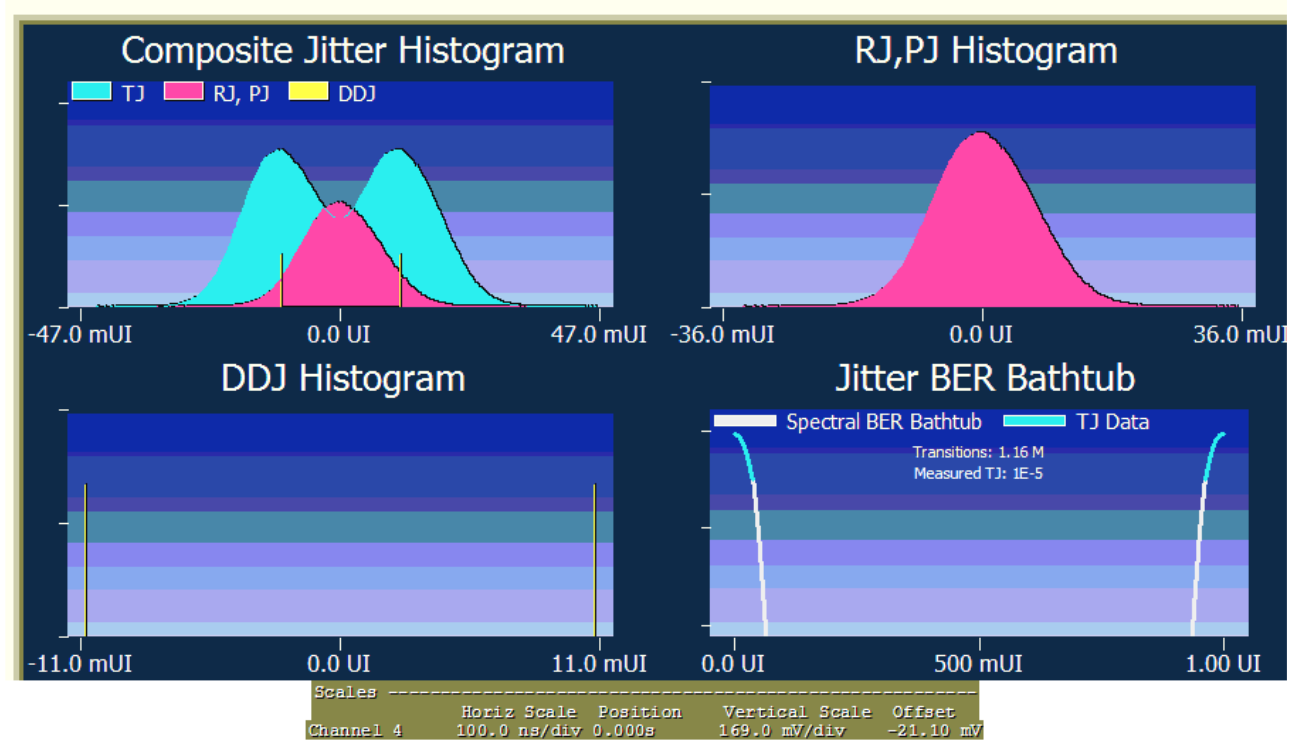
✓ Lane 2 - D10.2 Deterministic Jitter (TP3\_EQ)

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 250.000 mUI Lane 2 D10.2 Deterministic Jitter (TP3\_EQ) 36.300 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 100.0 mUI	Total Jitter (TJ) in ps 18.5185 ps	Periodic Jitter (PJ rms) 4.3 mUI	Periodic Jitter (PJ p-p) 16.4 mUI
Deterministic Jitter (DJ) 36.3 mUI	Random Jitter (RJ) 5.2 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 21.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2

Trial 1  
 Trial 1: Jitter Separation Image



✓ Lane 3 - D10.2 Deterministic Jitter (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 250.000 mUI D10.2 Deterministic Jitter (TP3\_EQ) 37.800 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 102.6 mUI	Total Jitter (TJ) in ps 19.0001 ps	Periodic Jitter (PJ rms) 4.1 mUI	Periodic Jitter (PJ p-p) 14.7 mUI
Deterministic Jitter (DJ) 37.8 mUI	Random Jitter (RJ) 5.3 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 24.9 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2



✓ Lane 0 - D10.2 Random Jitter (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

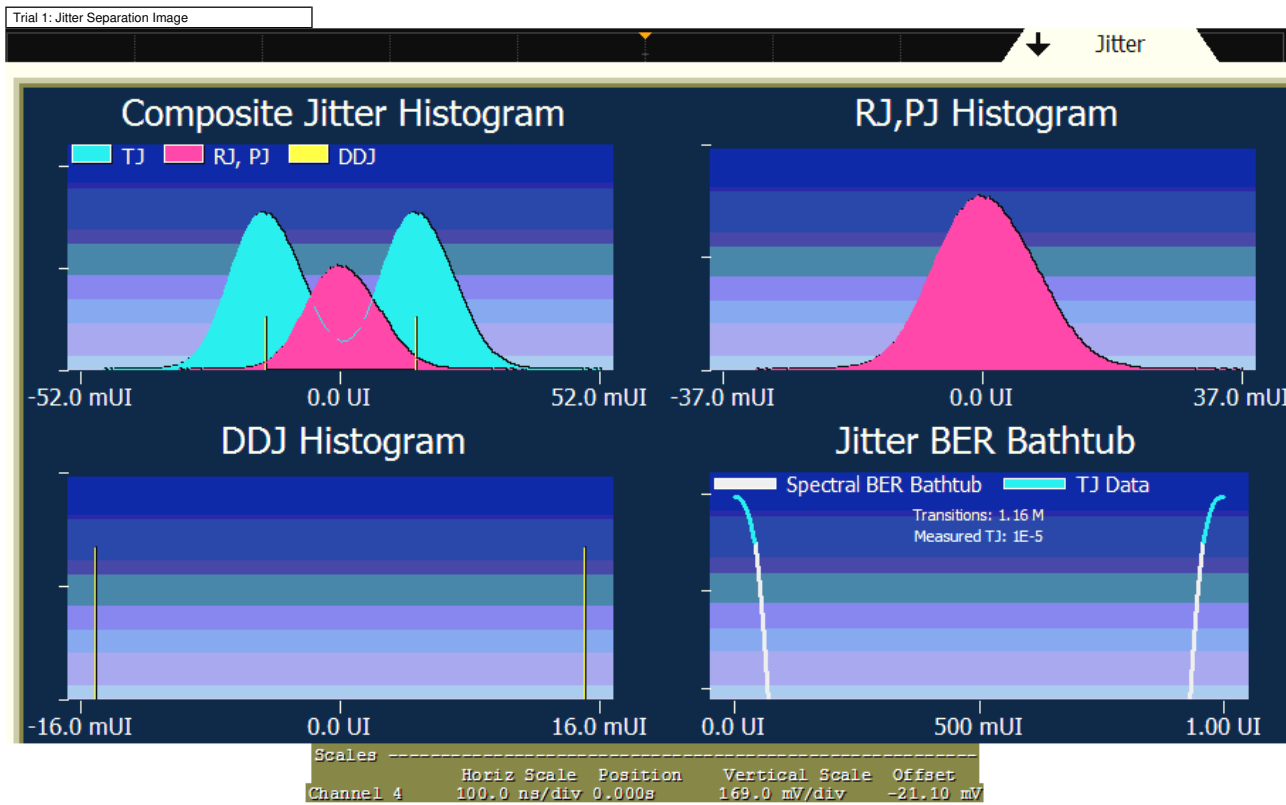
Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 230.000 mUI D10.2 Random Jitter (TP3\_EQ) 5.300 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 108.7 mUI	Total Jitter (TJ) in ps 20.1298 ps	Periodic Jitter (PJ rms) 4.5 mUI	Periodic Jitter (PJ p-p) 15.3 mUI
Deterministic Jitter (DJ) 43.8 mUI	Random Jitter (RJ) 5.3 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 30.3 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2

Trial 1





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✓ Lane 1 - D10.2 Random Jitter (TP3\_EQ) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

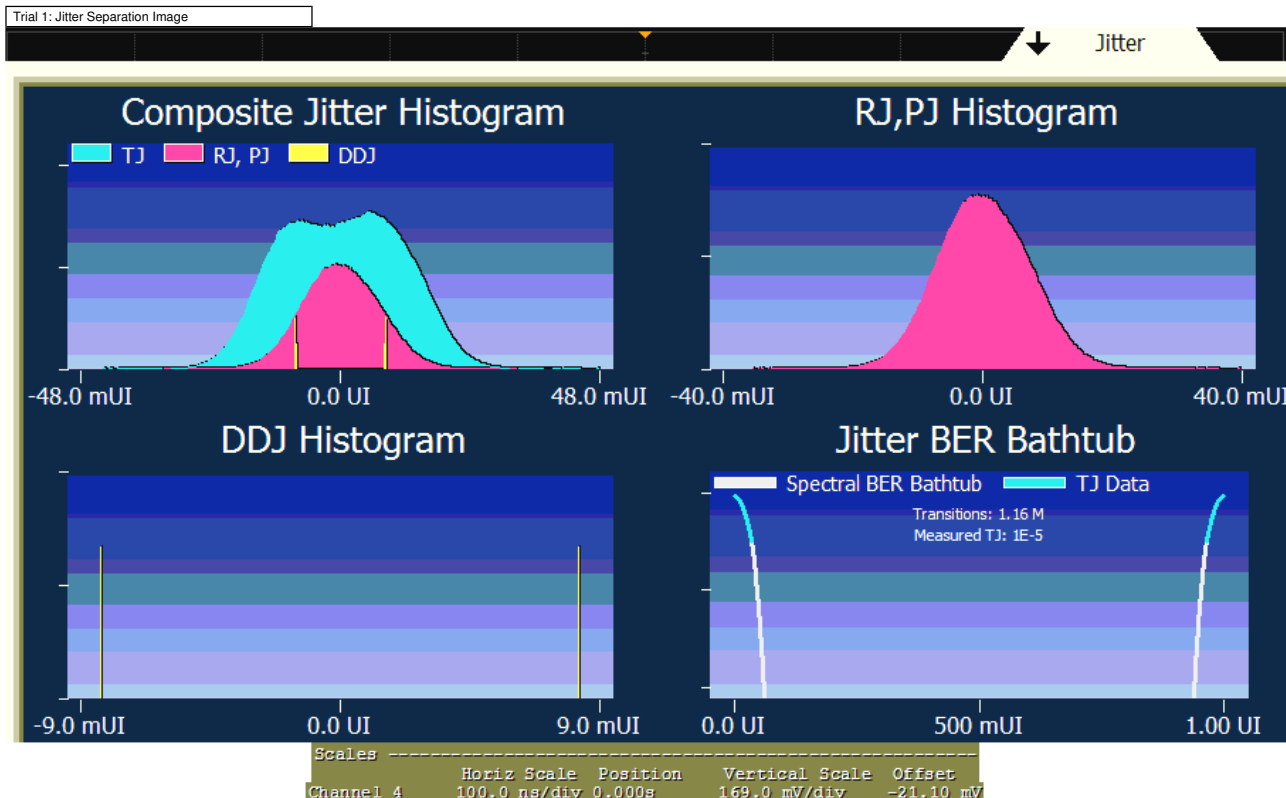
Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 230.000 mUI D10.2 Random Jitter (TP3\_EQ) 5.200 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 95.5 mUI	Total Jitter (TJ) in ps 17.6852 ps	Periodic Jitter (PJ rms) 4.5 mUI	Periodic Jitter (PJ p-p) 17.4 mUI
Deterministic Jitter (DJ) 32.2 mUI	Random Jitter (RJ) 5.2 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 16.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1



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✓ Lane 2 - D10.2 Random Jitter (TP3\_EQ)

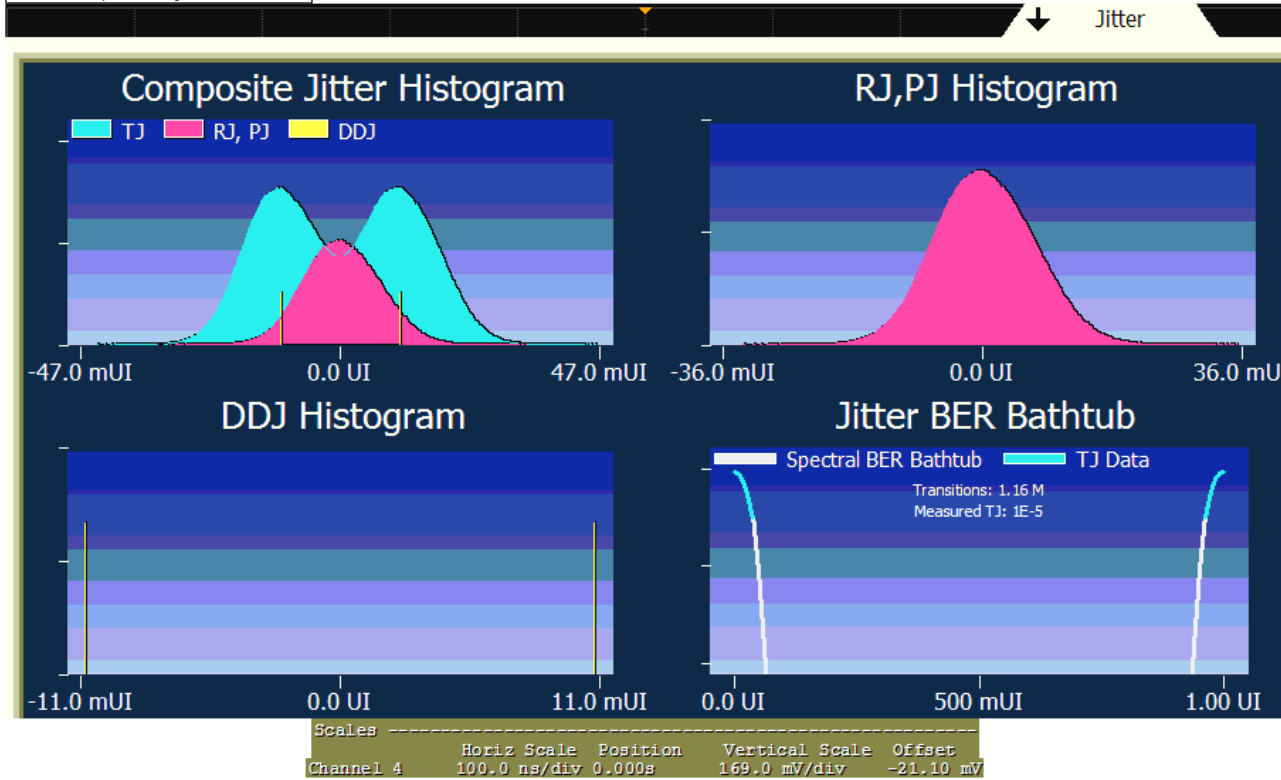
Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 230.000 mUI Lane 2 D10.2 Random Jitter (TP3\_EQ) 5.200 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 100.0 mUI	Total Jitter (TJ) in ps 18.5185 ps	Periodic Jitter (PJ rms) 4.3 mUI	Periodic Jitter (PJ p-p) 16.4 mUI
Deterministic Jitter (DJ) 36.3 mUI	Random Jitter (RJ) 5.2 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 21.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 3 - D10.2 Random Jitter (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 230.000 mUI D10.2 Random Jitter (TP3\_EQ) 5.300 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 102.6 mUI	Total Jitter (TJ) in ps 19.0001 ps	Periodic Jitter (PJ rms) 4.1 mUI	Periodic Jitter (PJ p-p) 14.7 mUI
Deterministic Jitter (DJ) 37.8 mUI	Random Jitter (RJ) 5.3 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 24.9 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2

Trial 1

Trial 1: Jitter Separation Image



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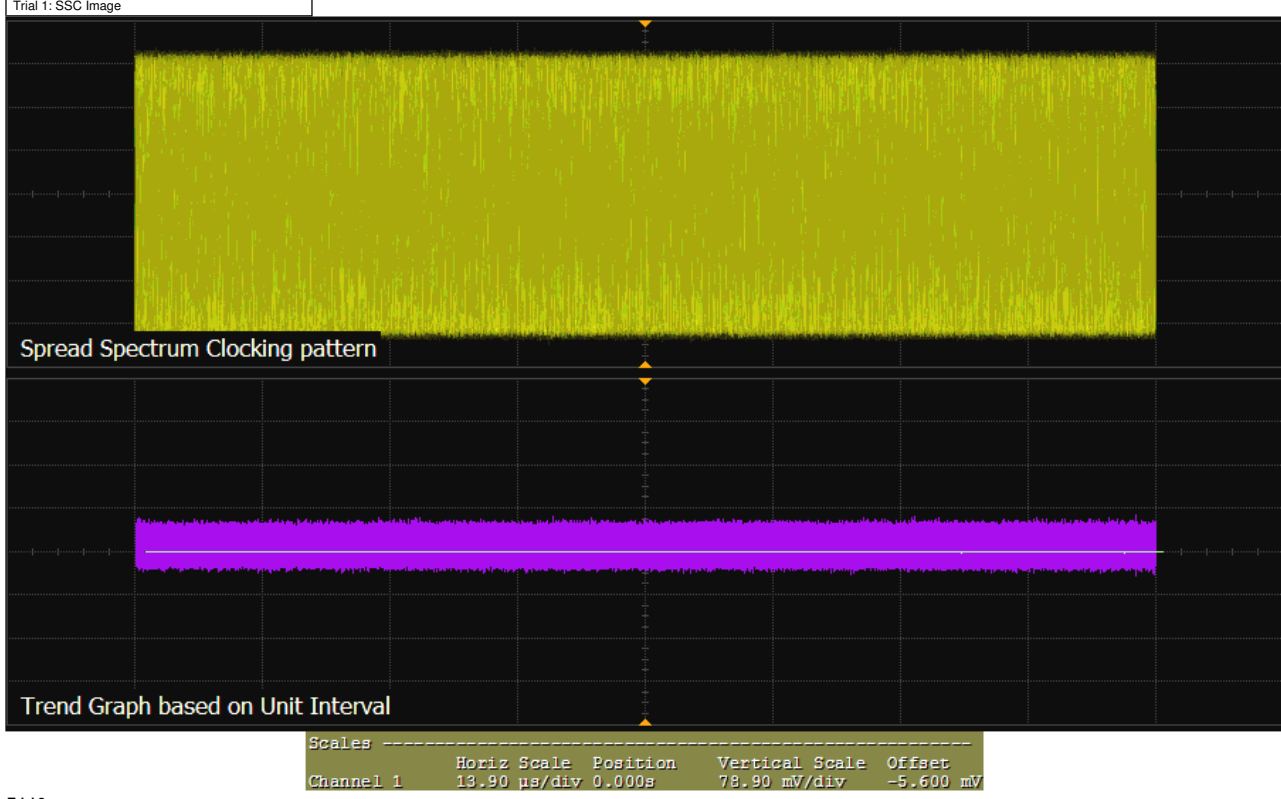
✓ Lane 0 - Main Link Frequency Compliance Reference: DisplayPort CTS Sec. 3.14

Test Summary: Pass Test Description: To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.  
 Pass Limits: [-5.300000 kppm to 300.000 kppm] Lane 0 - Main Link Frequency (Worst of 3 Trials) 5.457 ppm # Trials Run: 3 Worst Trial: Trial 3

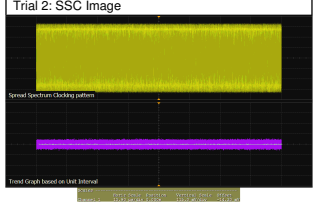
Overall Summary + details of 3 worst trials

Pass	Trial	Actual Value	Margin	SSC Image	Unit Interval (Mean)	Data Rate (Mean)	Data Rate (Max)	Data Rate (Min)	Upper limit Data Rate	Lower limit Data Rate	SSC Acquisitions	VTop	VBase	VSwing	Test Mode	Test Layer	Test Condition	Pass
	Avg	2.837 ppm	5.306 %															
	StdDev	3.768 ppm	67.29 m%															
	Range	6.938 ppm	123.9 m%															
	Min	-1.481 ppm	5.260 %															
	Max	5.457 ppm	5.384 %															
	Sum	8.512 ppm	15.92 %															
✓	Trial 1	-1.481 ppm	5.4%	(See image)	185.1855 ps	5.399992000000 Gbps	5.4004370038915 Gbps	5.3995359648065 Gbps	5.4016200000000 Gbps	5.3713800000000 Gbps	10	259.570 mV	268.380 mV	527.950 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S
✓	Trial 2	4.537 ppm	5.3%	(See image)	370.3687 ps	2.7000122500000 Gbps	2.7003862104967 Gbps	2.6996557401802 Gbps	2.7008100000000 Gbps	2.6856900000000 Gbps	10	305.310 mV	317.440 mV	622.750 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S
✓	Trial 3 (Worst)	5.457 ppm	5.3%	(See image)	617.2806 ps	1.6200088400000 Gbps	1.6203098726034 Gbps	1.6197073035935 Gbps	1.6204860000000 Gbps	1.6114140000000 Gbps	10	368.150 mV	400.000 mV	768.150 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S

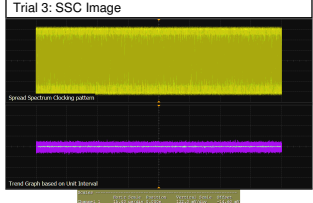
Trial 1



Trial 2



Trial 3



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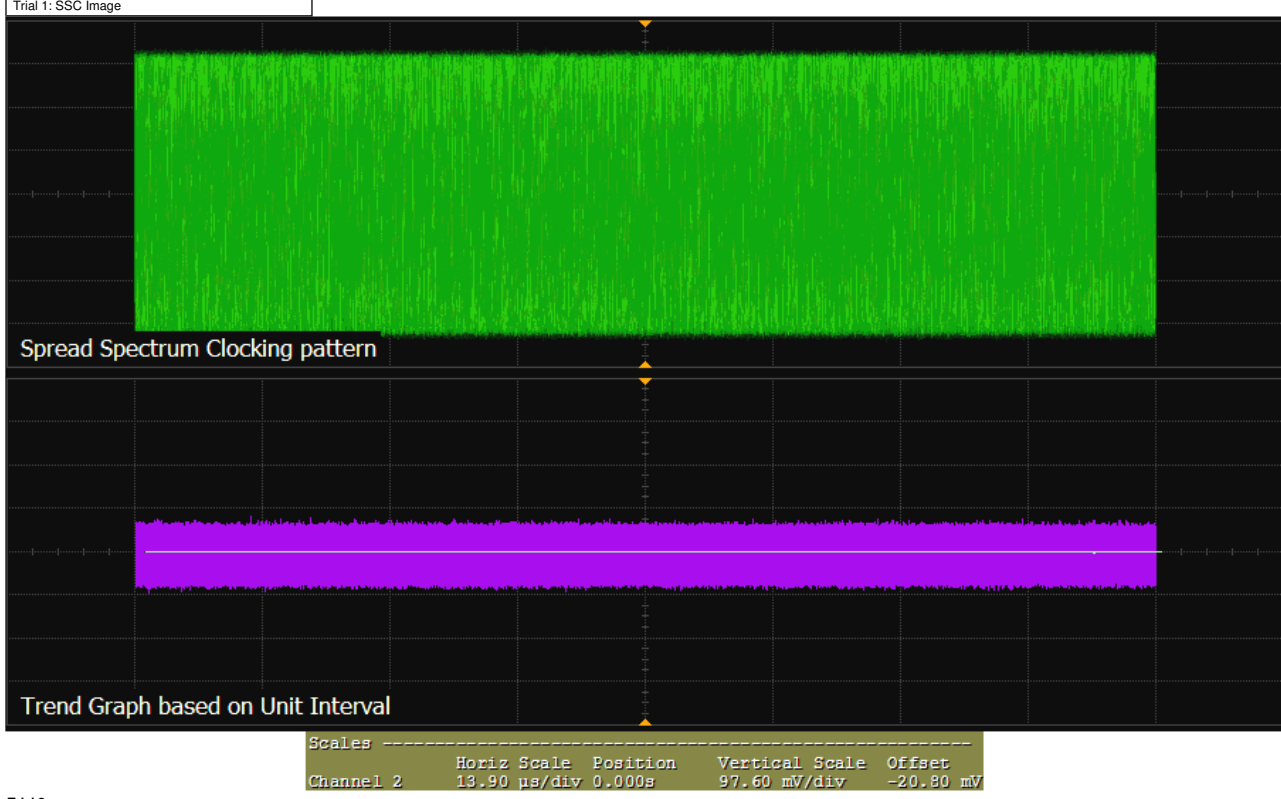
✓ Lane 1 - Main Link Frequency Compliance Reference: DisplayPort CTS Sec. 3.14

Test Summary: Pass Test Description: To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.  
 Pass Limits: [-5.300000 kppm to 300.000 ppm] Lane 1 - Main Link Frequency (Worst of 3 Trials) -2.778 ppm # Trials Run: 3 Worst Trial: Trial 3

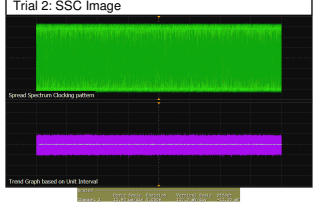
Overall Summary + details of 3 worst trials

Pass	Trial	Actual Value	Margin	SSC Image	Unit Interval (Mean)	Data Rate (Mean)	Data Rate (Max)	Data Rate (Min)	Upper limit Data Rate	Lower limit Data Rate	SSC Acquisitions	VTop	VBase	VSwing	Test Mode	Test Layer	Test Condition	I	T
	Avg	-9.676 ppm	5.530 %																
	StdDev	6.099 ppm	108.9 m%																
	Range	11.57 ppm	206.7 m%																
	Min	-14.35 ppm	5.407 %																
	Max	-2.778 ppm	5.613 %																
	Sum	-29.03 ppm	16.59 %																
✓	Trial 1	14.352 ppm	5.6%	(See image)	185.1878 ps	5.3999225000000 Gbps	5.4004720022610 Gbps	5.3995359644287 Gbps	5.4016200000000 Gbps	5.3713800000000 Gbps	10	310.720 mV	356.540 mV	667.260 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S	
✓	Trial 2	11.898 ppm	5.6%	(See image)	370.3748 ps	2.6999678750000 Gbps	2.7003803761382 Gbps	2.6996331480678 Gbps	2.7008100000000 Gbps	2.6856900000000 Gbps	10	326.910 mV	365.990 mV	692.900 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S	
✓	Trial 3 (Worst)	-2.778 ppm	5.4%	(See image)	617.2857 ps	1.6199955000000 Gbps	1.6203177482030 Gbps	1.6197125502837 Gbps	1.6204860000000 Gbps	1.6114140000000 Gbps	10	367.150 mV	392.800 mV	759.950 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S	

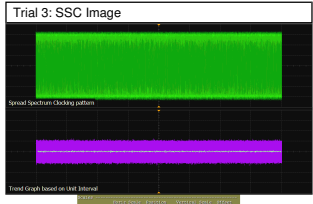
Trial 1



Trial 2



Trial 3



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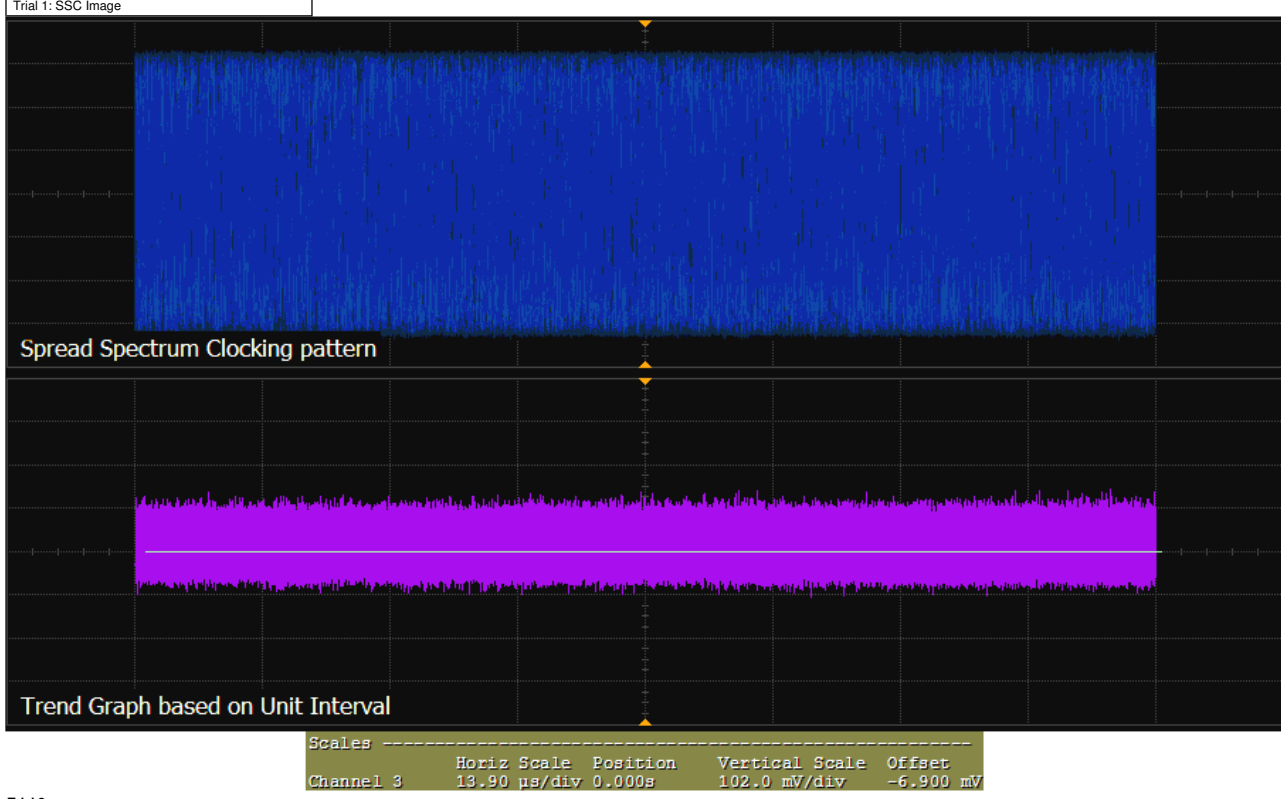
✓ Lane 2 - Main Link Frequency Compliance Reference: DisplayPort CTS Sec. 3.14

Test Summary: Pass Test Description: To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.  
 Pass Limits: [-5.300000 kppm to 300.000 kppm] Lane 2 - Main Link Frequency (Worst of 3 Trials) 5.861 ppm # Trials Run: 3 Worst Trial: Trial 2

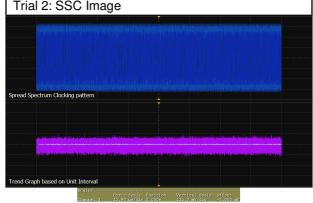
Overall Summary + details of 3 worst trials

Pass	Trial	Actual Value	Margin	SSC Image	Unit Interval (Mean)	Data Rate (Mean)	Data Rate (Max)	Data Rate (Min)	Upper limit Data Rate	Lower limit Data Rate	SSC Acquisitions	VTop	VBase	VSwing	Test Mode	Test Layer	Test Condition	I	T
	Avg	5.026 ppm	5.267 %																
	StdDev	1.087 ppm	19.42 m%																
	Range	2.065 ppm	36.88 m%																
	Min	3.796 ppm	5.252 %																
	Max	5.861 ppm	5.289 %																
	Sum	15.08 ppm	15.80 %																
✓	Trial 1	3.796 ppm	5.3%	(See image)	185.1845 ps	5.4000205000000 Gbps	5.4004865853297 Gbps	5.3995534573463 Gbps	5.4016200000000 Gbps	5.3713800000000 Gbps	10	346.790 mV	358.590 mV	705.380 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S	
✓	Trial 2 (Worst)	5.861 ppm	5.3%	(See image)	370.3682 ps	2.7000158250000 Gbps	2.7003694384251 Gbps	2.6996637572815 Gbps	2.7008100000000 Gbps	2.6856900000000 Gbps	10	321.720 mV	344.080 mV	665.800 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S	
✓	Trial 3	5.420 ppm	5.3%	(See image)	617.2806 ps	1.6200087800000 Gbps	1.6202886065934 Gbps	1.6197143862308 Gbps	1.6204860000000 Gbps	1.6114140000000 Gbps	10	370.750 mV	393.300 mV	764.050 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	S	

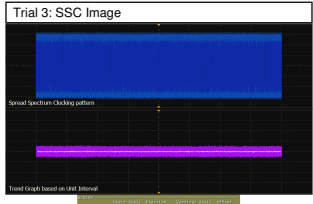
Trial 1



Trial 2



Trial 3



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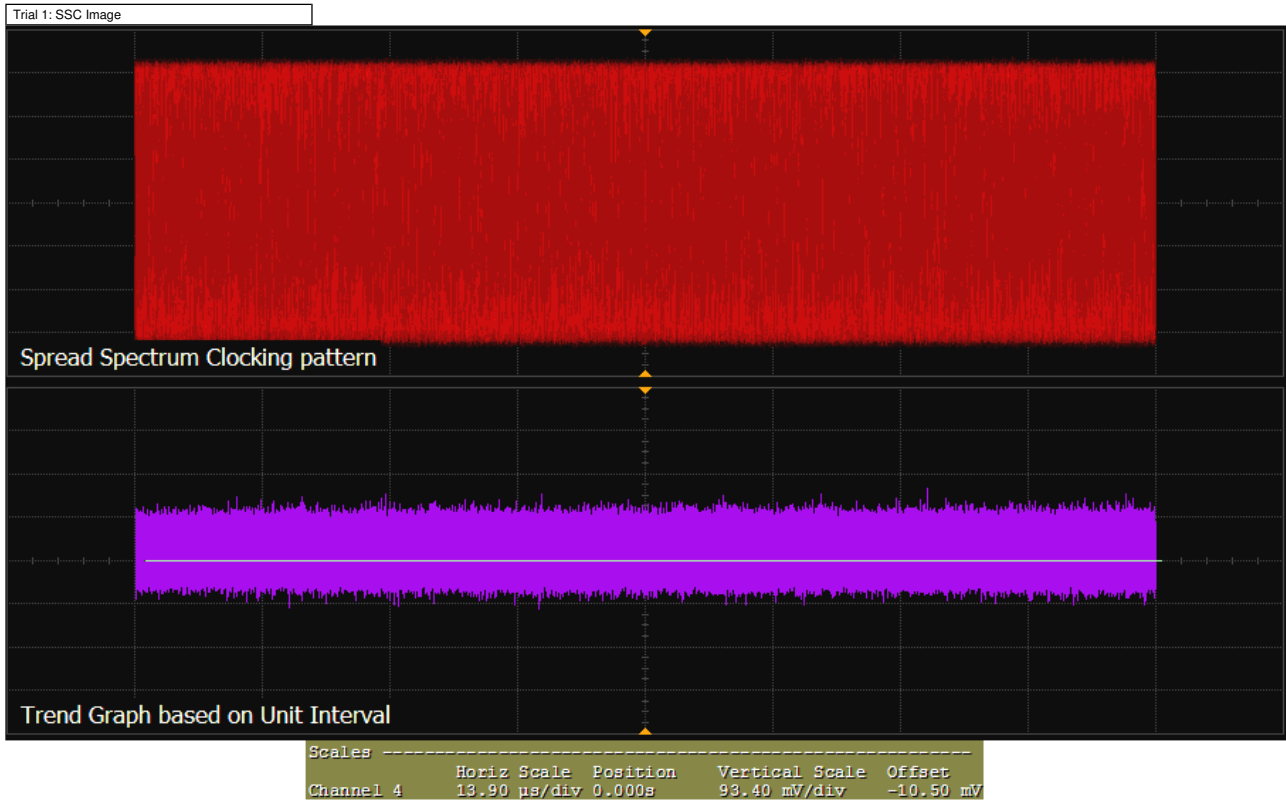
✓ Lane 3 - Main Link Frequency Compliance Reference: DisplayPort CTS Sec. 3.14

Test Summary: Pass Test Description: To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.  
 Pass Limits: [-5.300000 kppm to 300.000 ppm] Lane 3 - Main Link Frequency (Worst of 3 Trials) 6.049 ppm # Trials Run: 3 Worst Trial: Trial 3

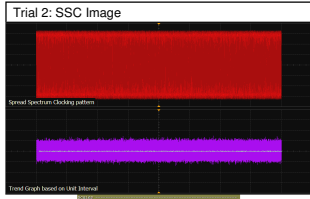
Overall Summary + details of 3 worst trials

Pass	Trial	Actual Value	Margin	SSC Image	Unit Interval (Mean)	Data Rate (Mean)	Data Rate (Max)	Data Rate (Min)	Upper limit Data Rate	Lower limit Data Rate	SSC Acquisitions	VTop	VBase	VSwing	Test Mode	Test Layer	Test Condition
	Avg	4.912 ppm	5.269 %														
	StdDev	1.227 ppm	21.91 m%														
	Range	2.438 ppm	43.54 m%														
	Min	3.611 ppm	5.249 %														
	Max	6.049 ppm	5.293 %														
	Sum	14.73 ppm	15.81 %														
✓	Trial 1	3.611 ppm	5.3%	(See image)	185.1845 ps	5.4000195000000 Gbps	5.4004778357531 Gbps	5.3995476262478 Gbps	5.4016200000000 Gbps	5.3713800000000 Gbps	10	304.120 mV	321.690 mV	625.810 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only
✓	Trial 2	5.074 ppm	5.3%	(See image)	370.3685 ps	2.7000137000000 Gbps	2.7003628751420 Gbps	2.6996695881595 Gbps	2.7008100000000 Gbps	2.6856900000000 Gbps	10	338.110 mV	355.440 mV	693.550 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only
✓	Trial 3 (Worst)	6.049 ppm	5.2%	(See image)	617.2802 ps	1.6200098000000 Gbps	1.6203145982816 Gbps	1.6197017940984 Gbps	1.6204860000000 Gbps	1.6114140000000 Gbps	10	371.830 mV	392.280 mV	764.110 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only

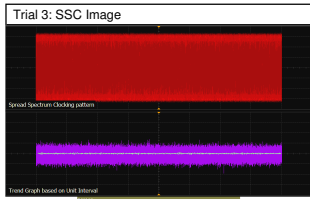
Trial 1



Trial 2



Trial 3



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 ✓ Lane 0 - HBR2CPAT Eye Diagram Test (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.1

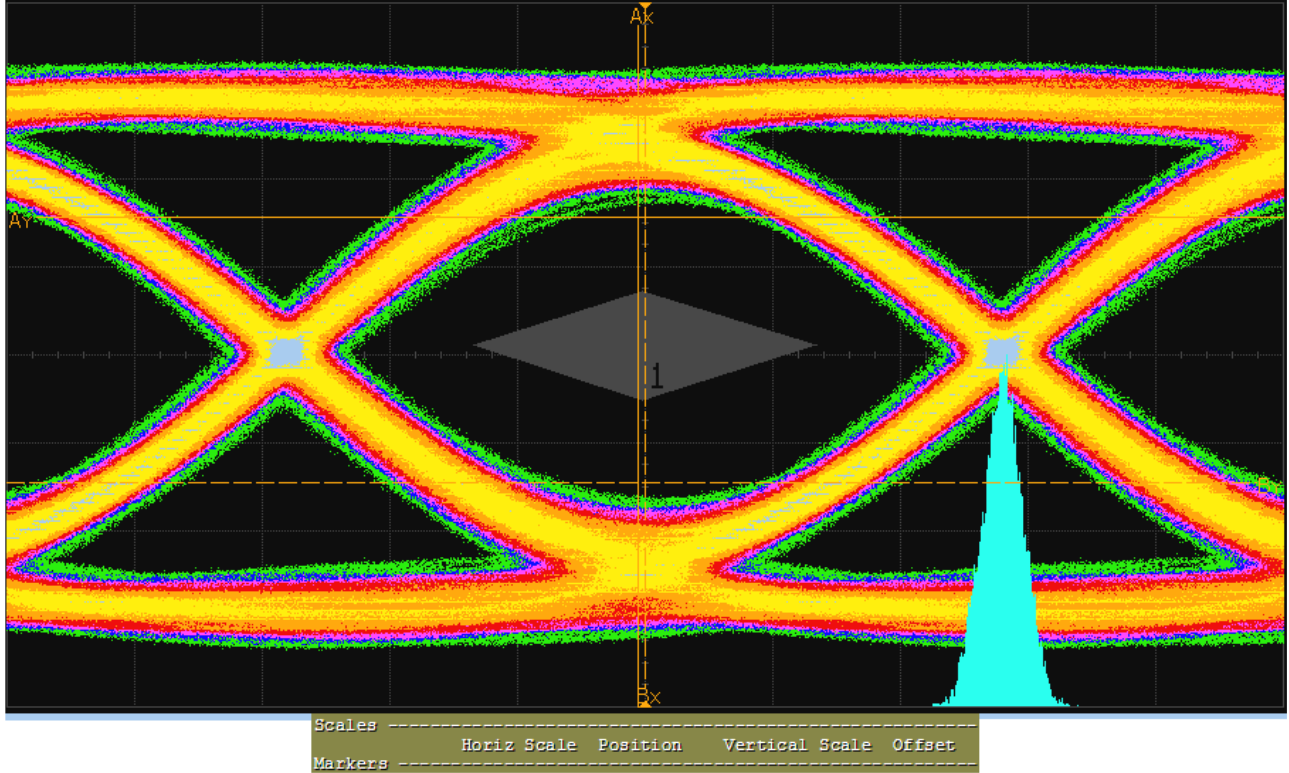
Test Summary: **Pass** Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ) 0.000

**Result Details**

Number of UI	1000000	Statistical Mask Height(VHigh)	65.127 mV	Statistical Mask Height(VLow)	-67.655 mV	Statistical Eye Height	321.468 mV	Statistical Mask Width	479.663 mUI
Measured RNoise VHigh(Sigma)	10.548 mV	Measured RNoise VLow(Sigma)	12.580 mV	Measured Eye Height	350.250 mV	Measured Eye Width	147.760 ps	Max Eye Height Position	490 mUI
Measured Rj	7.900 mUI	Mask Passing Center Position	0.000 V	Vertical Scale	106.450 mV	Test Mode	Compliance	Test Layer	Physical Layer Tests
DUT Type	Source	Test Type	Differential Tests	Connection Type	Differential Probe	BitRate	5.4 Gbps	Level	Swing 2
		PreEmphasis	Pre-emphasis 0	SSC	SSC Disabled	PostCursor2	Level 0		

Trial 1

Trial 1: Eye Diagram Test (TP3\_EQ)



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**✓ Lane 1 - HBR2CPAT Eye Diagram Test (TP3\_EQ)** Reference: DisplayPort CTS Sec. 3.1

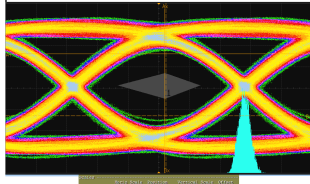
Test Summary: **Pass** Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ) 0.000

**Result Details**

Number of UI	1000000	Statistical Mask Height(VHigh)	66.790 mV	Statistical Mask Height(VLow)	-71.234 mV	Statistical Eye Height	332.856 mV	Statistical Mask Width	479.165 mUI
Measured RNoise VHigh(Sigma)	11.884 mV	Measured RNoise VLow(Sigma)	15.455 mV	Measured Eye Height	366.880 mV	Measured Eye Width	144.470 ps	Max Eye Height Position	530 mUI
Measured Rj	7.700 mUI	Mask Passing Center Position	0.000 V	Vertical Scale	114.304 mV	Test Mode	Compliance	Test Layer	Physical Layer Tests
DUT Type	Source	Test Type	Differential Tests	Connection Type	Differential Probe	BitRate	5.4 Gbps	Level	Swing 2
		PreEmphasis	Pre-emphasis 0	SSC	SSC Disabled	PostCursor2	Level 0		

Trial 1

Trial 1: Eye Diagram Test (TP3\_EQ)



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**✓ Lane 2 - HBR2CPAT Eye Diagram Test (TP3\_EQ)** Reference: DisplayPort CTS Sec. 3.1

Test Summary: **Pass** Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ) 0.000

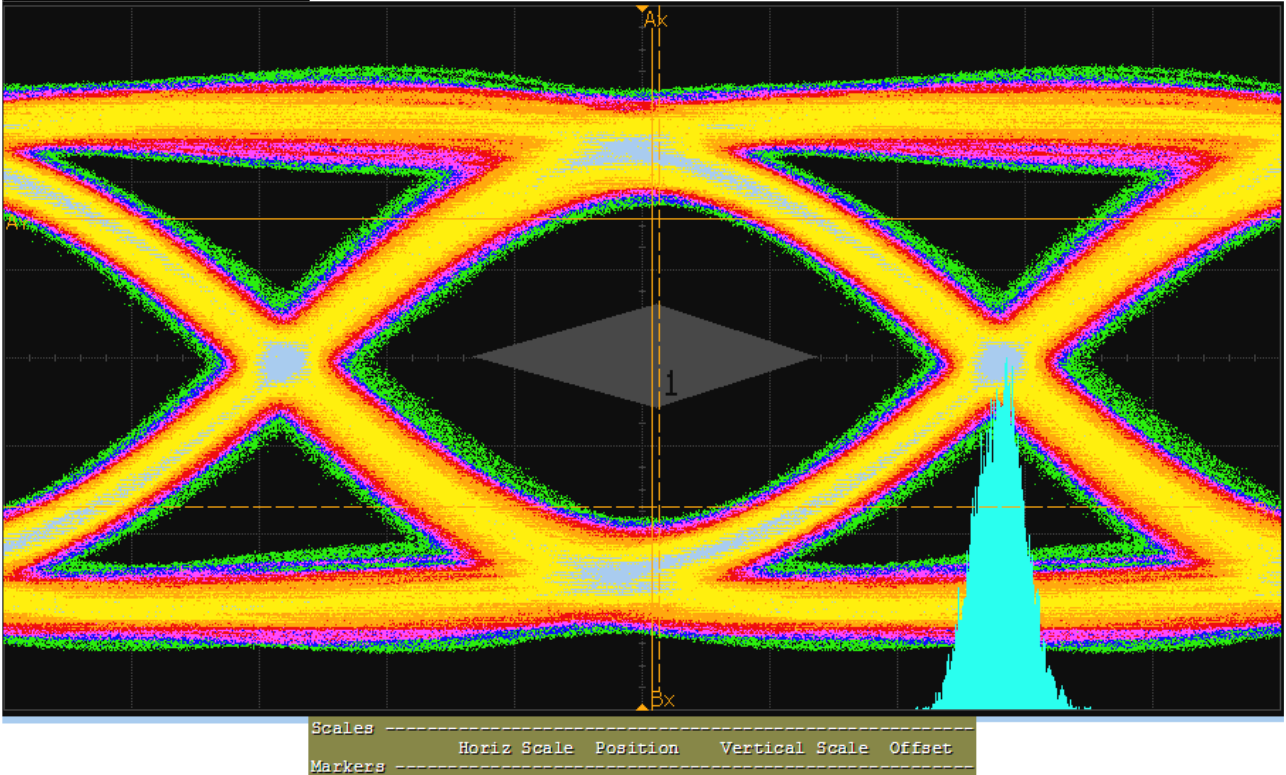
**Result Details**

Number of UI	1000000	Statistical Mask Height(VHigh)	69.565 mV	Statistical Mask Height(VLow)	-66.726 mV	Statistical Eye Height	379.028 mV	Statistical Mask Width	480.161 mUI
Measured RNoise VHigh(Sigma)	14.114 mV	Measured RNoise VLow(Sigma)	11.833 mV	Measured Eye Height	411.320 mV	Measured Eye Width	140.070 ps	Max Eye Height Position	510 mUI
Measured Rj	8.100 mUI	Mask Passing Center Position	0.000 V	Vertical Scale	115.918 mV	Test Mode	Compliance	Test Layer	Physical Layer Tests
DUT Type	Source	Test Type	Differential Tests	Connection Type	Differential Probe	BitRate	5.4 Gbps	Level	Swing 2
		PreEmphasis	Pre-emphasis 0	SSC	SSC Disabled	PostCursor2	Level 0		

Trial 1



Trial 1: Eye Diagram Test (TP3\_EQ)



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✓ Lane 3 - HBR2CPAT Eye Diagram Test (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

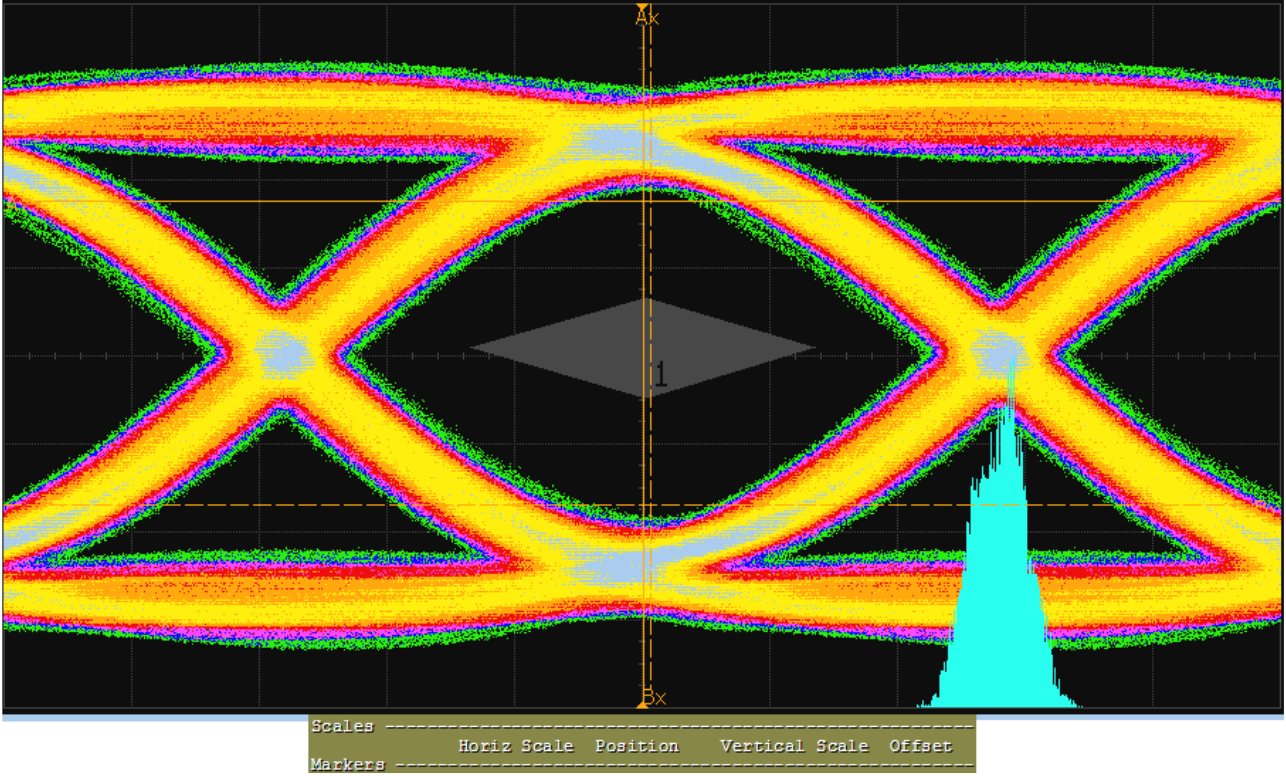
Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ) 0.000

Result Details

Number of UI	1000000	Statistical Mask Height(VHigh)	64.694 mV	Statistical Mask Height(VLow)	-65.455 mV	Statistical Eye Height	394.002 mV	Statistical Mask Width	479.414 mUI
Measured RNoise VHigh(Sigma)	10.200 mV	Measured RNoise VLow(Sigma)	10.811 mV	Measured Eye Height	420.150 mV	Measured Eye Width	142.630 ps	Max Eye Height Position	500 mUI
Measured Rj	7.800 mUI	Mask Passing Center Position	0.000 V	Vertical Scale	114.253 mV	Test Mode	Compliance	Test Layer	Physical Layer Tests
DUT Type	Source	Test Type	Differential Tests	Connection Type	Differential Probe	BitRate	5.4 Gbps	Level Swing	2
						PreEmphasis	Pre-emphasis 0	SSC	SSC Disabled
						PostCursor2	Level 0		

Trial 1

Trial 1: Eye Diagram Test (TP3\_EQ)



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✓ Lane 0 - HBR2CPAT Total Jitter Test (TP3\_EQ)

Reference: DisplayPort CTS Sec. 3.12: Table 3.19 VESA DisplayPort Standard specification

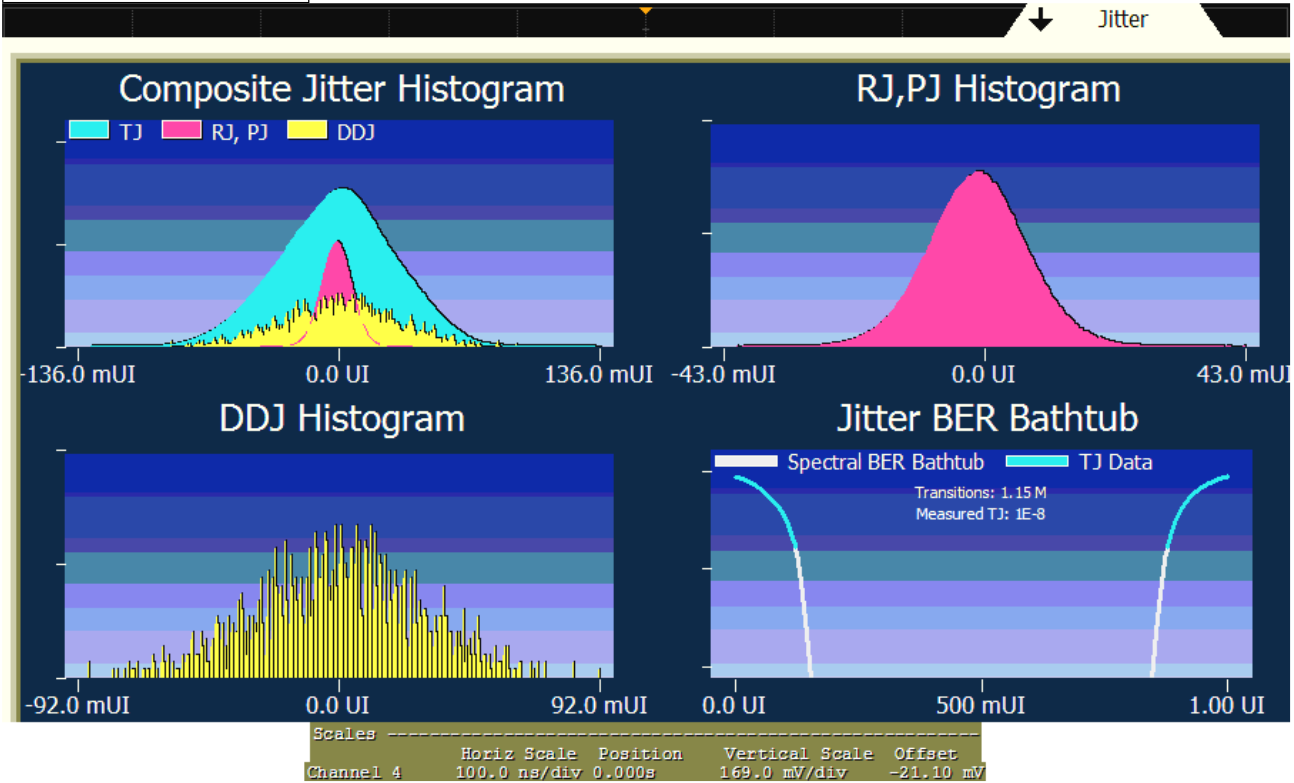
Test Summary: **Pass** Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
**Pass Limits:** <= 580.000 mUI | **HBR2CPAT Total Jitter Test (TP3\_EQ)** 262.600 mUI

**Result Details**

**Jitter Separation Image** (See image) | **Edges** 1.00000000 M | **Total Jitter (TJ)** 262.6 mUI | **Total Jitter (TJ) in ps** 48.6283 ps | **Periodic Jitter (PJ rms)** 2.3 mUI | **Periodic Jitter (PJ p-p)** 11.3 mUI  
**Deterministic Jitter (DJ)** 168.2 mUI | **Random Jitter (RJ)** 7.8 mUI | **ISI Jitter (ISI)** 154.4 mUI | **Data Dependent Jitter (DDJ)** 181.1 mUI | **Bit Error Rate (BER)** E9 | **Test Mode** Compliance  
**Test Layer** Physical Layer Tests | **Test Condition** Compliance Conditions Only | **DUT Type** Source | **Test Type** Differential Tests | **Connection Type** Differential Probe | **BitRate** 5.4 Gbps | **Level** Swing 2  
**PreEmphasis** Pre-emphasis 0 | **SSC** SSC Disabled | **PostCursor2** Level 0

Trial 1

Trial 1: Jitter Separation Image



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**Lane 1 - HBR2CPAT Total Jitter Test (TP3\_EQ)** Reference: DisplayPort CTS Sec. 3.12: Table 3.19 VESA DisplayPort Standard specification

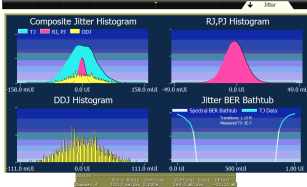
Test Summary: **Pass** Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
**Pass Limits:** <= 580.000 mUI | **HBR2CPAT Total Jitter Test (TP3\_EQ)** 286.700 mUI

**Result Details**

**Jitter Separation Image** (See image) | **Edges** 1.00000000 M | **Total Jitter (TJ)** 286.7 mUI | **Total Jitter (TJ) in ps** 53.0909 ps | **Periodic Jitter (PJ rms)** 2.2 mUI | **Periodic Jitter (PJ p-p)** 12.7 mUI  
**Deterministic Jitter (DJ)** 191.5 mUI | **Random Jitter (RJ)** 7.9 mUI | **ISI Jitter (ISI)** 194.7 mUI | **Data Dependent Jitter (DDJ)** 206.4 mUI | **Bit Error Rate (BER)** E9 | **Test Mode** Compliance  
**Test Layer** Physical Layer Tests | **Test Condition** Compliance Conditions Only | **DUT Type** Source | **Test Type** Differential Tests | **Connection Type** Differential Probe | **BitRate** 5.4 Gbps | **Level** Swing 2  
**PreEmphasis** Pre-emphasis 0 | **SSC** SSC Disabled | **PostCursor2** Level 0

Trial 1

Trial 1: Jitter Separation Image



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**Lane 2 - HBR2CPAT Total Jitter Test (TP3\_EQ)** Reference: DisplayPort CTS Sec. 3.12: Table 3.19 VESA DisplayPort Standard specification

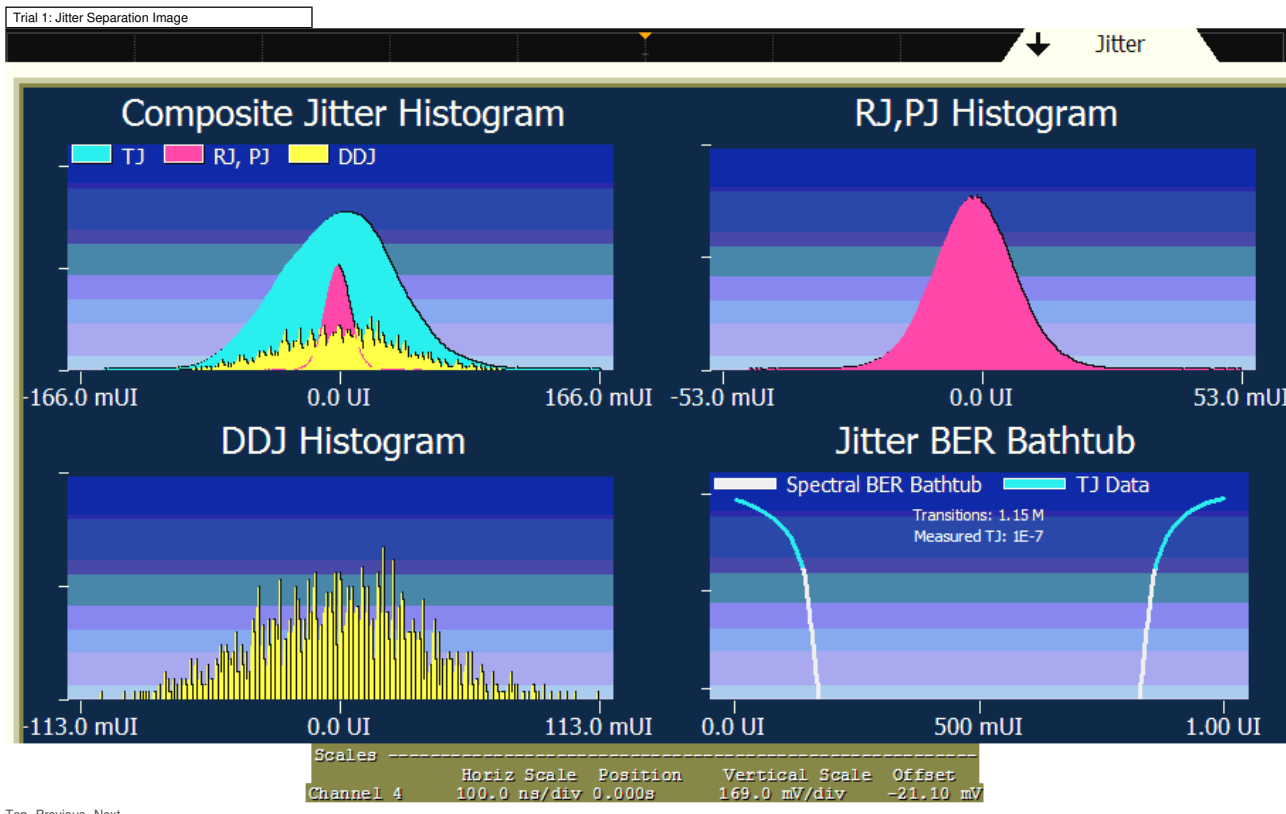
Test Summary: **Pass** Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
**Pass Limits:** <= 580.000 mUI | **Lane 2 HBR2CPAT Total Jitter Test (TP3\_EQ)** 300.000 mUI

**Result Details**

**Jitter Separation Image** (See image) | **Edges** 1.00000000 M | **Total Jitter (TJ)** 300.0 mUI | **Total Jitter (TJ) in ps** 55.5537 ps | **Periodic Jitter (PJ rms)** 2.5 mUI | **Periodic Jitter (PJ p-p)** 15.9 mUI  
**Deterministic Jitter (DJ)** 205.1 mUI | **Random Jitter (RJ)** 7.9 mUI | **ISI Jitter (ISI)** 206.8 mUI | **Data Dependent Jitter (DDJ)** 217.7 mUI | **Bit Error Rate (BER)** E9 | **Test Mode** Compliance  
**Test Layer** Physical Layer Tests | **Test Condition** Compliance Conditions Only | **DUT Type** Source | **Test Type** Differential Tests | **Connection Type** Differential Probe | **BitRate** 5.4 Gbps | **Level** Swing 2  
**PreEmphasis** Pre-emphasis 0 | **SSC** SSC Disabled | **PostCursor2** Level 0

Trial 1





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✓ Lane 3 - HBR2CPAT Total Jitter Test (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.12; Table 3.19 VESA DisplayPort Standard specification

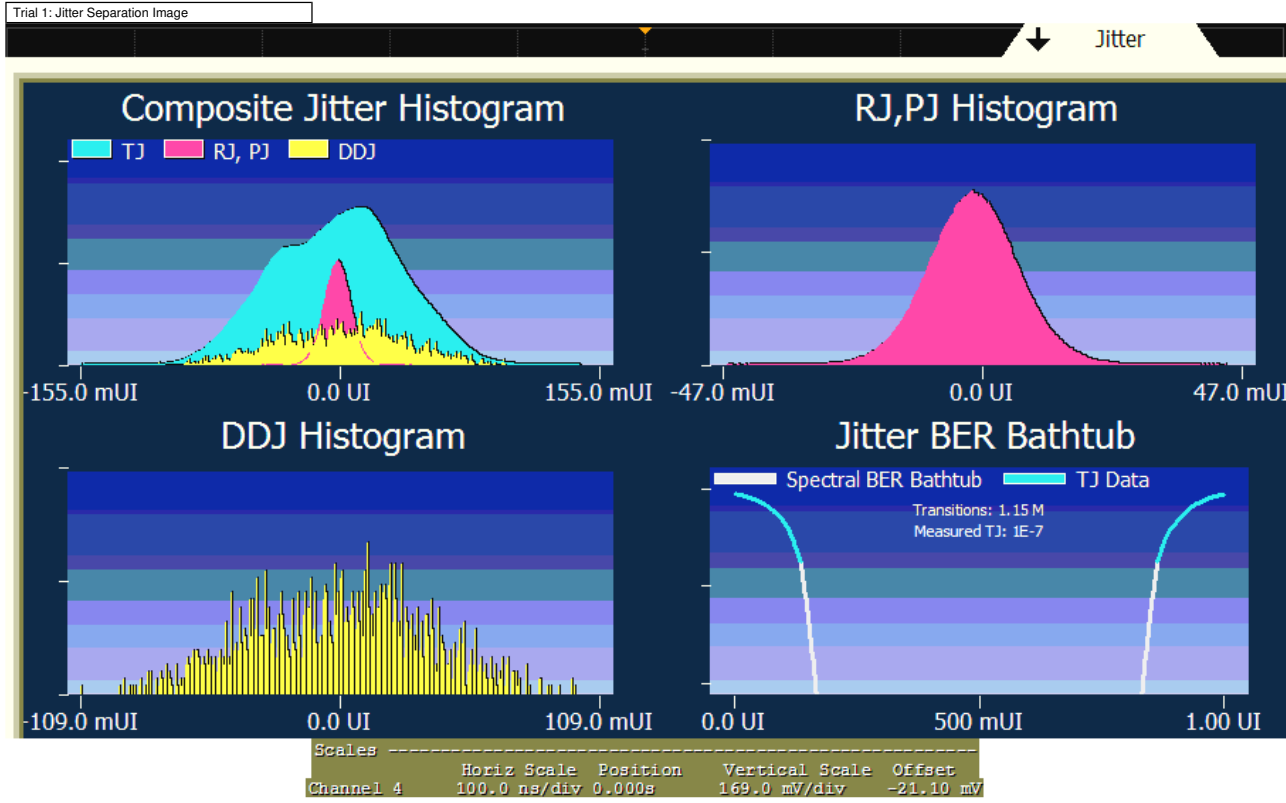
Test Summary: **Pass** Test Description: To evaluate the Total Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 580.000 mUI | **HBR2CPAT Total Jitter Test (TP3\_EQ)** 289.700 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.00000000 M	Total Jitter (TJ) 289.7 mUI	Total Jitter (TJ) in ps 53.6464 ps	Periodic Jitter (PJ rms) 2.1 mUI	Periodic Jitter (PJ p-p) 12.0 mUI
Deterministic Jitter (DJ) 194.5 mUI	Random Jitter (RJ) 7.9 mUI	ISI Jitter (ISI) 187.5 mUI	Data Dependent Jitter (DDJ) 208.2 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2

**Trial 1**



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✓ Lane 0 - HBR2CPAT Deterministic Jitter Test (TP3\_EQ)

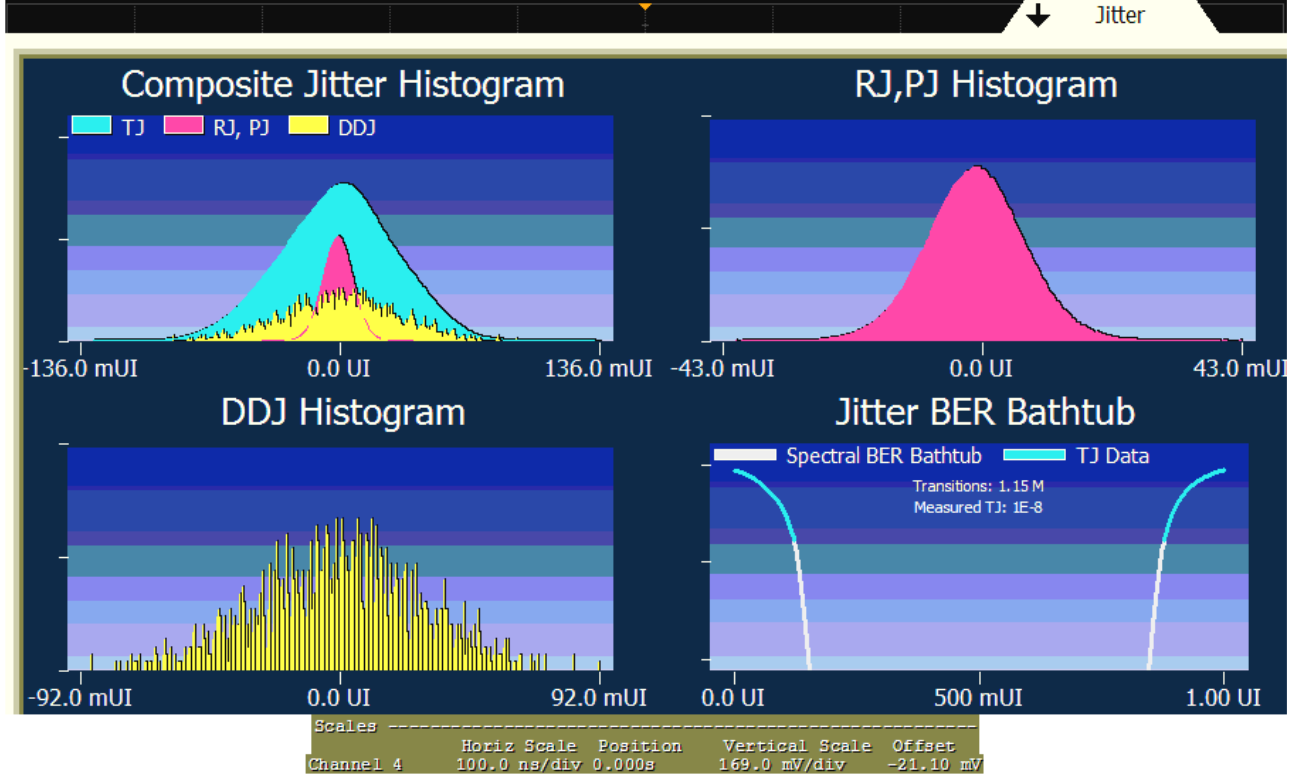
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 490.000 mUI HBR2CPAT Deterministic Jitter Test (TP3\_EQ) 168.200 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 262.6 mUI	Total Jitter (TJ) in ps 48.6283 ps	Periodic Jitter (PJ rms) 2.3 mUI	Periodic Jitter (PJ p-p) 11.3 mUI
Deterministic Jitter (DJ) 168.2 mUI	Random Jitter (RJ) 7.8 mUI	ISI Jitter (ISI) 154.4 mUI	Data Dependent Jitter (DDJ) 181.1 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 1 - HBR2CPAT Deterministic Jitter Test (TP3\_EQ)

Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

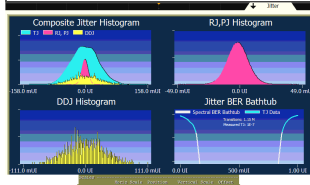
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 490.000 mUI HBR2CPAT Deterministic Jitter Test (TP3\_EQ) 191.500 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 286.7 mUI	Total Jitter (TJ) in ps 53.0909 ps	Periodic Jitter (PJ rms) 2.2 mUI	Periodic Jitter (PJ p-p) 12.7 mUI
Deterministic Jitter (DJ) 191.5 mUI	Random Jitter (RJ) 7.9 mUI	ISI Jitter (ISI) 194.7 mUI	Data Dependent Jitter (DDJ) 206.4 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 2 - HBR2CPAT Deterministic Jitter Test (TP3\_EQ)

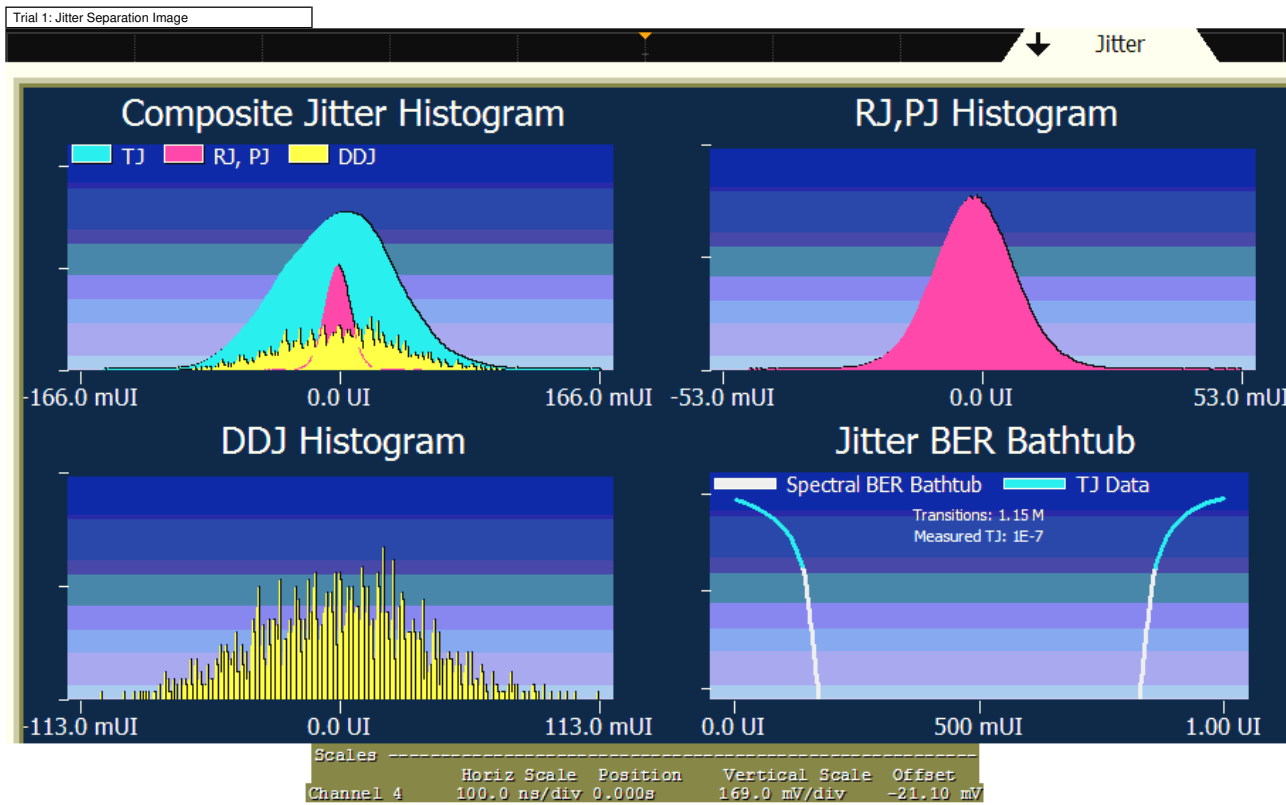
Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 490.000 mUI Lane 2 HBR2CPAT Deterministic Jitter Test (TP3\_EQ) 205.100 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 300.0 mUI	Total Jitter (TJ) in ps 55.5537 ps	Periodic Jitter (PJ rms) 2.5 mUI	Periodic Jitter (PJ p-p) 15.9 mUI
Deterministic Jitter (DJ) 205.1 mUI	Random Jitter (RJ) 7.9 mUI	ISI Jitter (ISI) 206.8 mUI	Data Dependent Jitter (DDJ) 217.7 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 2
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1



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✓ Lane 3 - HBR2CPAT Deterministic Jitter Test (TP3\_EQ) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

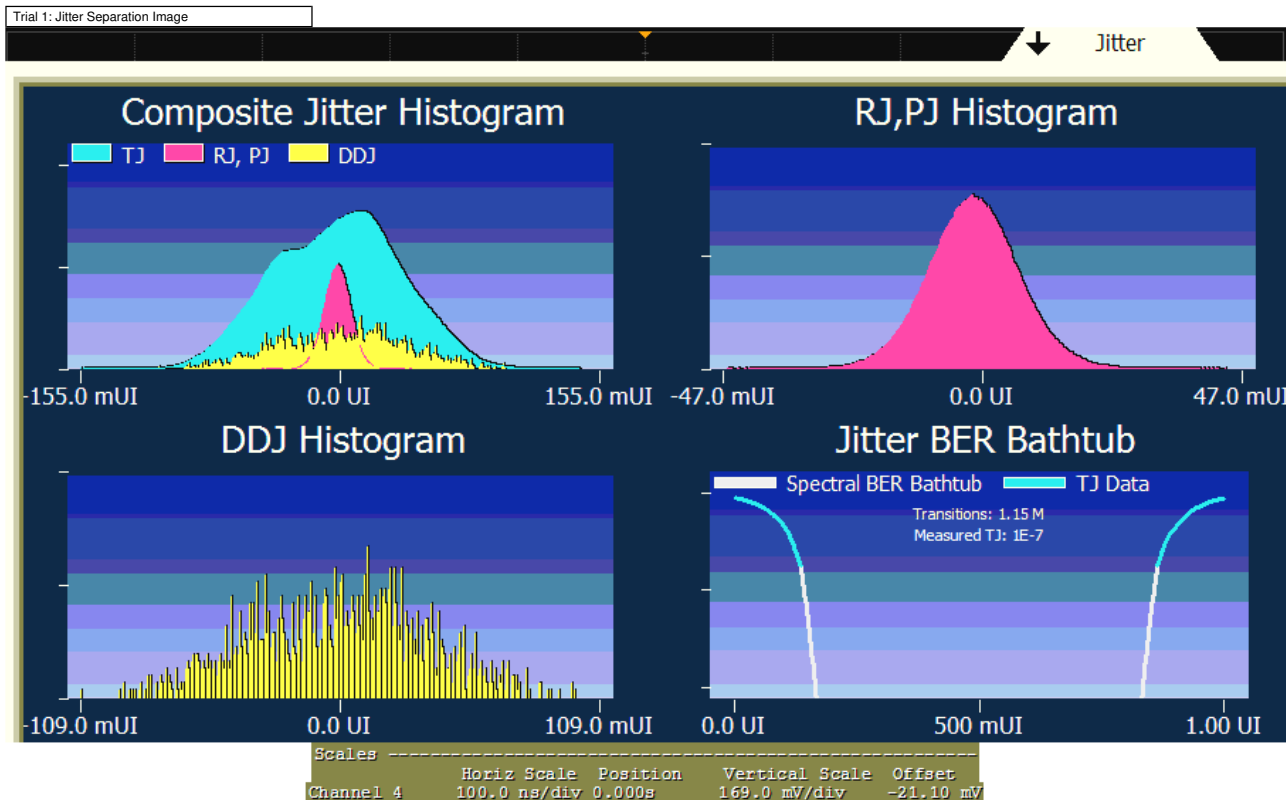
Test Summary: **Pass** Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 490.000 mUI | **HBR2CPAT Deterministic Jitter Test (TP3\_EQ)** 194.500 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 289.7 mUI	Total Jitter (TJ) in ps 53.6464 ps	Periodic Jitter (PJ rms) 2.1 mUI	Periodic Jitter (PJ p-p) 12.0 mUI
Deterministic Jitter (DJ) 194.5 mUI	Random Jitter (RJ) 7.9 mUI	ISI Jitter (ISI) 187.5 mUI	Data Dependent Jitter (DDJ) 208.2 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 2

Trial 1



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✓ Lane 0 - PLTPAT - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the Peak to Peak Voltage.  
**Pass Limits:** <= 1.380 V | **Peak to Peak Voltage (Worst of 9 Trials)** 1.081 V | **# Trials Run:** 9 | **Worst Trial:** Trial 9

Overall Summary + details of 9 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	772.9 mV	43.99 %													
	<i>StdDev</i>	192.1 mV	13.92 %													
	<i>Range</i>	624.4 mV	45.22 %													
	<i>Min</i>	456.9 mV	21.67 %													
	<i>Max</i>	1.081 V	66.88 %													
	<i>Sum</i>	6.956 V	395.9 %													
✓	Trial 1	874 mV	36.7%	427.140 mV	-446.740 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	906 mV	34.3%	449.130 mV	-456.680 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	647 mV	53.1%	313.270 mV	-333.670 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	780 mV	43.5%	388.630 mV	-391.560 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	799 mV	42.1%	395.270 mV	-404.080 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 6	457 mV	66.9%	218.190 mV	-238.660 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	553 mV	59.9%	268.850 mV	-283.960 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	859 mV	37.8%	427.080 mV	-431.750 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 9 (Worst)	1.081 V	21.7%	530.840 mV	-550.450 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 1 - PLTPAT - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the peak to peak voltage.  
**Pass Limits:** <= 1.380 V **Peak to Peak Voltage (Worst of 10 Trials)** 1.093 V **# Trials Run:** 10 **Worst Trial:** Trial 10

Overall Summary + details of 10 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	790.4 mV	42.72 %													
	<i>StdDev</i>	207.8 mV	15.07 %													
	<i>Range</i>	631.8 mV	45.80 %													
	<i>Min</i>	461.5 mV	20.80 %													
	<i>Max</i>	1.093 V	66.59 %													
	<i>Sum</i>	7.904 V	427.2 %													
✓	Trial 1	872 mV	36.8%	427.240 mV	-444.550 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	987 mV	28.5%	483.710 mV	-502.970 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	651 mV	52.8%	315.300 mV	-335.300 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	794 mV	42.5%	387.890 mV	-406.580 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	861 mV	37.6%	411.980 mV	-448.920 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 6	461 mV	66.6%	222.040 mV	-239.440 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	564 mV	59.1%	273.150 mV	-291.150 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	627 mV	54.6%	296.640 mV	-330.650 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	994 mV	28.0%	486.970 mV	-506.770 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10 (Worst)	1.093 V	20.8%	534.220 mV	-559.020 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 2 - PLTPAT - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the peak to peak voltage.  
**Pass Limits:** <= 1.380 V **Peak to Peak Voltage (Worst of 10 Trials)** 1.091 V **# Trials Run:** 10 **Worst Trial:** Trial 10

Overall Summary + details of 10 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	<i>808.3 mV</i>	<i>41.43 %</i>													
	<i>StdDev</i>	<i>201.4 mV</i>	<i>14.60 %</i>													
	<i>Range</i>	<i>614.2 mV</i>	<i>44.57 %</i>													
	<i>Min</i>	<i>476.5 mV</i>	<i>20.94 %</i>													
	<i>Max</i>	<i>1.091 V</i>	<i>65.51 %</i>													
	<i>Sum</i>	<i>8.083 V</i>	<i>414.3 %</i>													
✓	Trial 1	890 mV	35.5%	437.370 mV	-452.570 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	937 mV	32.1%	455.870 mV	-481.190 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	664 mV	51.9%	322.350 mV	-341.520 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	790 mV	42.8%	379.950 mV	-409.600 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	955 mV	30.8%	463.080 mV	-492.080 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 6	476 mV	65.5%	229.730 mV	-246.730 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	549 mV	60.2%	261.440 mV	-287.310 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	733 mV	46.9%	353.010 mV	-380.350 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	998 mV	27.7%	488.330 mV	-509.850 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10 (Worst)	1.091 V	20.9%	535.130 mV	-555.520 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 3 - PLTPAT - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: **Pass** Test Description: To evaluate the peak to peak voltage.  
**Pass Limits:** <= 1.380 V | **Peak to Peak Voltage (Worst of 10 Trials)** 1.099 V | **# Trials Run:** 10 | **Worst Trial:** Trial 10

Overall Summary + details of 10 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<b>Avg</b>	784.8 mV	43.12 %													
	<b>StdDev</b>	205.4 mV	14.87 %													
	<b>Range</b>	647.4 mV	46.88 %													
	<b>Min</b>	451.6 mV	20.36 %													
	<b>Max</b>	1.099 V	67.25 %													
	<b>Sum</b>	7.848 V	431.2 %													
✓	Trial 1	874 mV	36.7%	426.850 mV	-447.020 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	982 mV	28.8%	479.090 mV	-503.170 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	645 mV	53.3%	311.390 mV	-333.330 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	787 mV	43.0%	382.220 mV	-404.700 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 5	908 mV	34.2%	442.480 mV	-465.500 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 6	452 mV	67.2%	216.540 mV	-235.010 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	555 mV	59.8%	266.880 mV	-287.920 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	641 mV	53.6%	310.590 mV	-330.380 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	906 mV	34.3%	434.300 mV	-471.500 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10 (Worst)	1.099 V	20.4%	535.470 mV	-563.470 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 0 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [5.2000 dB to 6.9000 dB] | **Lane 0 Non-PreEmphasis Level Test (Swing 2/Swing 0)** 5.7342 dB

Result Details

Level VH Image (Swing 2) (See image) | Level VL Image (Swing 2) (See image) | Level VH Image (Swing 0) (See image) | Level VL Image (Swing 0) (See image) | Number of UI 1000  
 VH Trigger Pattern 011111 | VL Trigger Pattern 100000 | VTop (Swing 2) 382.349 mV | VBase (Swing 2) -406.953 mV | VSwing (Swing 2) 789.302 mV | VTop (Swing 0) 193.426 mV  
 VBase(Swing 0) -214.453 mV | VSwing(Swing 0) 407.879 mV | Test Mode Compliance | Test Layer Physical Layer Tests | Test Condition Compliance Conditions Only | DUT Type Source  
 Test Type Differential Tests | Connection Type Differential Probe | BitRate 5.4 Gbps | Level Swing 2 | PreEmphasis Pre-emphasis 0 | SSC SSC Disabled | PostCursor2 Level 0

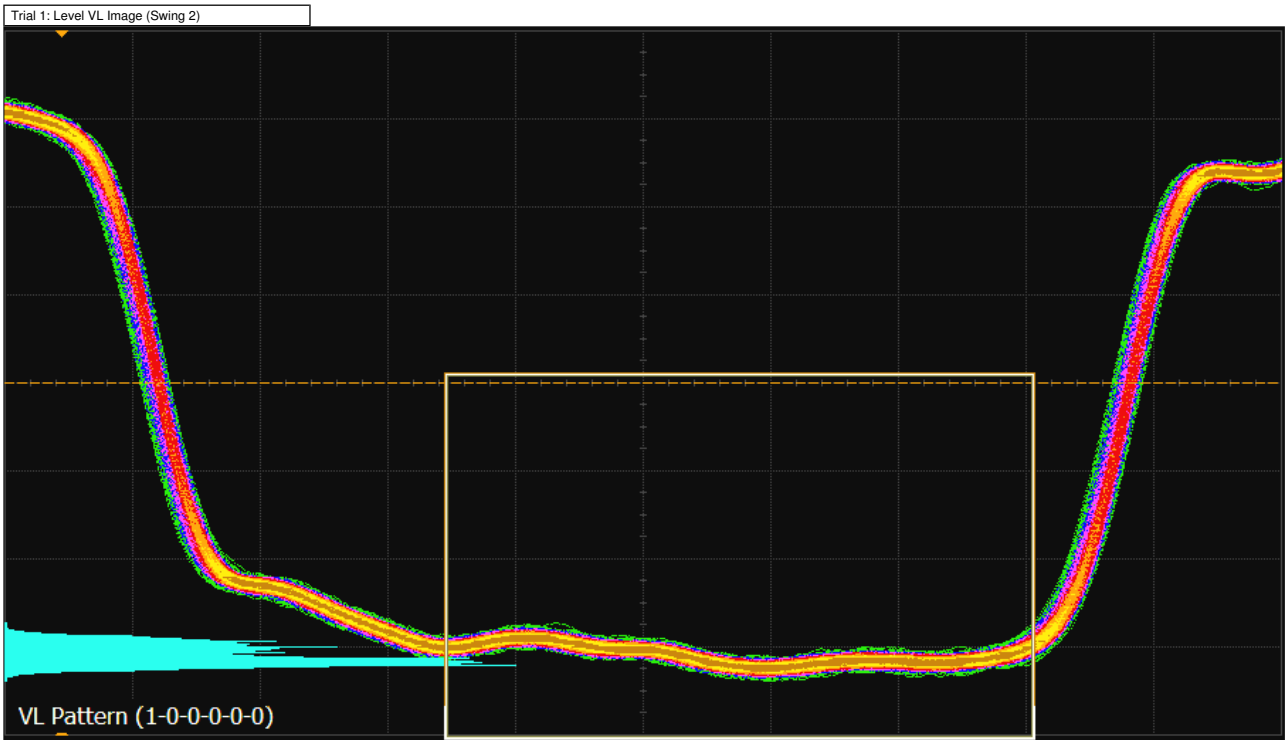
Trial 1

Trial 1: Level VH Image (Swing 2)

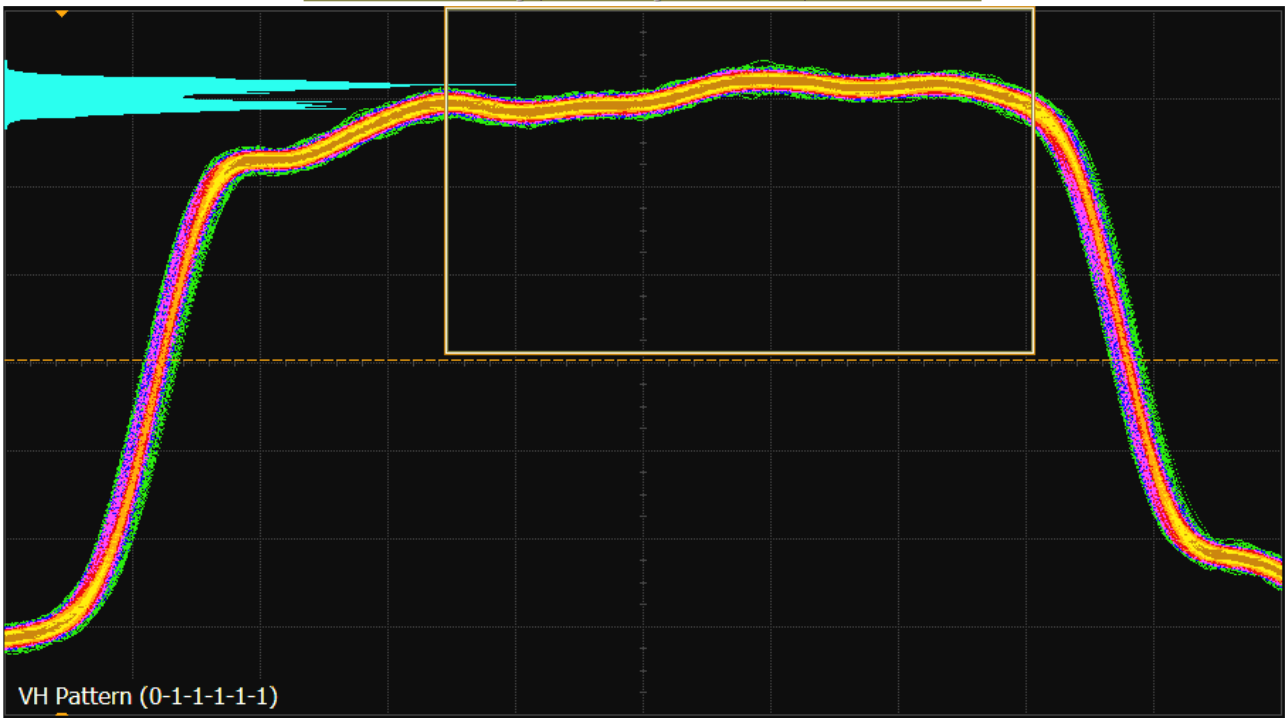


VH Pattern (0-1-1-1-1)

Scales  
 Channel 1 Horiz Scale Position Vertical Scale Offset  
 122.0 ps/div 555.6 ps 130.0 mV/div -9.200 mV

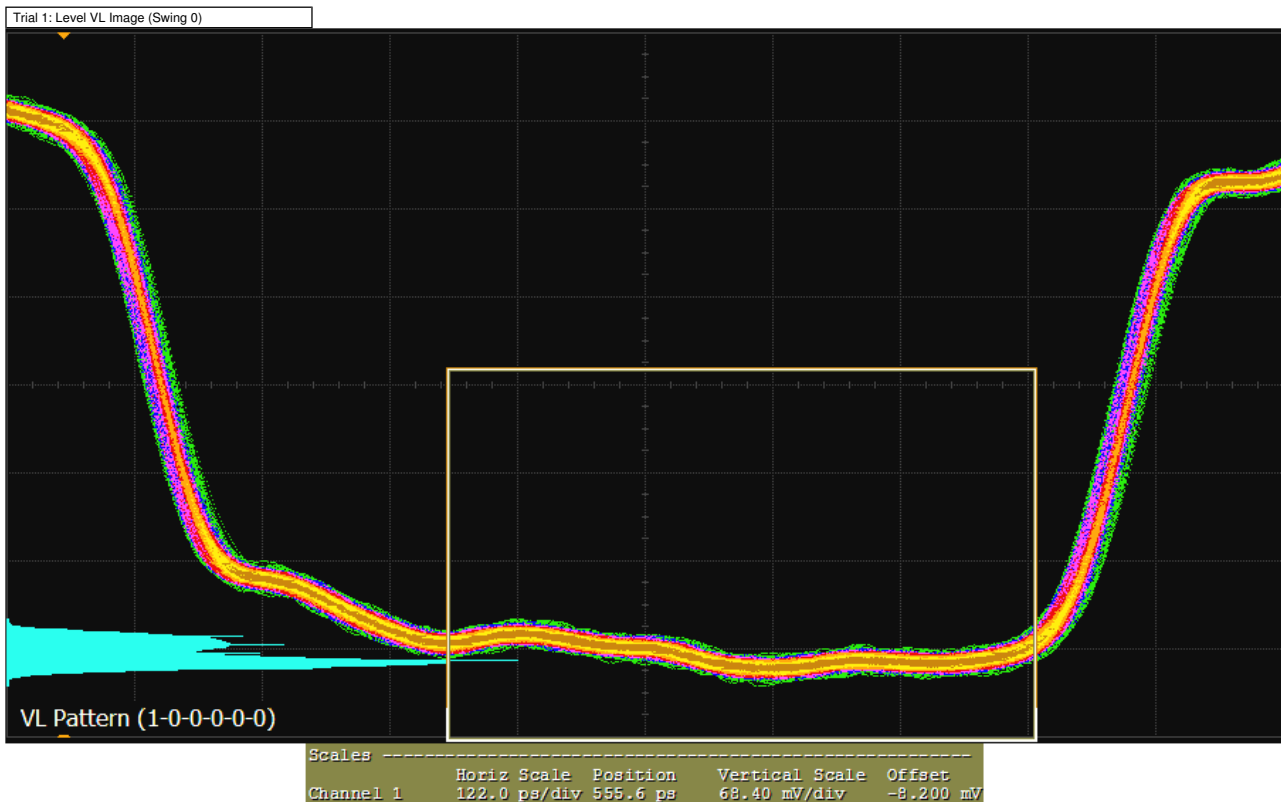


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	130.0 mV/div	-9.200 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	68.40 mV/div	-8.200 mV





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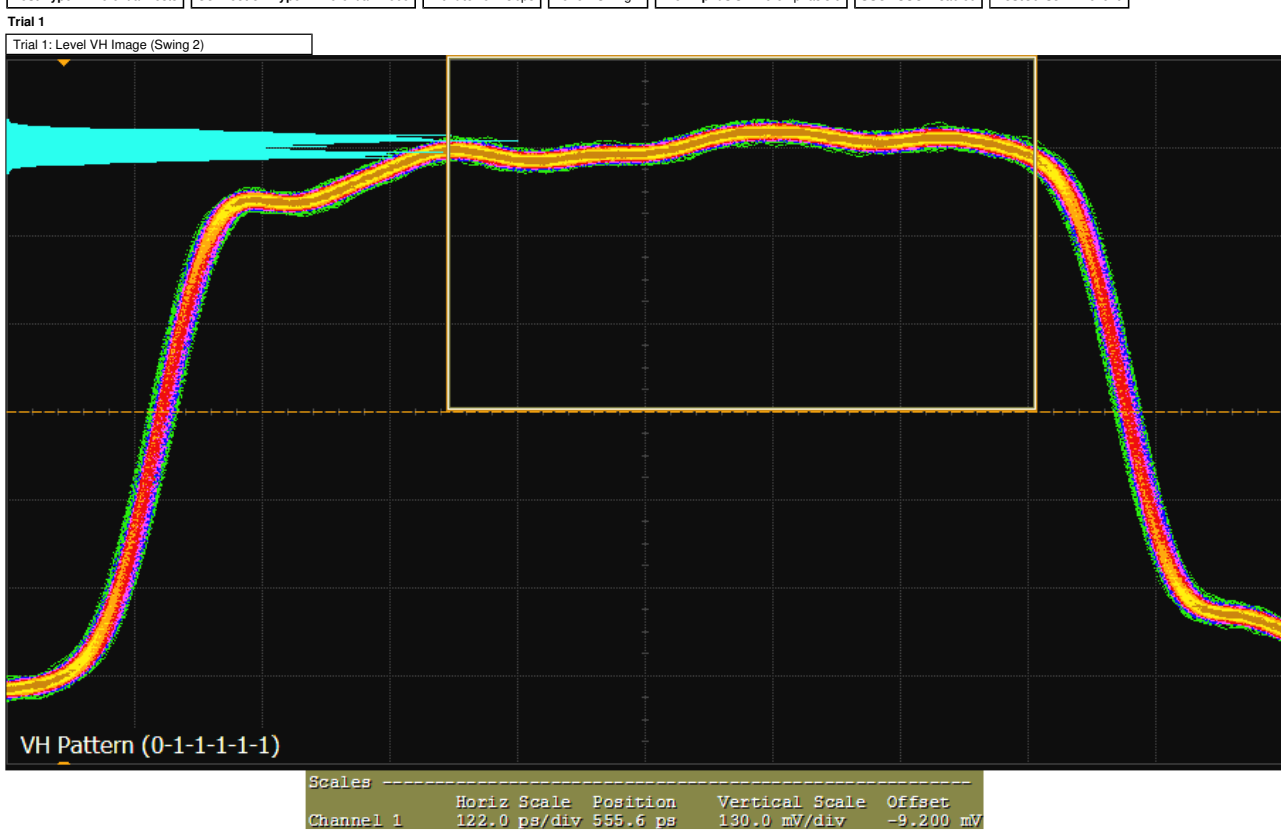
✓ Lane 0 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

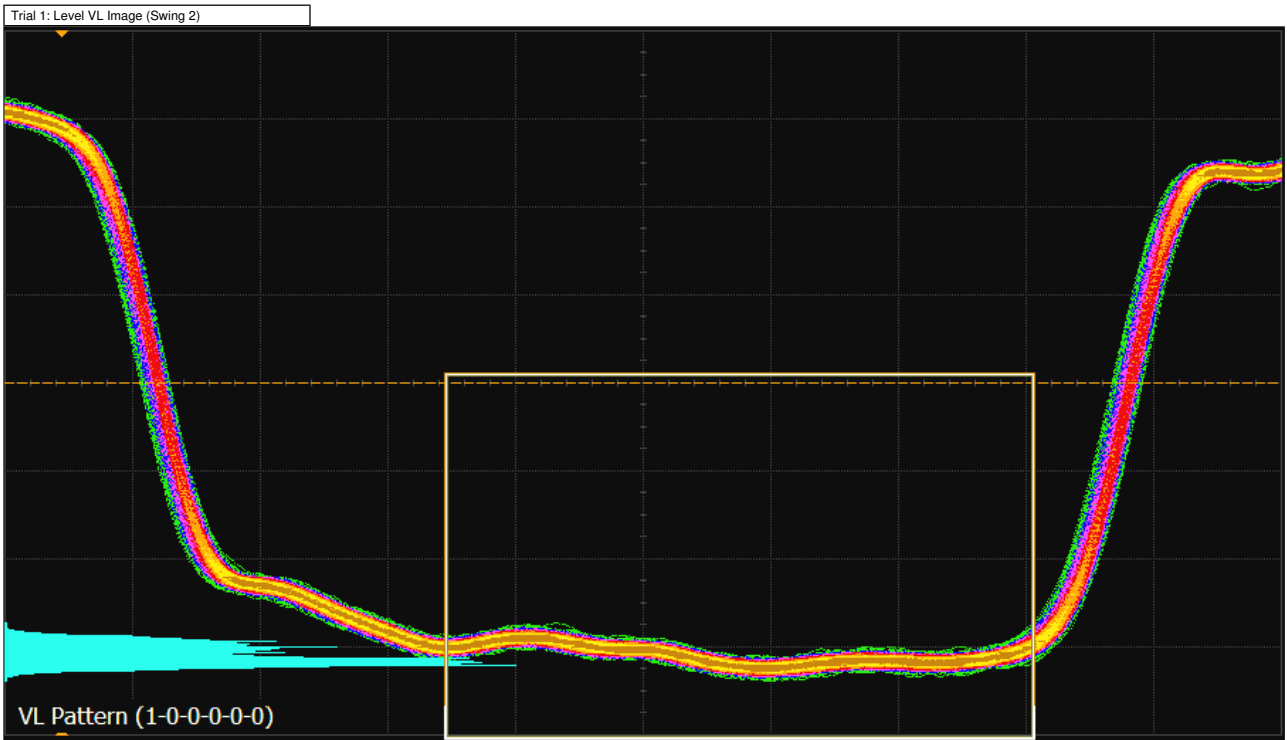
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Pass Limits: [1.6000 dB to 3.5000 dB] Lane 0 Non-PreEmphasis Level Test (Swing 2/Swing 1) 2.6962 dB

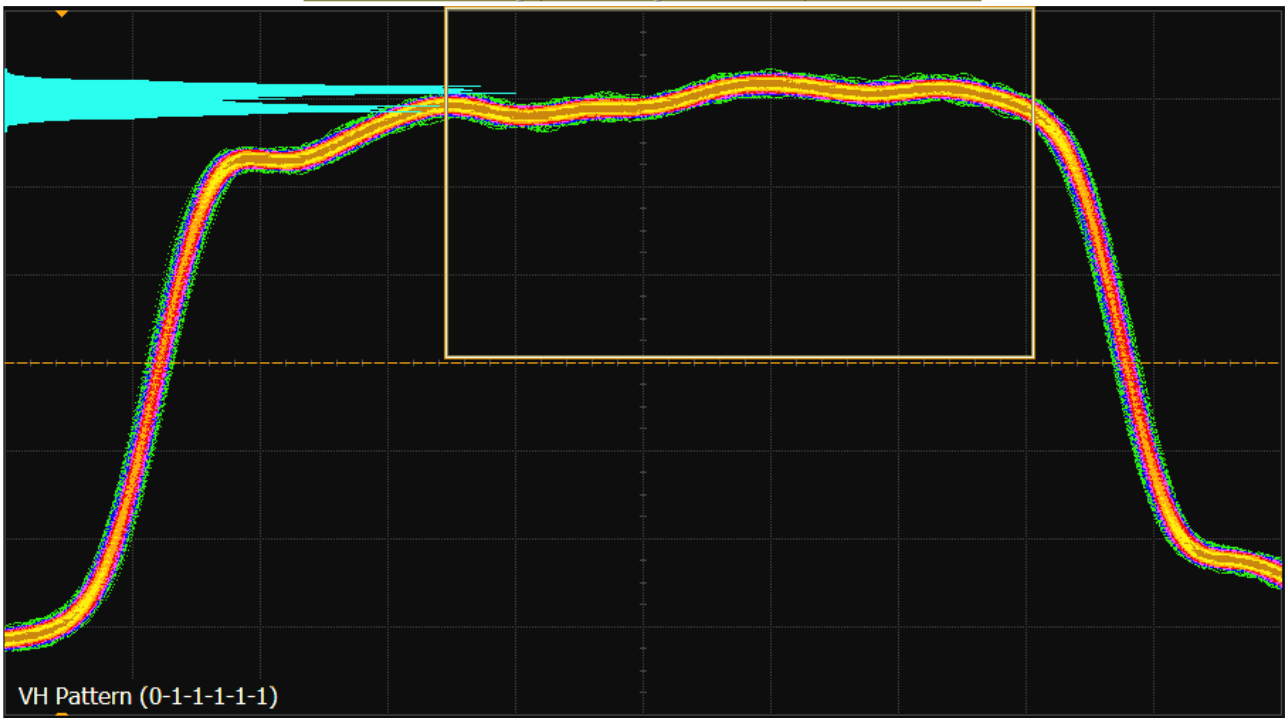
**Result Details**

<span style="border: 1px solid black; padding: 2px;">Level VH Image (Swing 2) (See image)</span>	<span style="border: 1px solid black; padding: 2px;">Level VL Image (Swing 2) (See image)</span>	<span style="border: 1px solid black; padding: 2px;">Level VH Image (Swing 1) (See image)</span>	<span style="border: 1px solid black; padding: 2px;">Level VL Image (Swing 1) (See image)</span>	<span style="border: 1px solid black; padding: 2px;">Number of UI 1000</span>
<span style="border: 1px solid black; padding: 2px;">VH Trigger Pattern 011111</span>	<span style="border: 1px solid black; padding: 2px;">VL Trigger Pattern 100000</span>	<span style="border: 1px solid black; padding: 2px;">VTop (Swing 2) 382.349 mV</span>	<span style="border: 1px solid black; padding: 2px;">VBase (Swing 2) -406.953 mV</span>	<span style="border: 1px solid black; padding: 2px;">VSwing (Swing 2) 789.302 mV</span>
<span style="border: 1px solid black; padding: 2px;">VTop (Swing 1) 277.980 mV</span>	<span style="border: 1px solid black; padding: 2px;">VBase (Swing 1) -300.693 mV</span>	<span style="border: 1px solid black; padding: 2px;">VSwing (Swing 1) 578.674 mV</span>	<span style="border: 1px solid black; padding: 2px;">Test Mode Compliance</span>	<span style="border: 1px solid black; padding: 2px;">Test Layer Physical Layer Tests</span>
<span style="border: 1px solid black; padding: 2px;">Test Condition Compliance Conditions Only</span>	<span style="border: 1px solid black; padding: 2px;">DUT Type Source</span>	<span style="border: 1px solid black; padding: 2px;">Test Type Differential Tests</span>	<span style="border: 1px solid black; padding: 2px;">Connection Type Differential Probe</span>	<span style="border: 1px solid black; padding: 2px;">BitRate 5.4 Gbps</span>
<span style="border: 1px solid black; padding: 2px;">Level Swing 2</span>	<span style="border: 1px solid black; padding: 2px;">PreEmphasis Pre-emphasis 0</span>	<span style="border: 1px solid black; padding: 2px;">SSC SSC Disabled</span>	<span style="border: 1px solid black; padding: 2px;">PostCursor2 Level 0</span>	

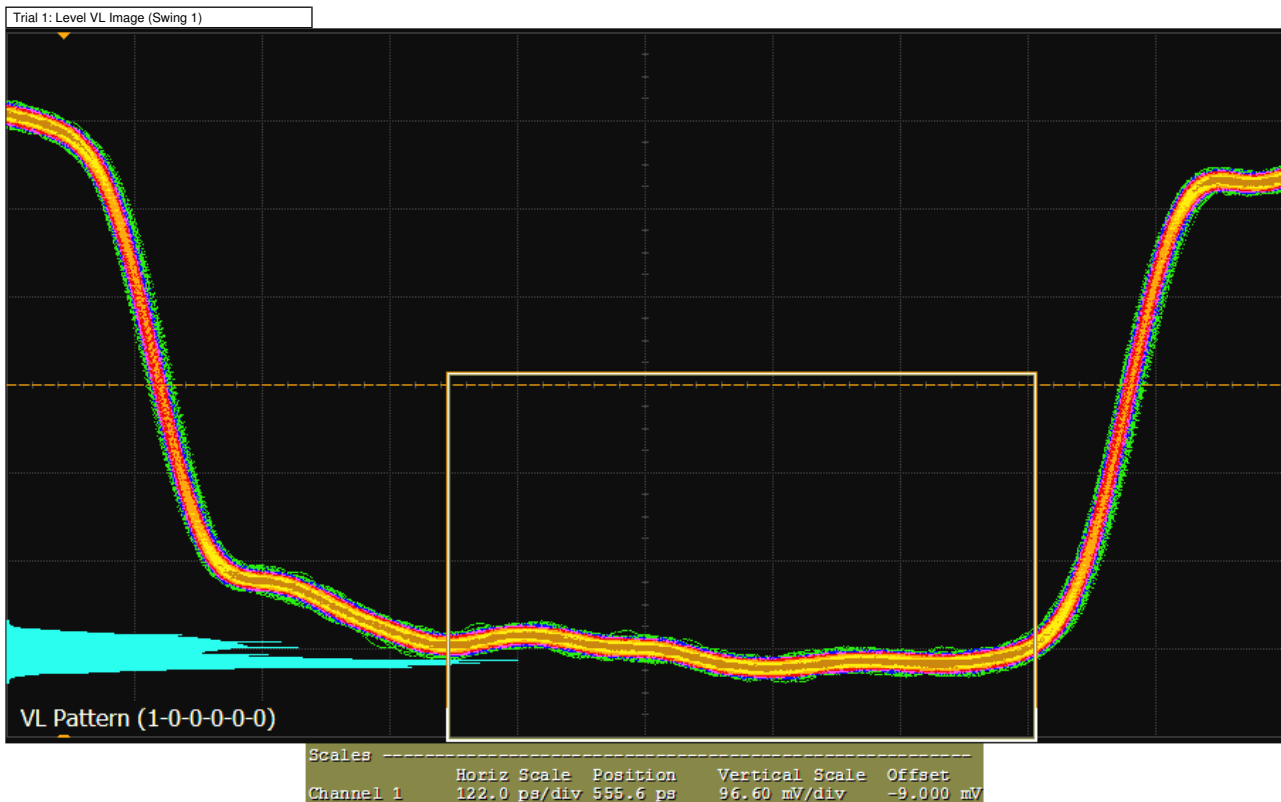




Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	130.0 mV/div	-9.200 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	96.60 mV/div	-9.000 mV



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✓ Lane 1 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

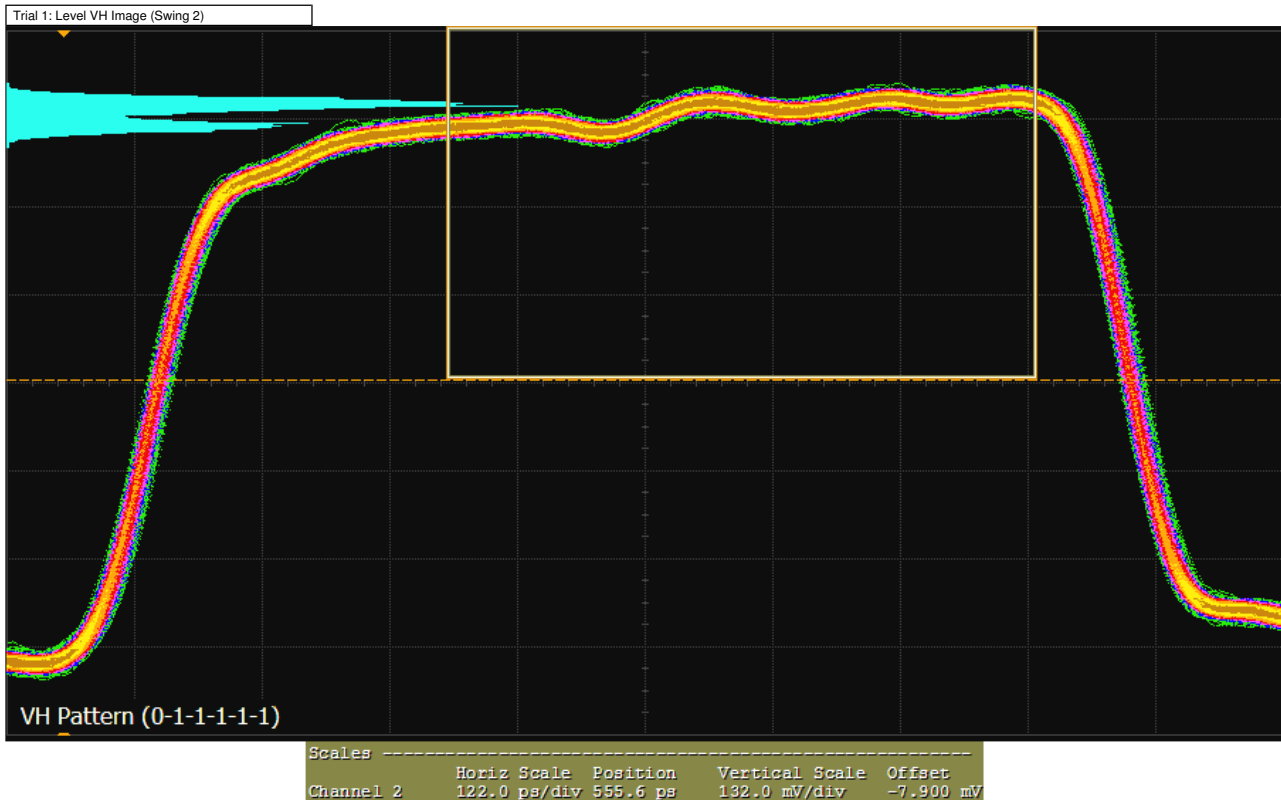
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

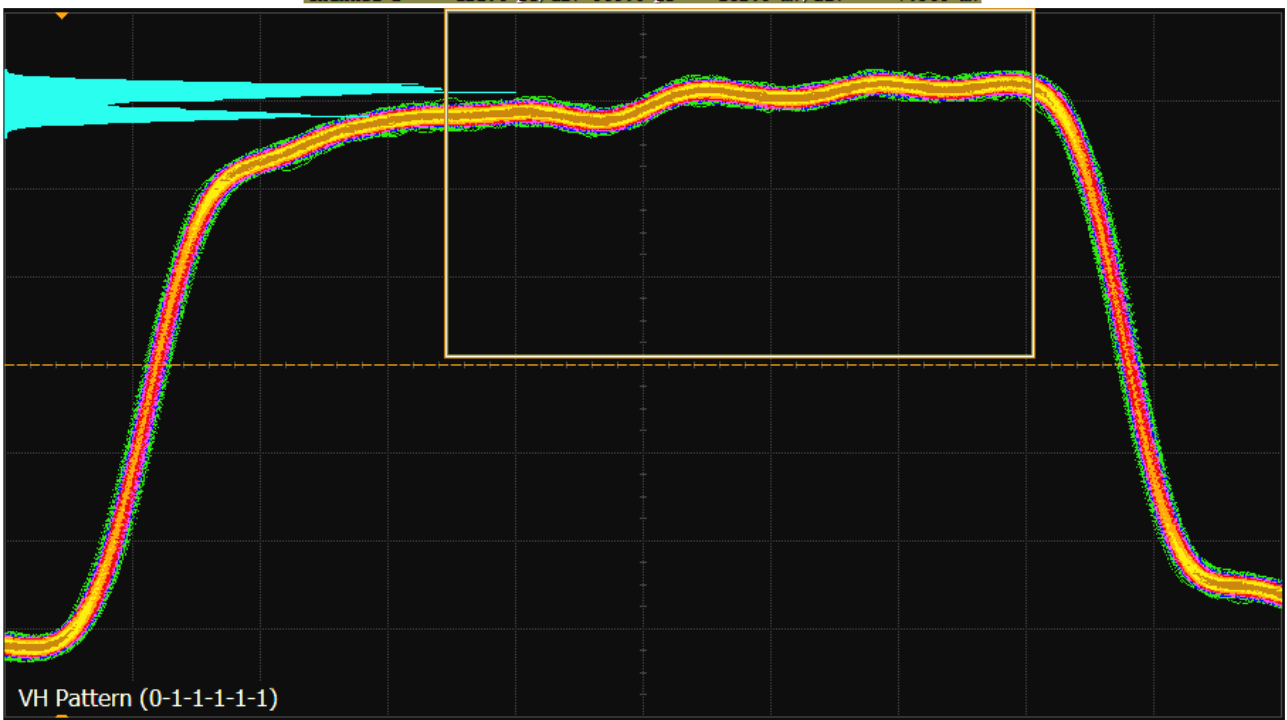
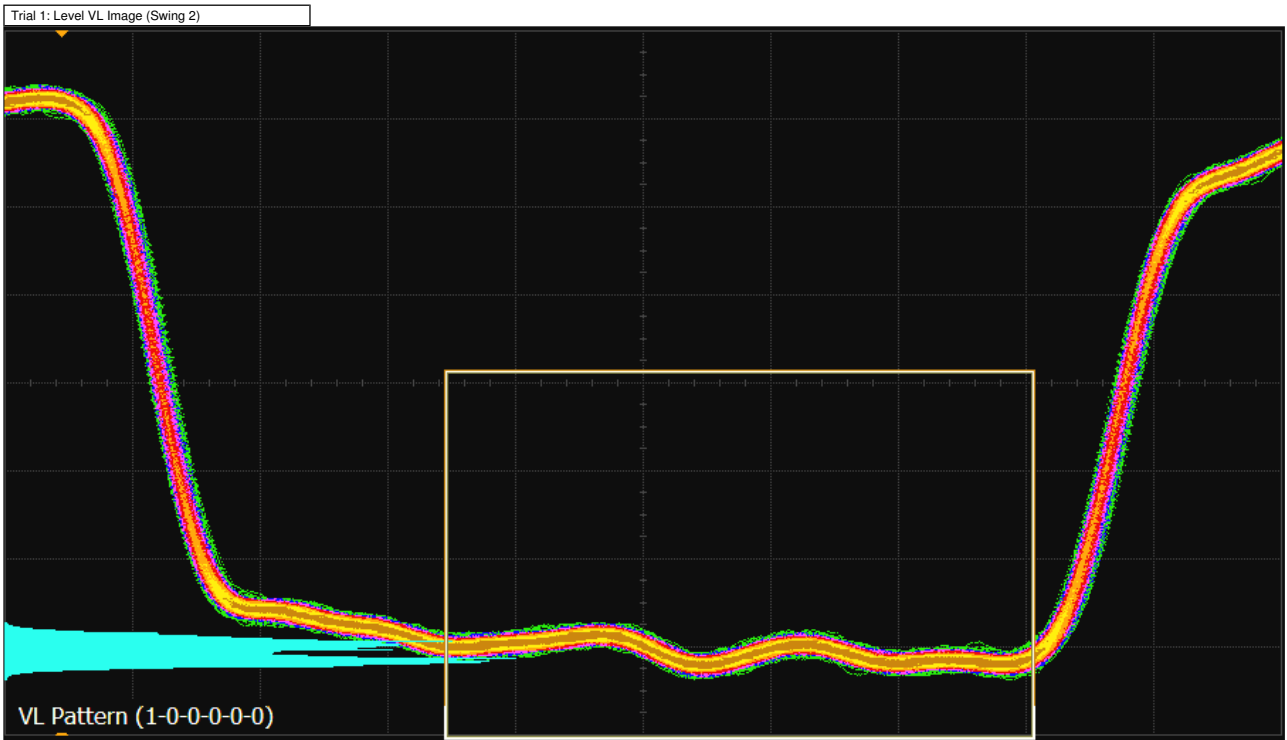
Pass Limits: [5.2000 dB to 6.9000 dB] Lane 1 Non-PreEmphasis Level Test (Swing 2/Swing 0) 5.6800 dB

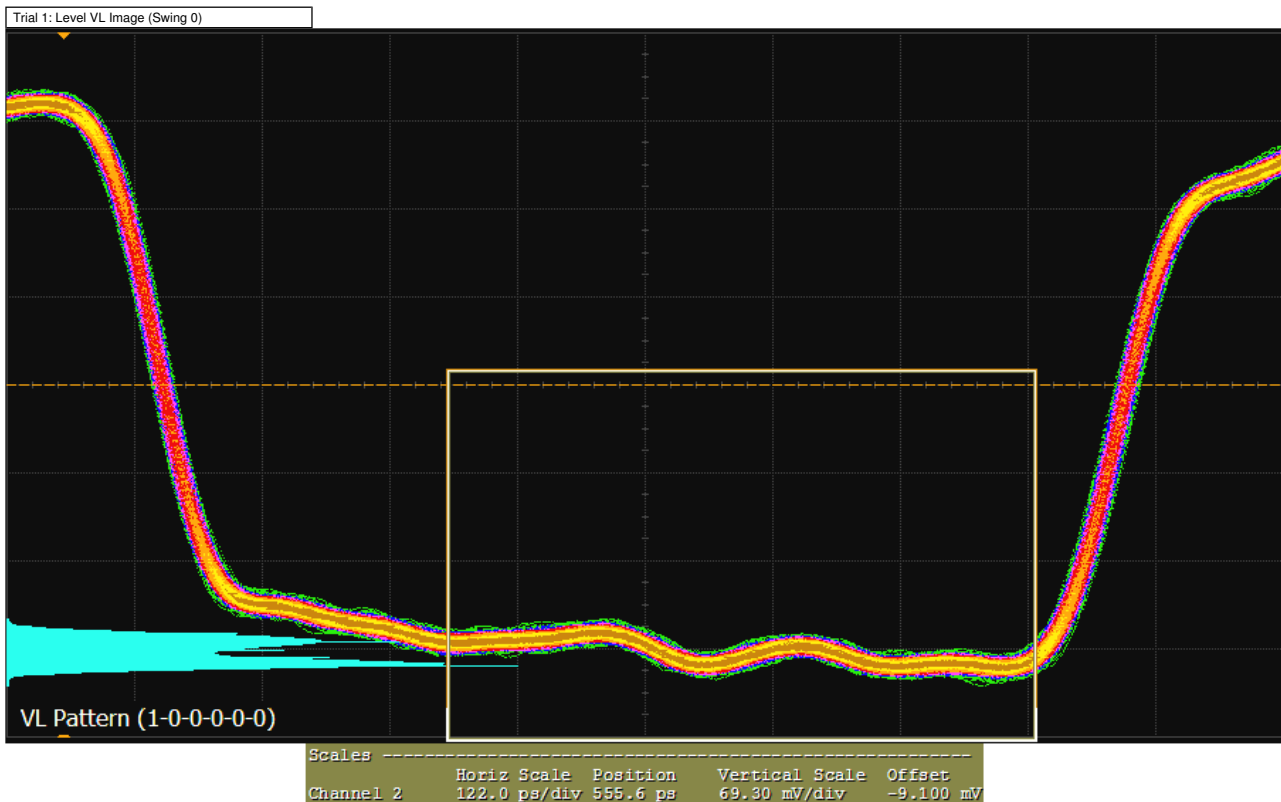
Result Details

Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Level VH Image (Swing 0) (See image)	Level VL Image (Swing 0) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 2) 381.989 mV	VBase (Swing 2) -403.042 mV	VSwing (Swing 2) 785.031 mV
VTop (Swing 0) 194.318 mV	VBase (Swing 0) -213.893 mV	VSwing (Swing 0) 408.211 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 2	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

Trial 1







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✓ Lane 1 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

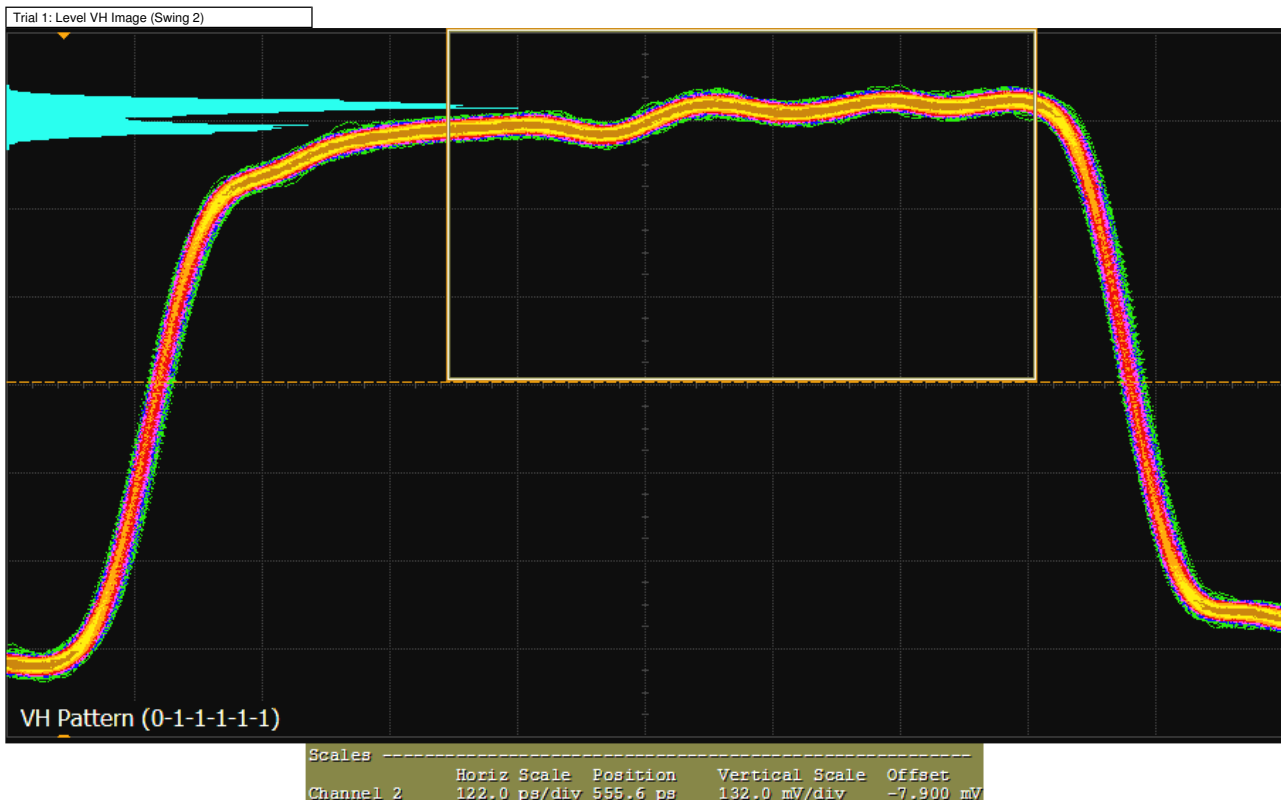
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

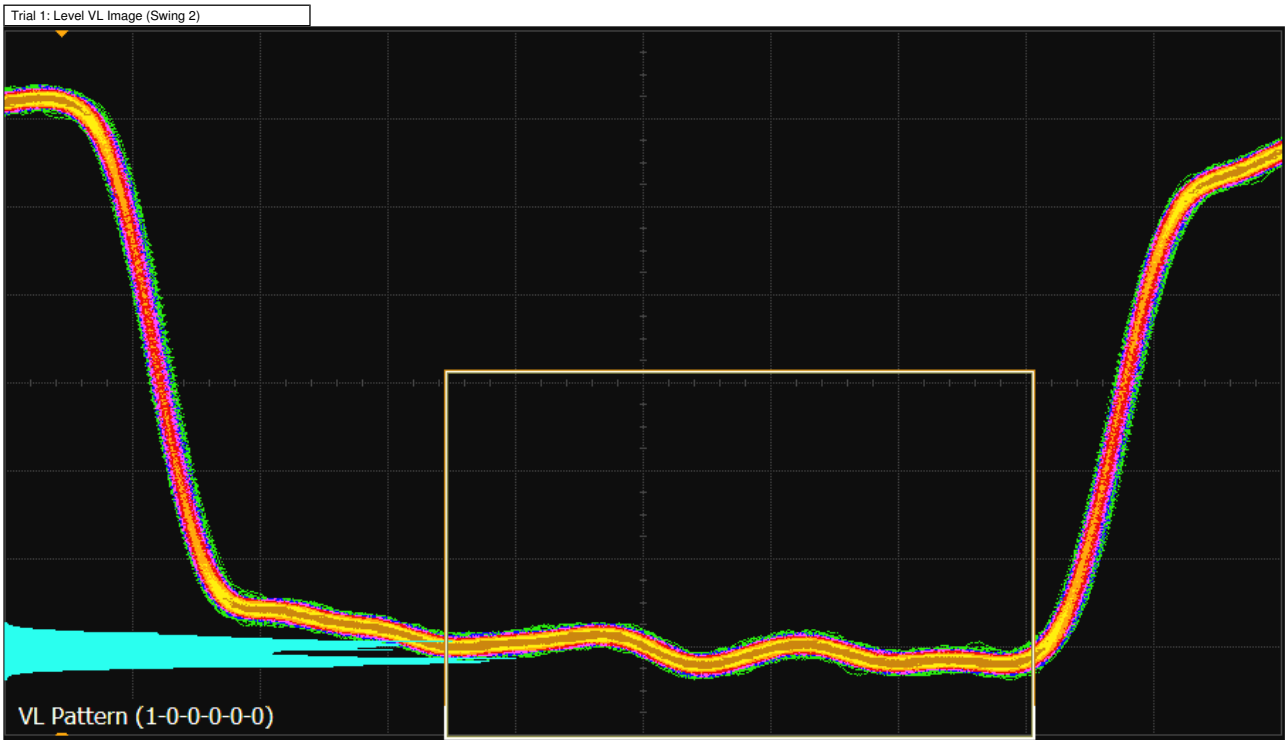
Pass Limits: [1.6000 dB to 3.5000 dB] Lane 1 Non-PreEmphasis Level Test (Swing 2/Swing 1) 2.6135 dB

Result Details

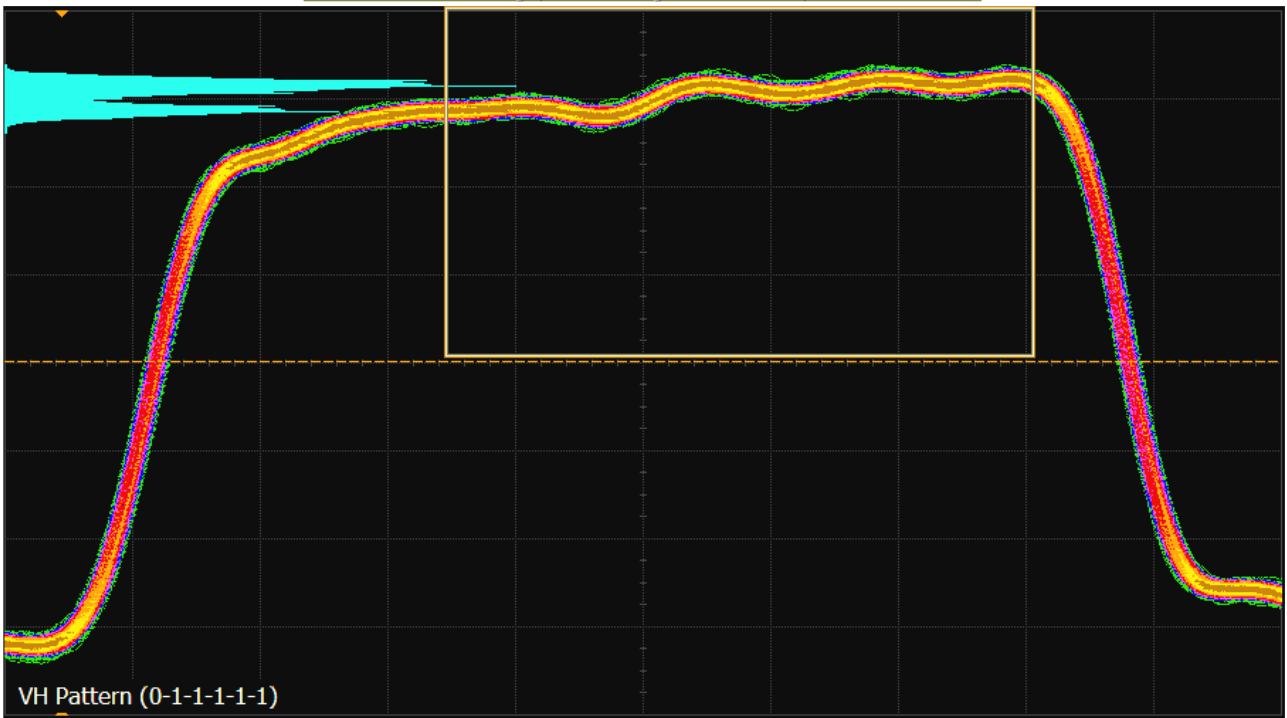
Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Level VH Image (Swing 1) (See image)	Level VL Image (Swing 1) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 2) 381.989 mV	VBase (Swing 2) -403.042 mV	VSwing (Swing 2) 785.031 mV
VTop (Swing 1) 279.833 mV	VBase (Swing 1) -301.213 mV	VSwing (Swing 1) 581.046 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 2	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

Trial 1

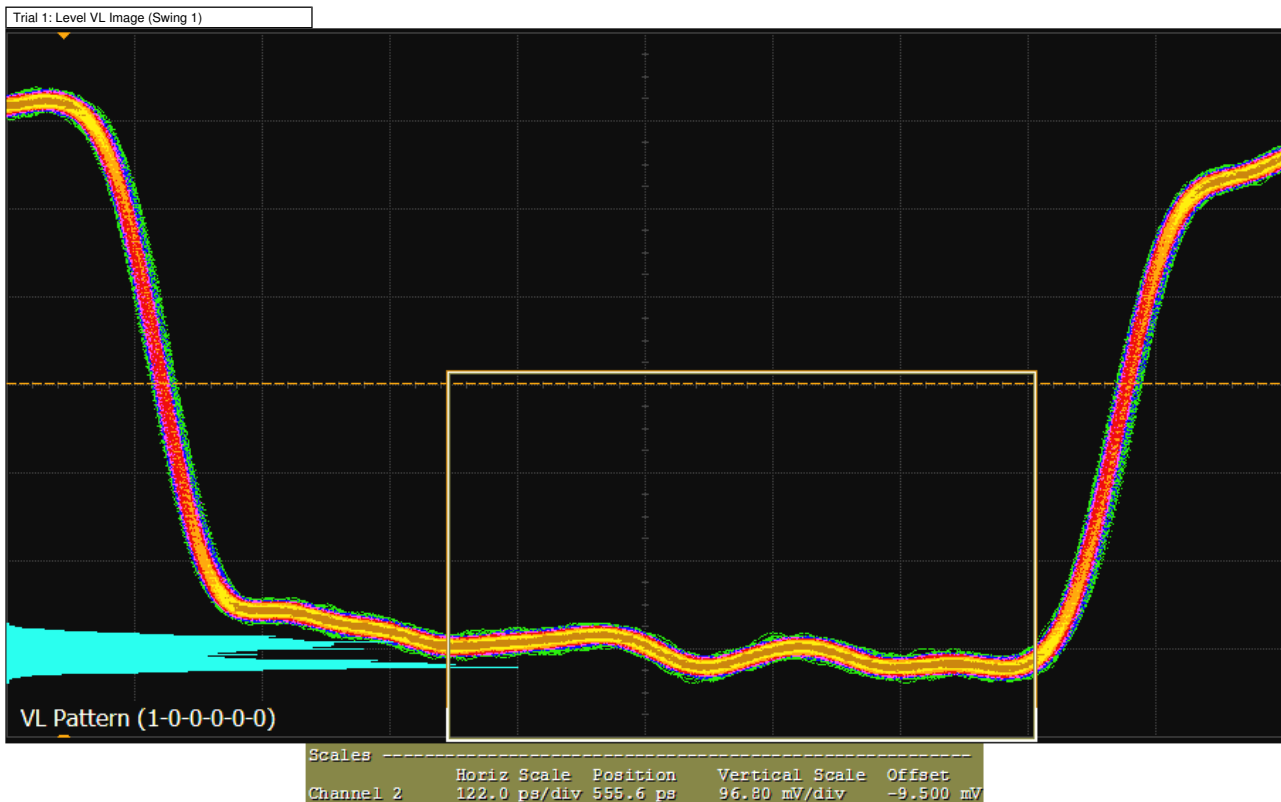




Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	132.0 mV/div	-7.900 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	96.80 mV/div	-9.500 mV



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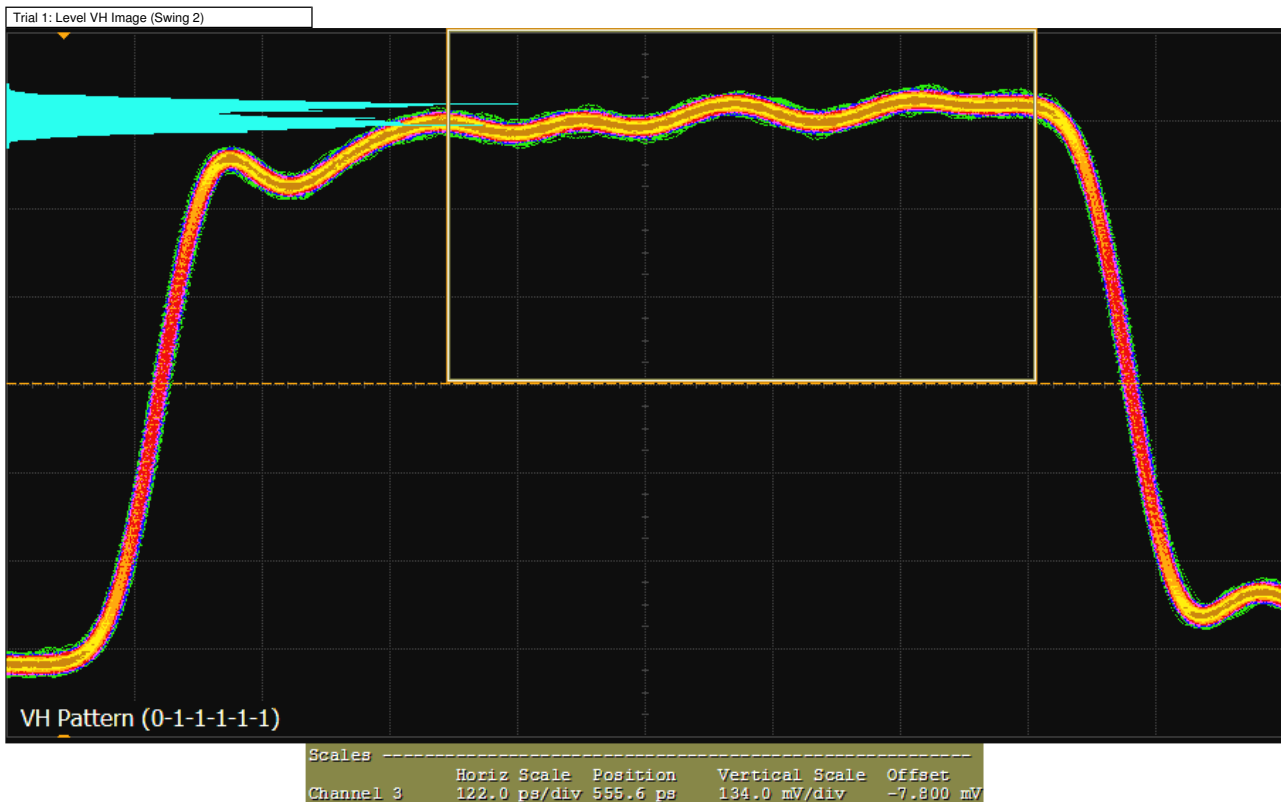
✓ Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
Pass Limits: [5.2000 dB to 6.9000 dB] Lane 2 Non-PreEmphasis Level Test (Swing 2/Swing 0) 5.4931 dB

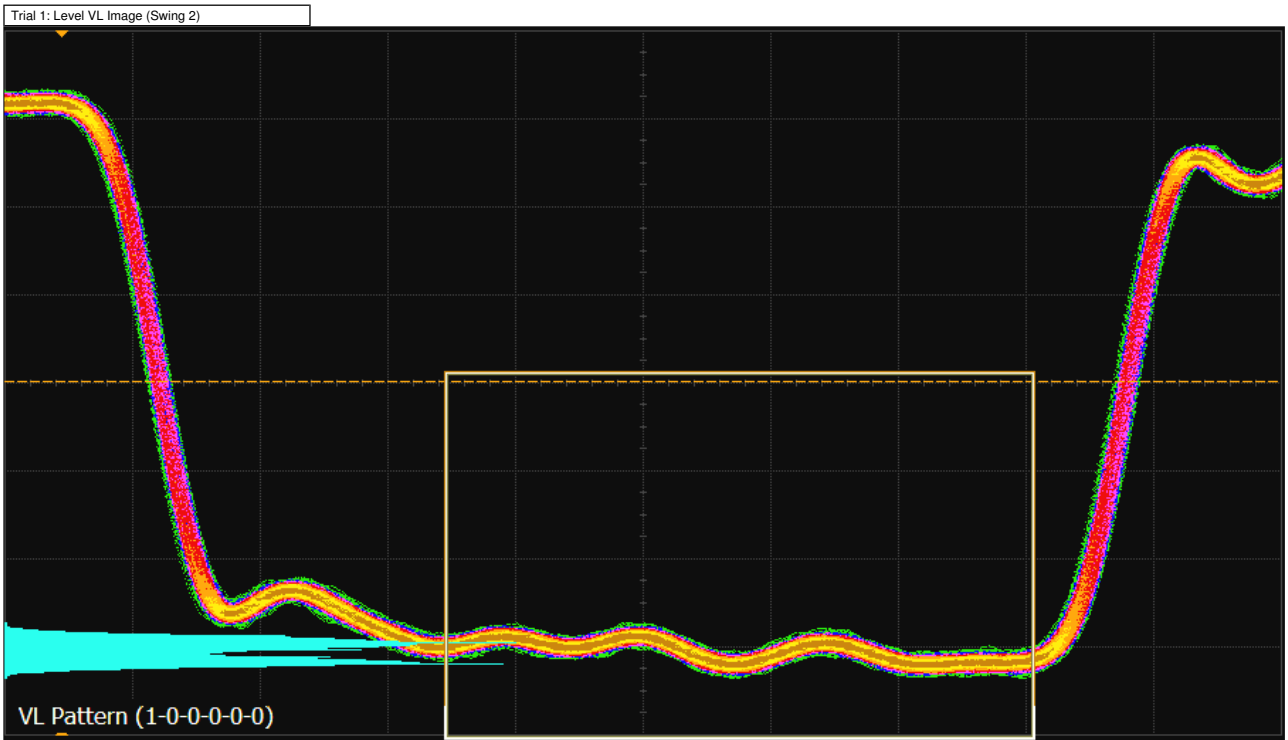
Result Details

Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Level VH Image (Swing 0) (See image)	Level VL Image (Swing 0) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 2) 389.754 mV	VBase (Swing 2) -410.343 mV	VSwing (Swing 2) 800.097 mV
VTop (Swing 0) 203.827 mV	VBase (Swing 0) -221.268 mV	VSwing (Swing 0) 425.095 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 2	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

Trial 1







Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	134.0 mV/div	-7.800 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	70.40 mV/div	-7.800 mV





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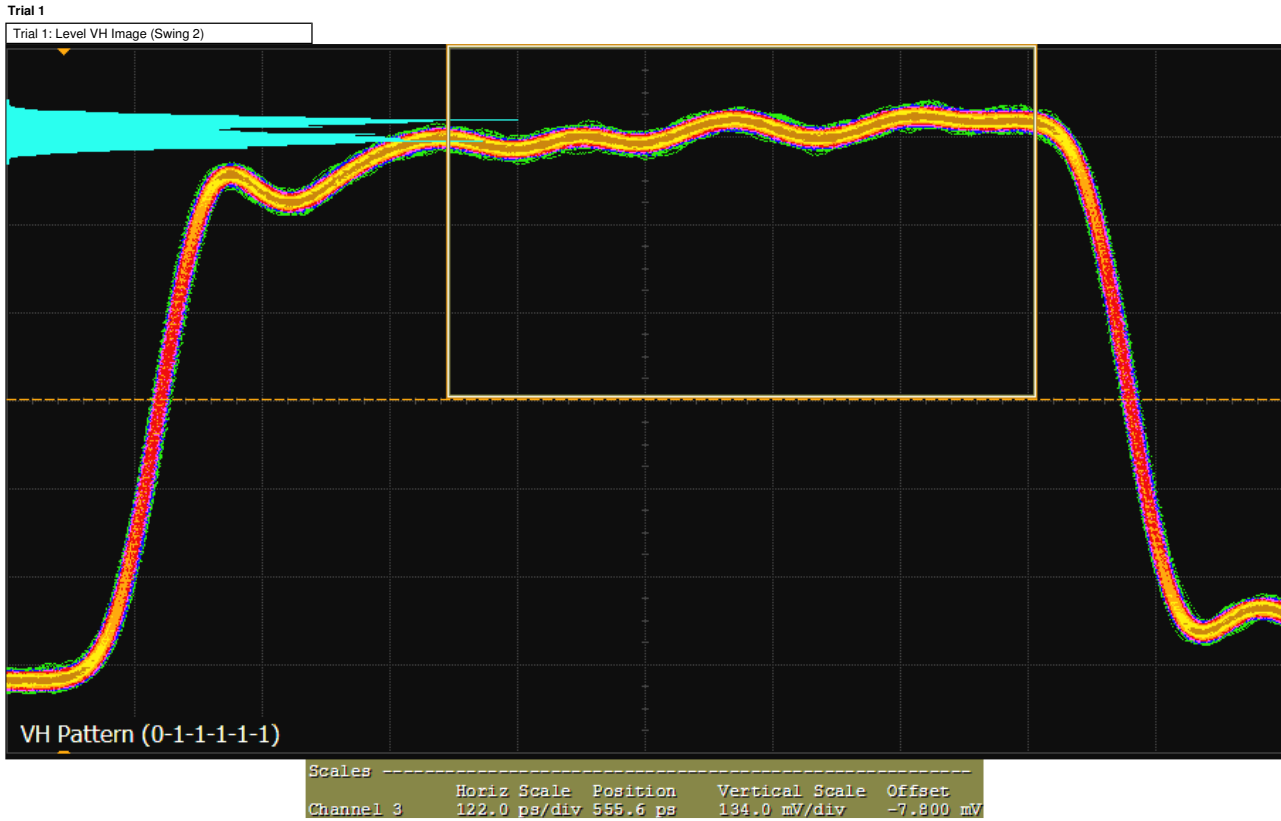
✓ Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

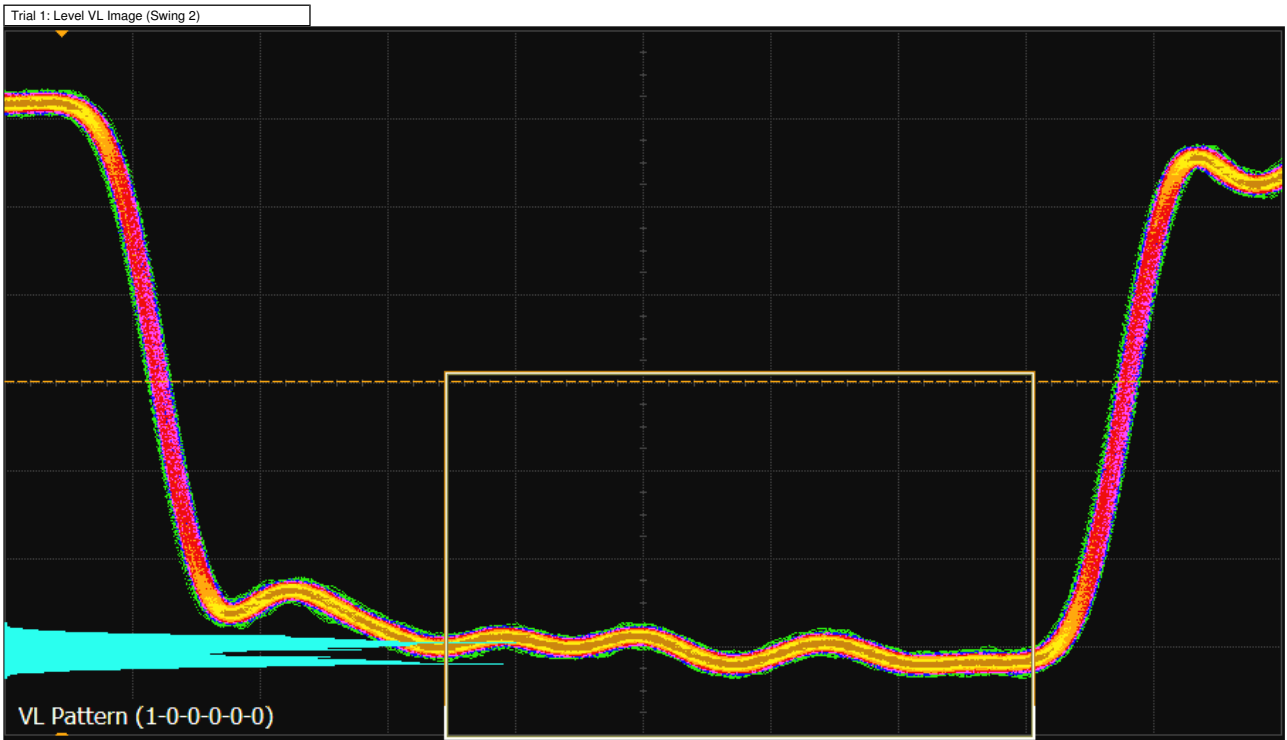
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Pass Limits: [1.6000 dB to 3.5000 dB] Lane 2 Non-PreEmphasis Level Test (Swing 2/Swing 1) 2.5816 dB

**Result Details**

Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Level VH Image (Swing 1) (See image)	Level VL Image (Swing 1) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 2) 389.754 mV	VBase (Swing 2) -410.343 mV	VSwing (Swing 2) 800.097 mV
VTop (Swing 1) 287.727 mV	VBase (Swing 1) -306.648 mV	VSwing (Swing 1) 594.375 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 2	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

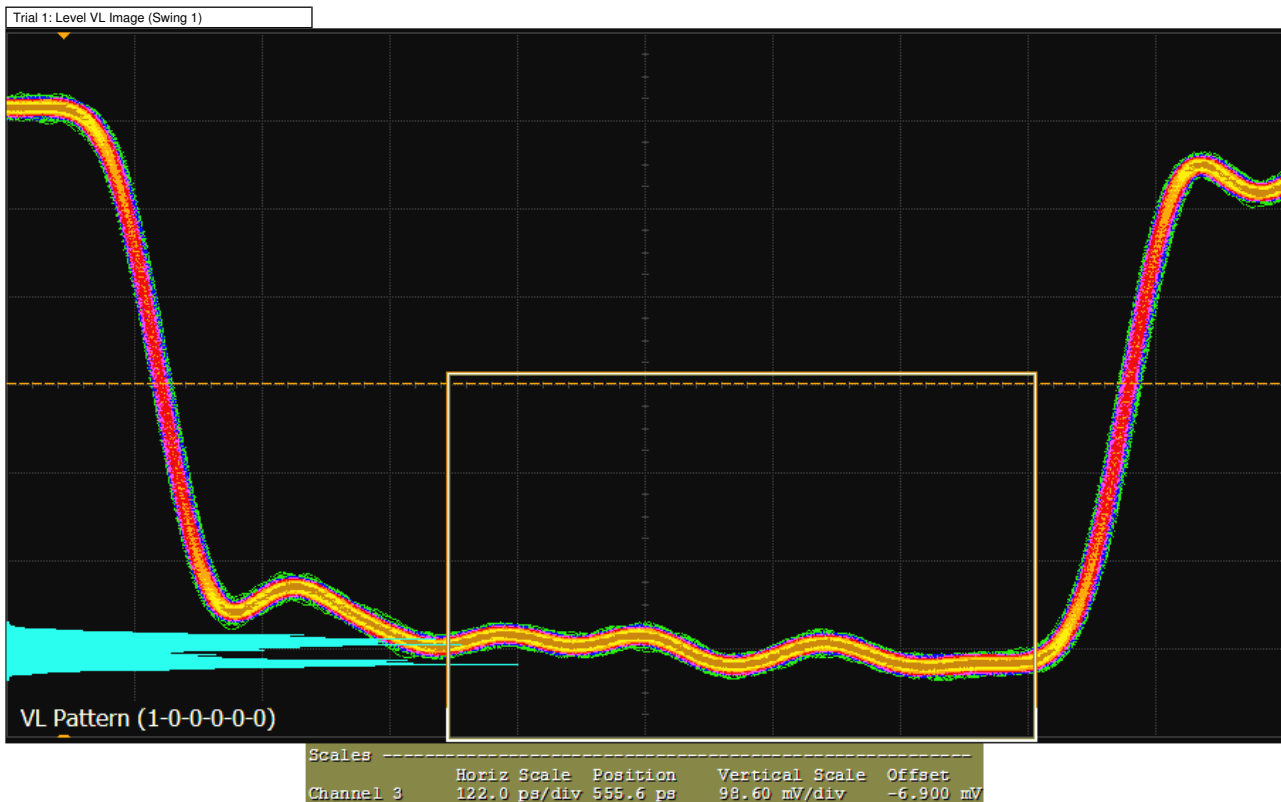




Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	134.0 mV/div	-7.800 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	98.60 mV/div	-6.900 mV



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✓ Lane 3 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

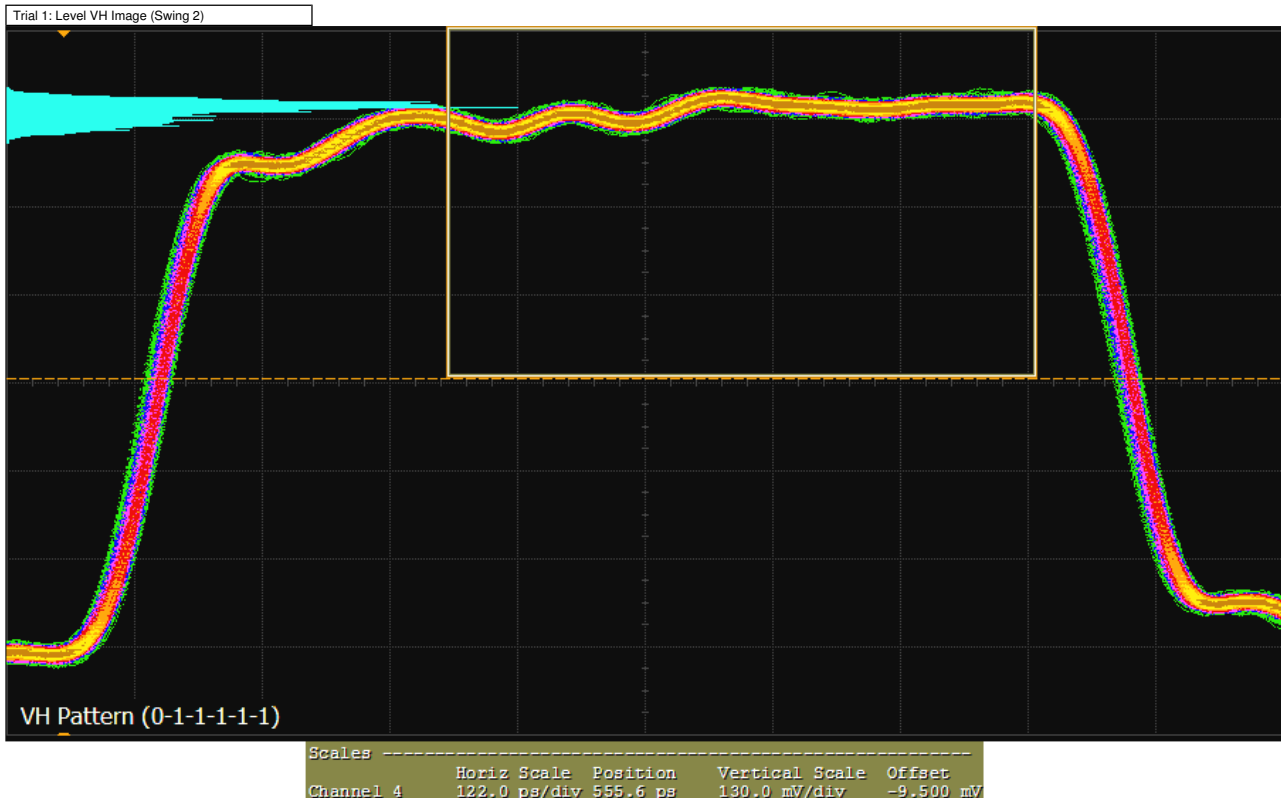
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Pass Limits: [5.2000 dB to 6.9000 dB] Lane 3 Non-PreEmphasis Level Test (Swing 2/Swing 0) 5.9114 dB

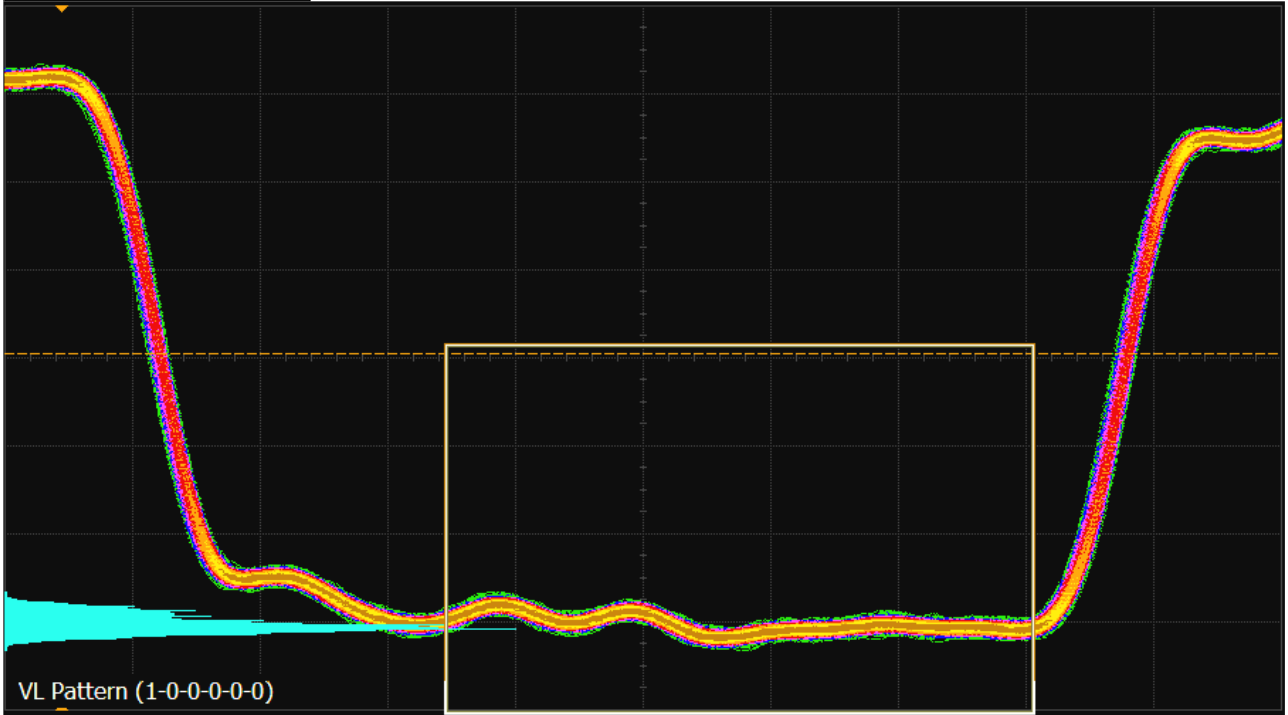
Result Details

Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Level VH Image (Swing 0) (See image)	Level VL Image (Swing 0) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 2) 386.243 mV	VBase (Swing 2) -408.020 mV	VSwing (Swing 2) 794.263 mV
VTop (Swing 0) 192.181 mV	VBase (Swing 0) -209.976 mV	VSwing (Swing 0) 402.157 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 2	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

Trial 1



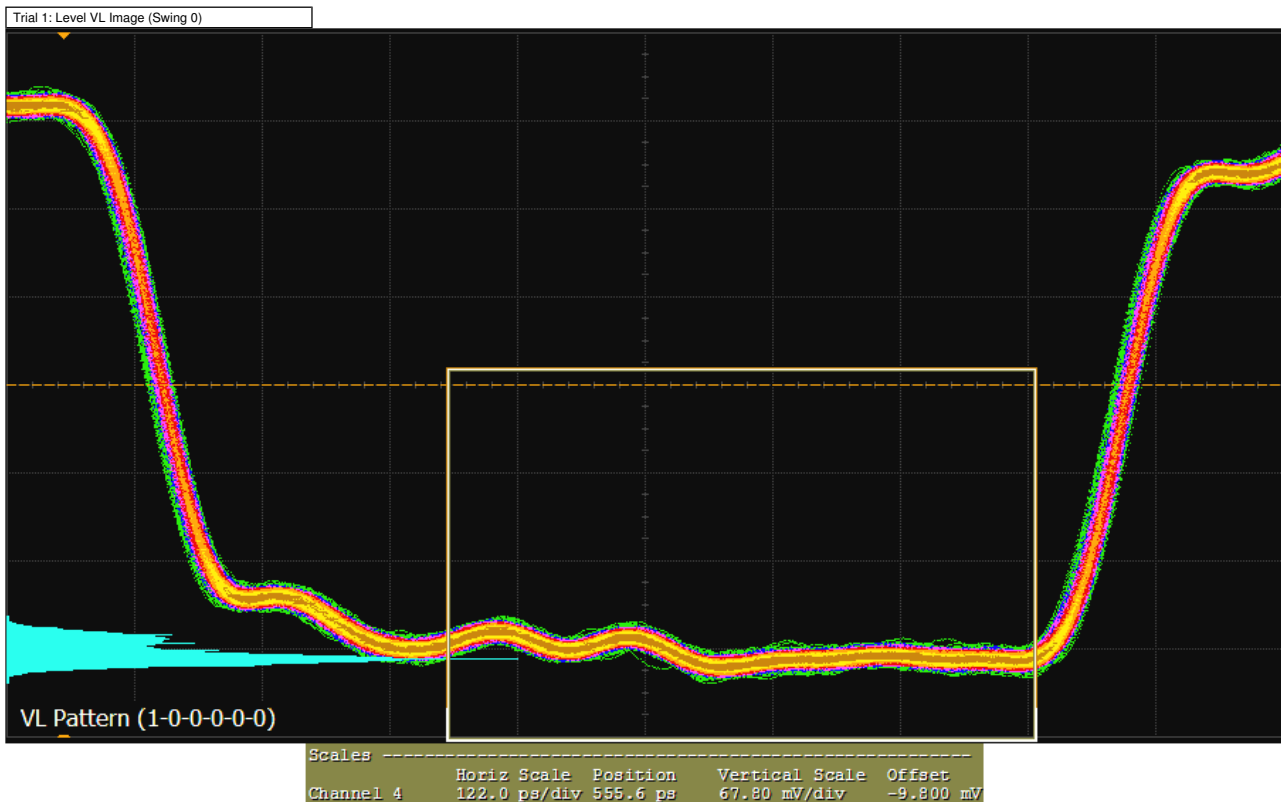
Trial 1: Level VL Image (Swing 2)



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	122.0 ps/div	555.6 ps	130.0 mV/div	-9.500 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	122.0 ps/div	555.6 ps	67.80 mV/div	-9.800 mV



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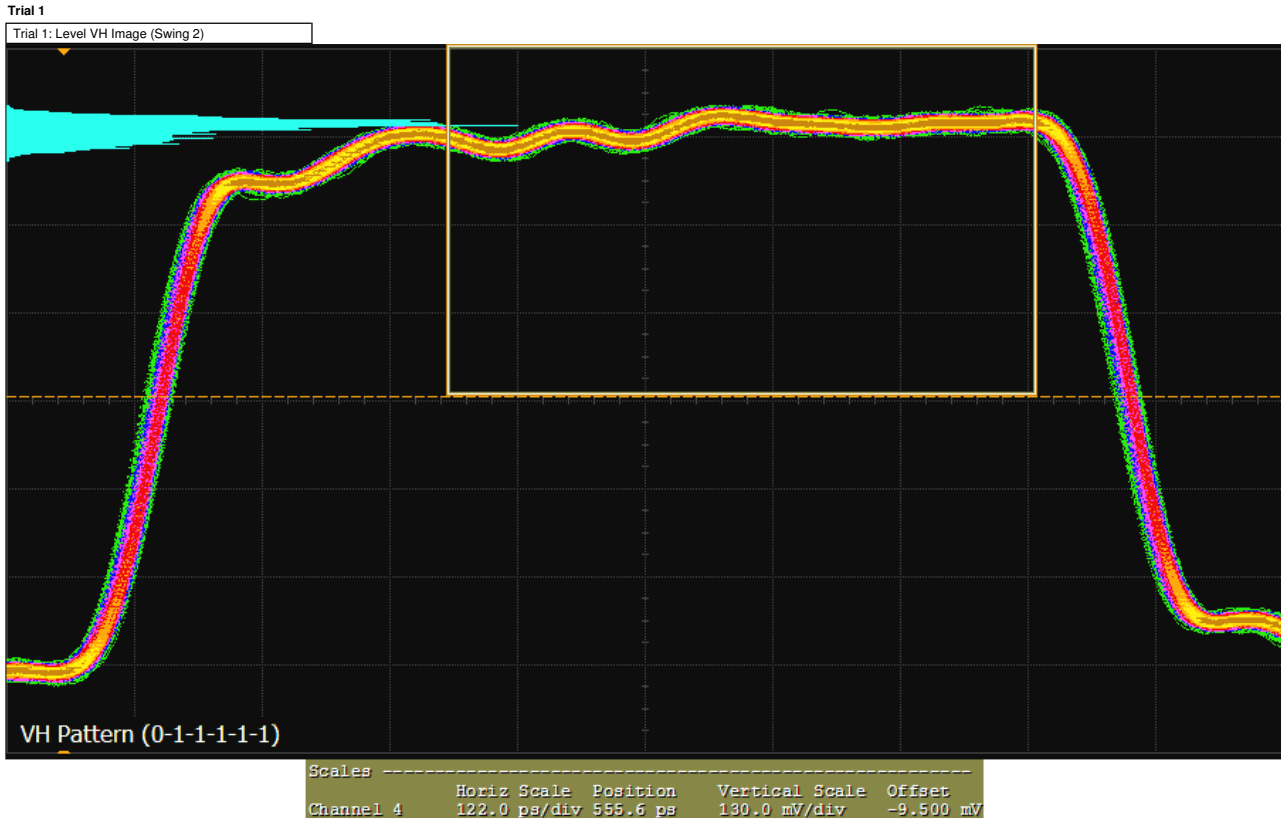
✓ Lane 3 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

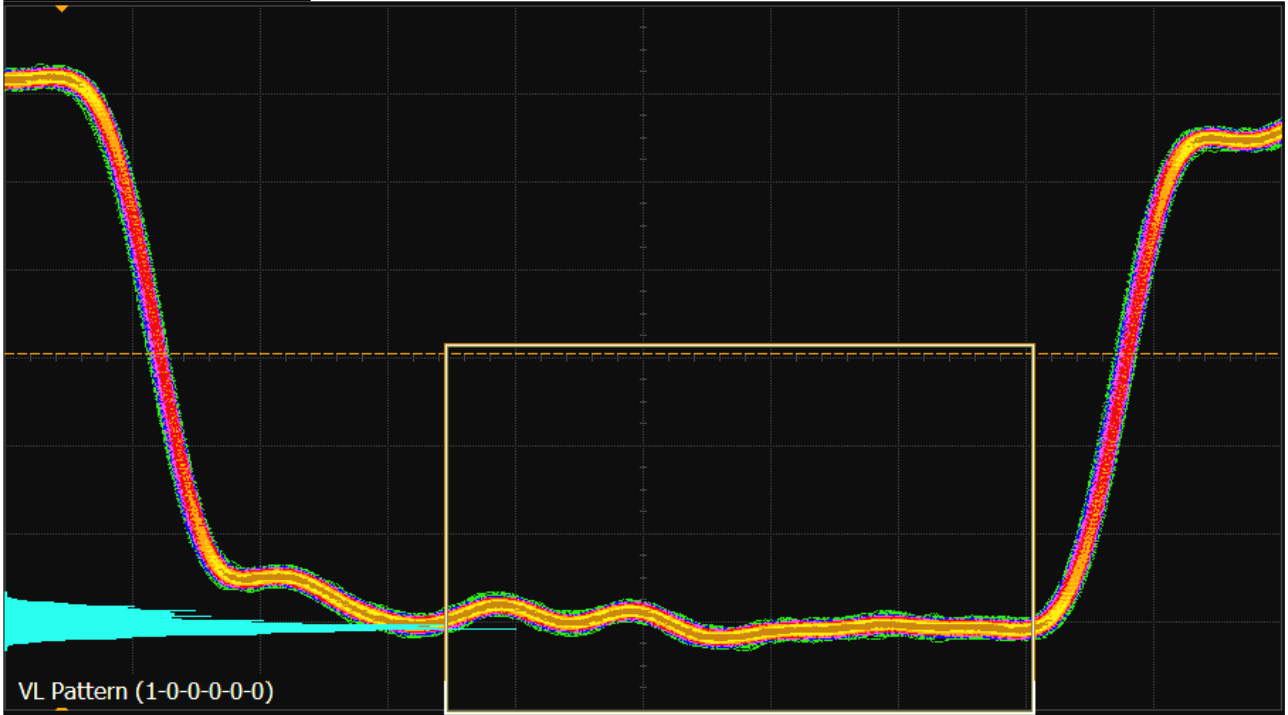
Pass Limits: [1.6000 dB to 3.5000 dB] Lane 3 Non-PreEmphasis Level Test (Swing 2/Swing 1) 2.7417 dB

**Result Details**

<a href="#">Level VH Image (Swing 2)</a> (See image)	<a href="#">Level VL Image (Swing 2)</a> (See image)	<a href="#">Level VH Image (Swing 1)</a> (See image)	<a href="#">Level VL Image (Swing 1)</a> (See image)	<b>Number of UI</b> 1000
<b>VH Trigger Pattern</b> 011111	<b>VL Trigger Pattern</b> 100000	<b>VTop (Swing 2)</b> 386.243 mV	<b>VBase (Swing 2)</b> -408.020 mV	<b>VSwing (Swing 2)</b> 794.263 mV
<b>VTop (Swing 1)</b> 279.623 mV	<b>VBase (Swing 1)</b> -299.647 mV	<b>VSwing (Swing 1)</b> 579.270 mV	<b>Test Mode</b> Compliance	<b>Test Layer</b> Physical Layer Tests
<b>Test Condition</b> Compliance Conditions Only	<b>DUT Type</b> Source	<b>Test Type</b> Differential Tests	<b>Connection Type</b> Differential Probe	<b>BitRate</b> 5.4 Gbps
<b>Level</b> Swing 2	<b>PreEmphasis</b> Pre-emphasis 0	<b>SSC</b> SSC Disabled	<b>PostCursor2</b> Level 0	



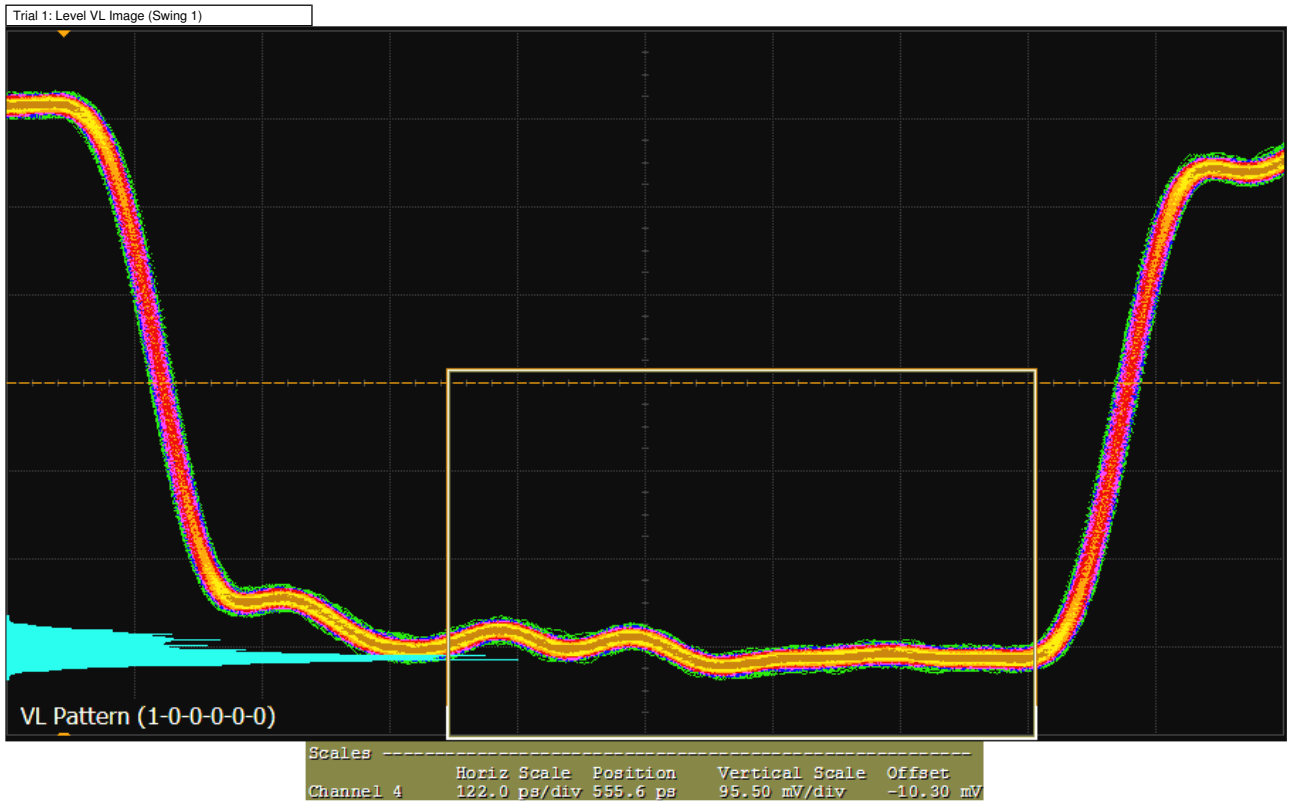
Trial 1: Level VL Image (Swing 2)



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	122.0 ps/div	555.6 ps	130.0 mV/div	-9.500 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	122.0 ps/div	555.6 ps	95.50 mV/div	-10.30 mV



✓ Lane 0 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

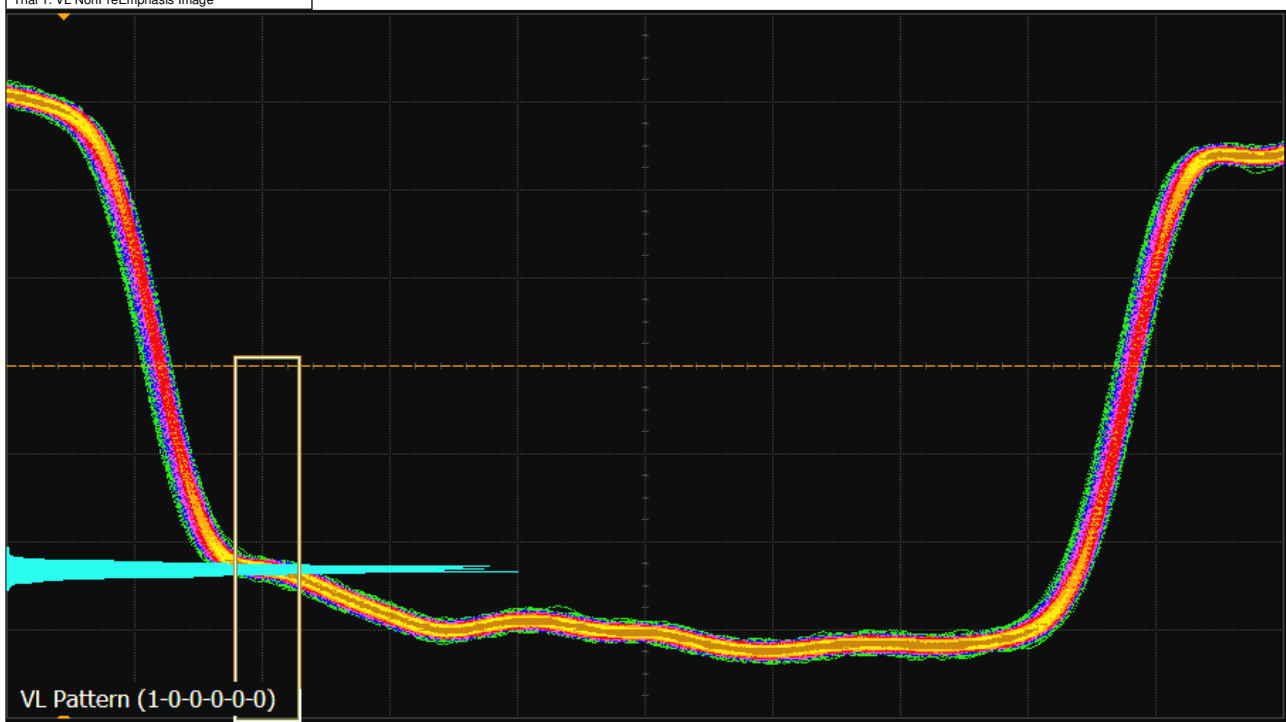
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: <= 250 mdB PreEmphasis (Pre-emphasis 0) (Worst of 4 Trials) -2.285 dB # Trials Run: 4 Worst Trial: Trial 1

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-2.439 dB	1.076 k%											
	StdDev	157.6 mdB	63.12 %											
	Range	344.3 mdB	138.0 %											
	Min	-2.630 dB	1.014 k%											
	Max	-2.285 dB	1.152 k%											
	Sum	-9.755 dB	4.302 k%											
✓	Trial 1 (Worst)	-2.285 dB	101E+01% (See image)	(See image)	(See image)	1000	606.696 mV	789.302 mV	-2.285 dB	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-2.503 dB	110E+01% (See image)	(See image)	(See image)	1000	433.772 mV	578.674 mV	-2.503 dB	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-2.630 dB	115E+01% (See image)	(See image)	(See image)	1000	301.332 mV	407.879 mV	-2.630 dB	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	-2.337 dB	103E+01% (See image)	(See image)	(See image)	1000	756.095 mV	989.497 mV	-2.337 dB	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

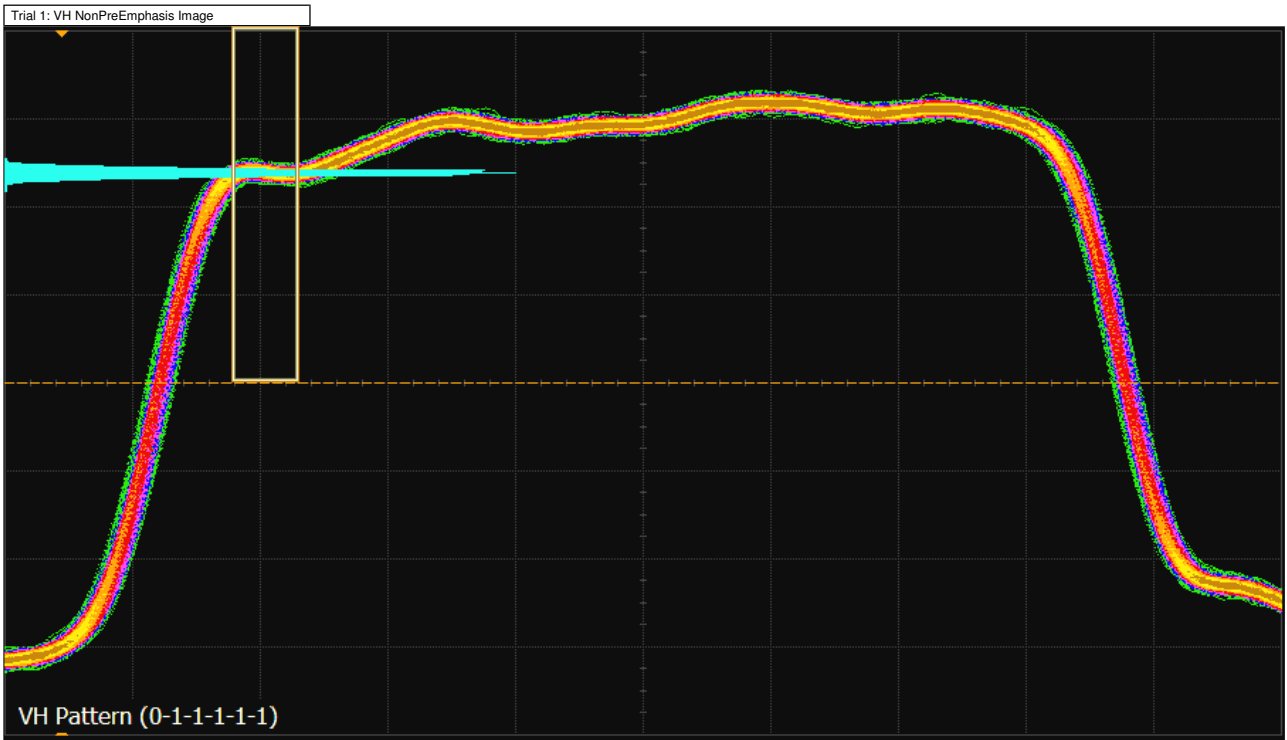
Trial 1

Trial 1: VL NonPreEmphasis Image

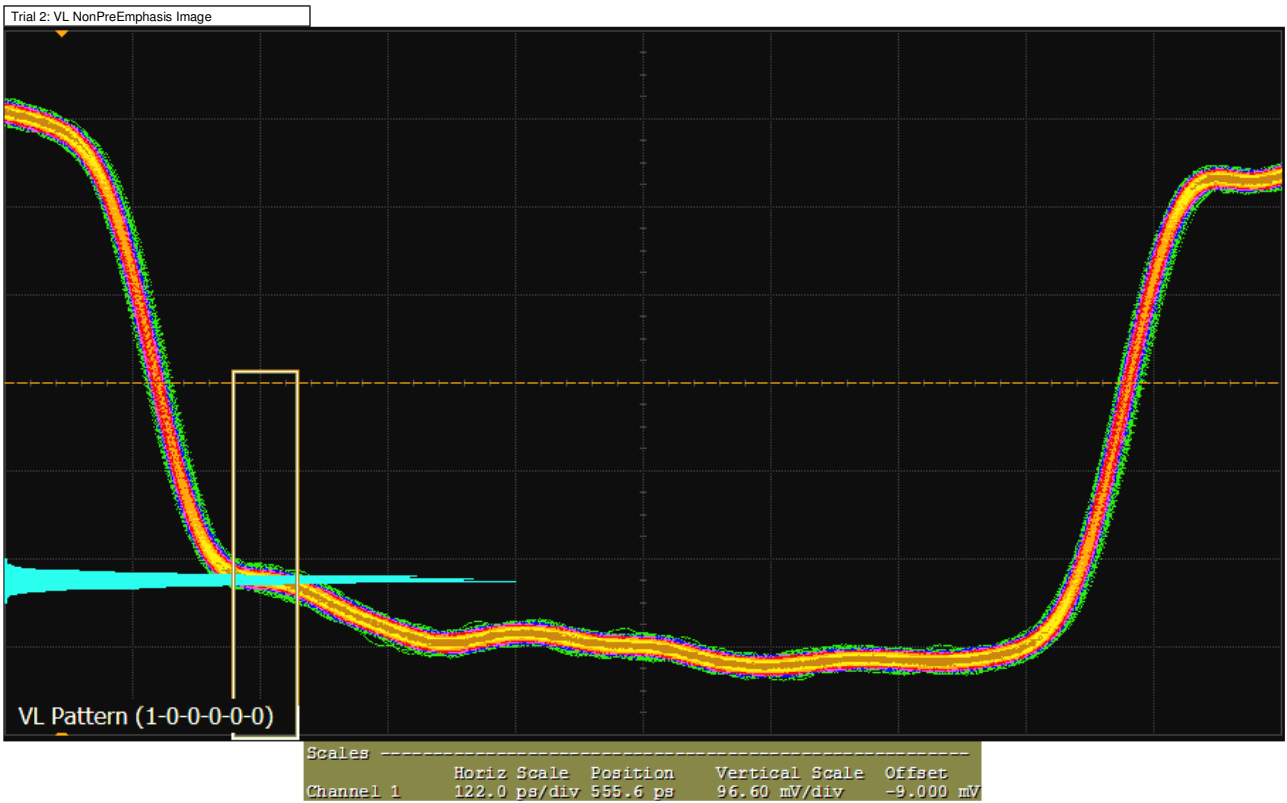


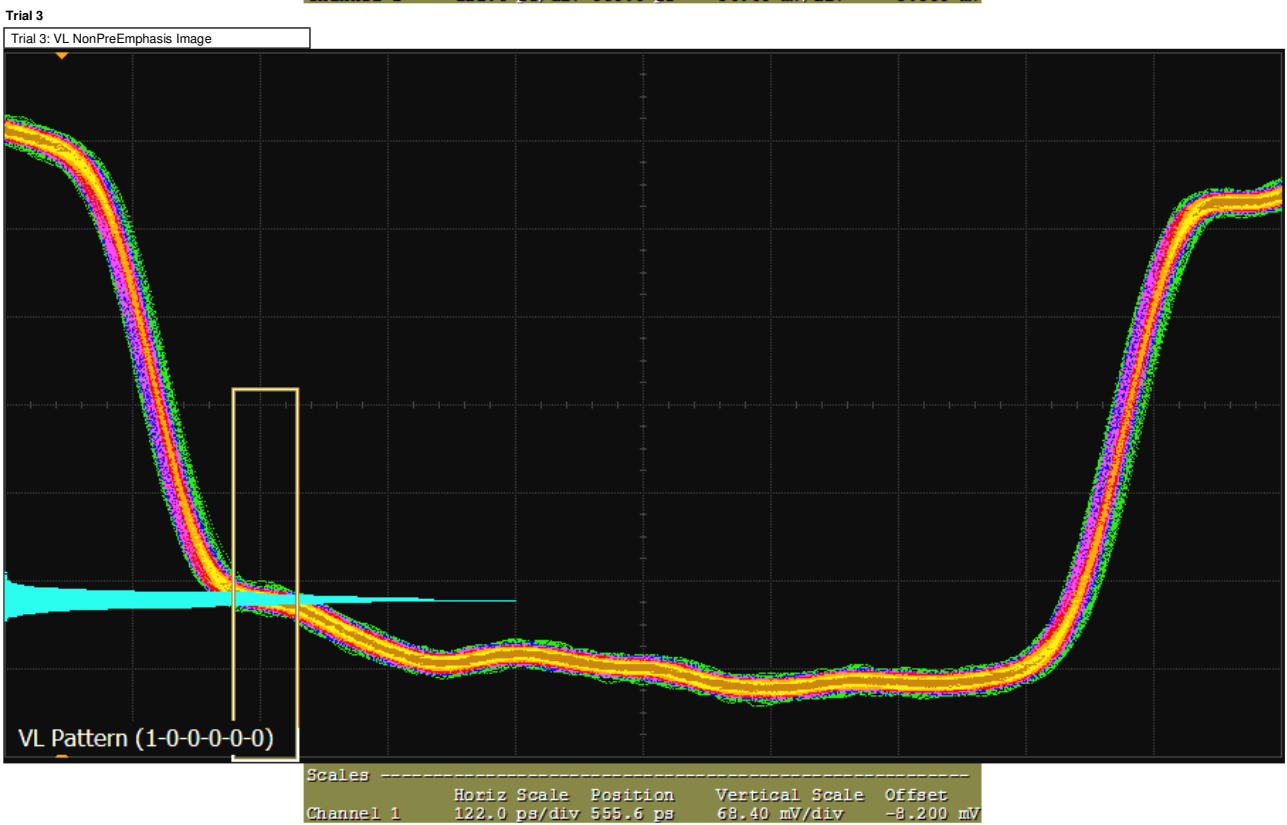
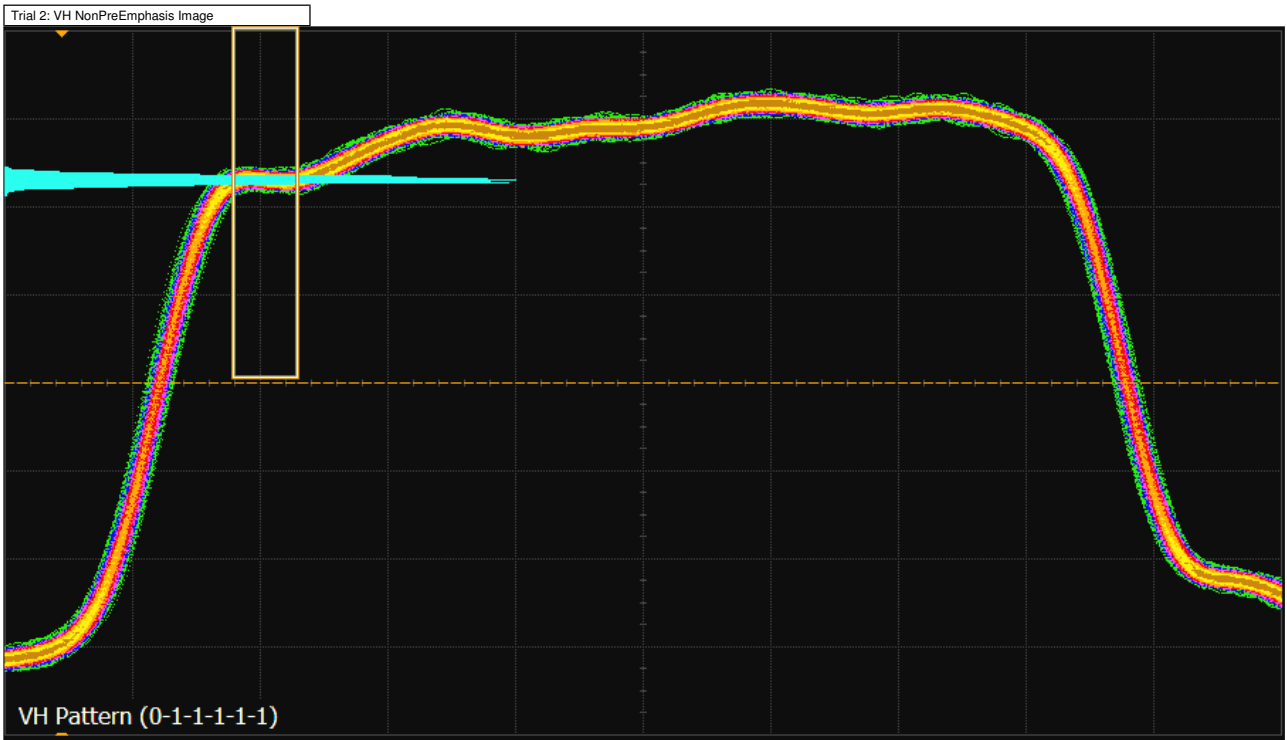
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	122.0 ps/div	555.6 ps	130.0 mV/div	-9.200 mV

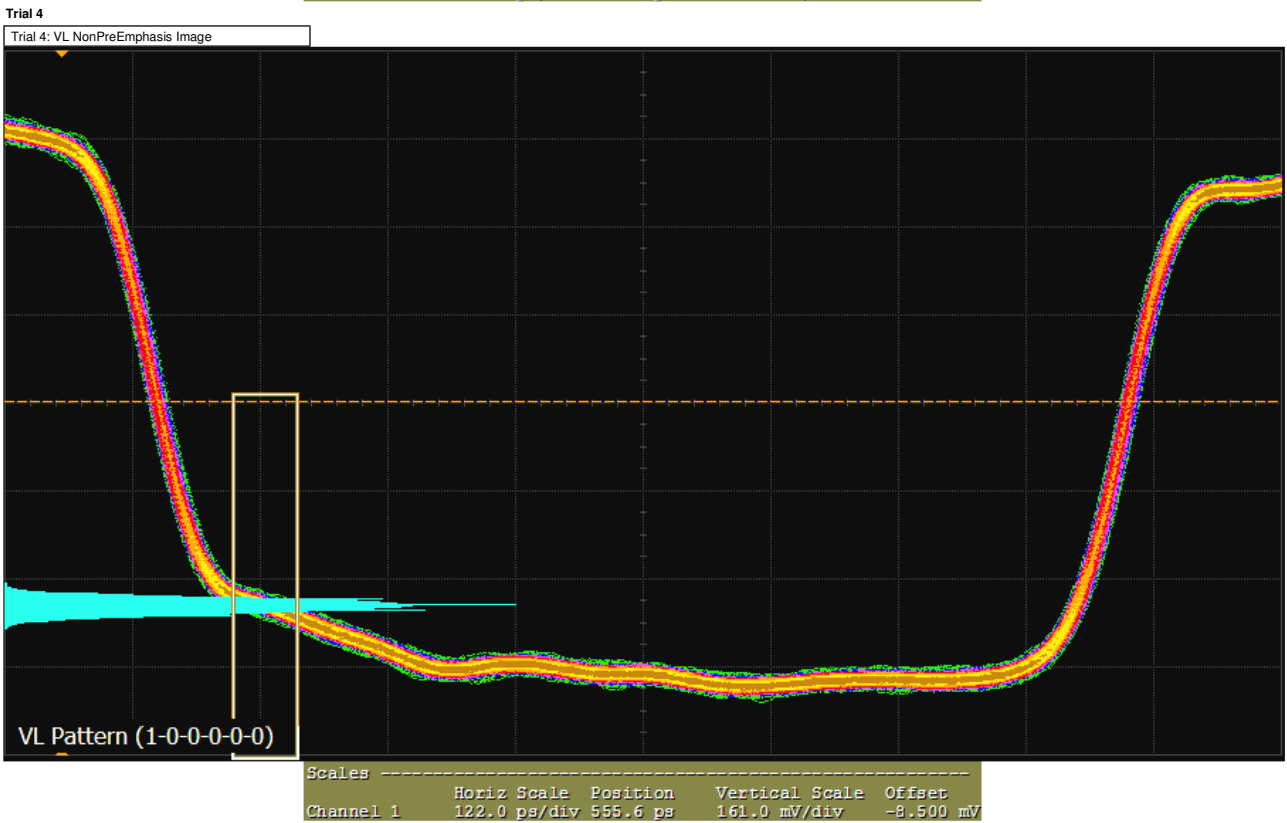
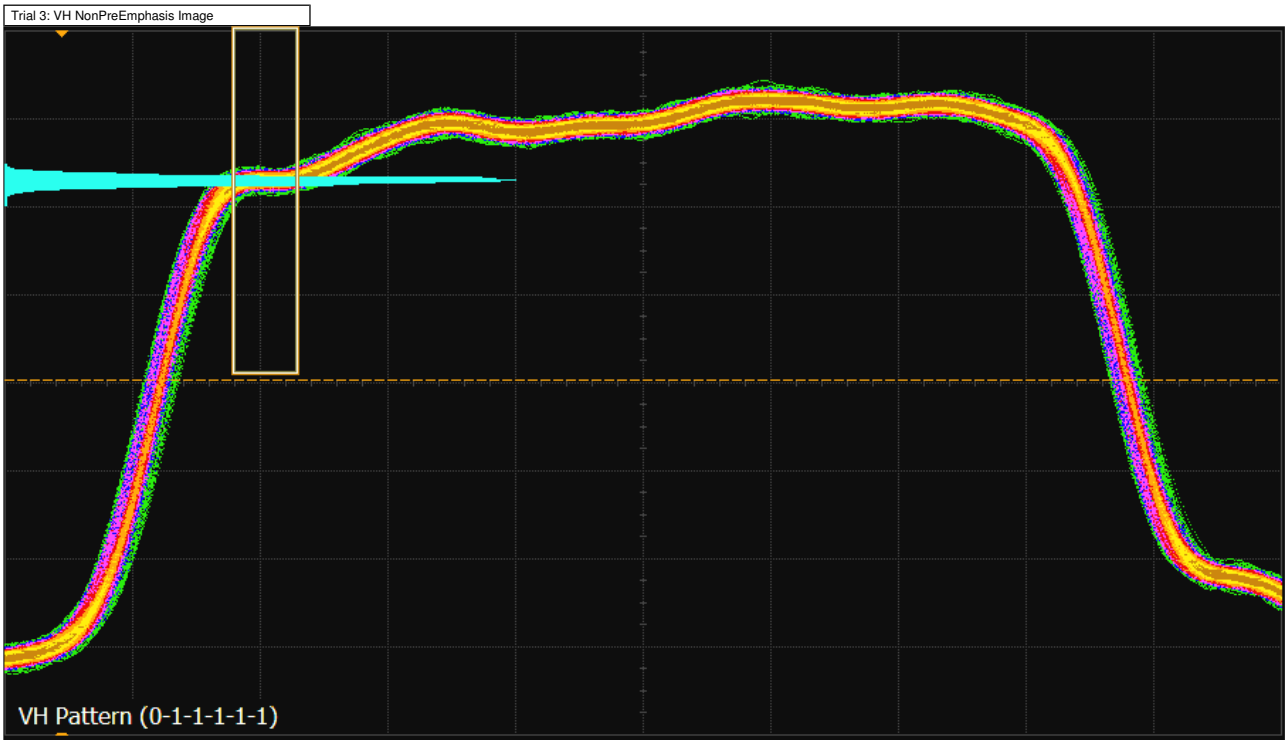


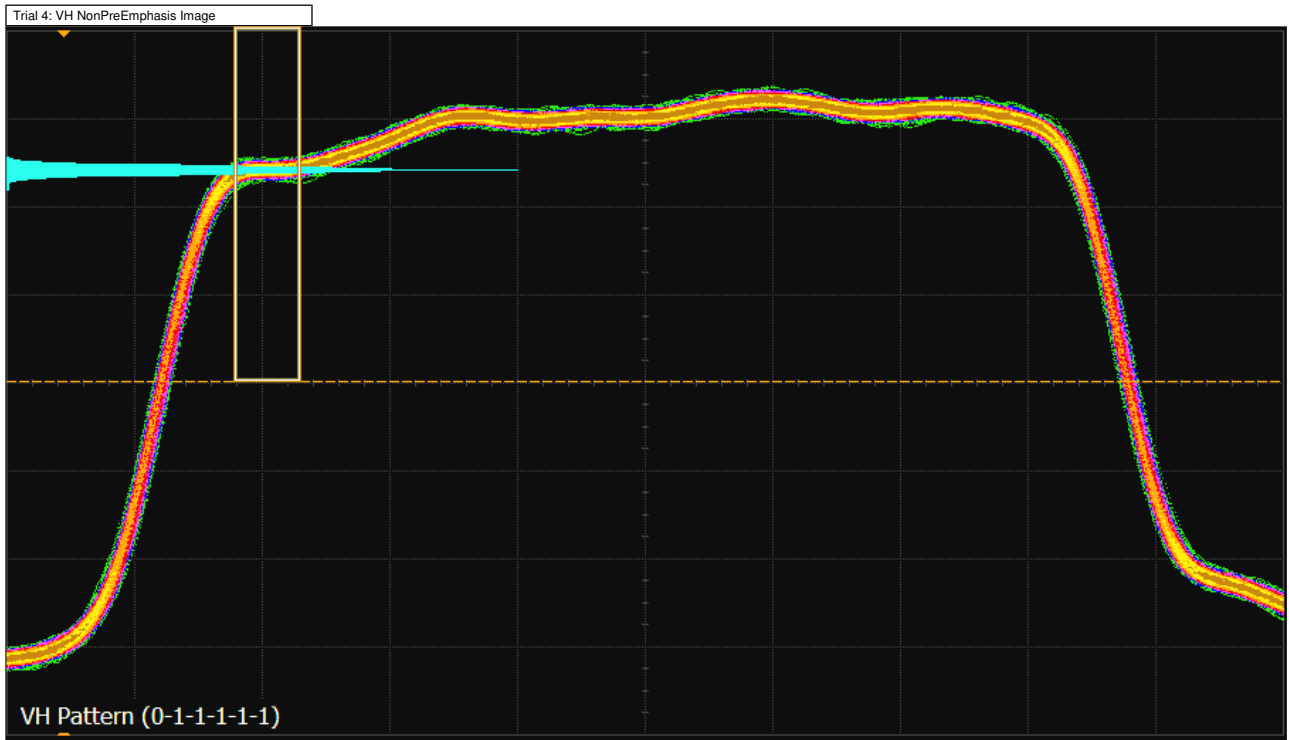


Trial 2









Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	161.0 mV/div	-8.500 mV

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✓ Lane 1 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

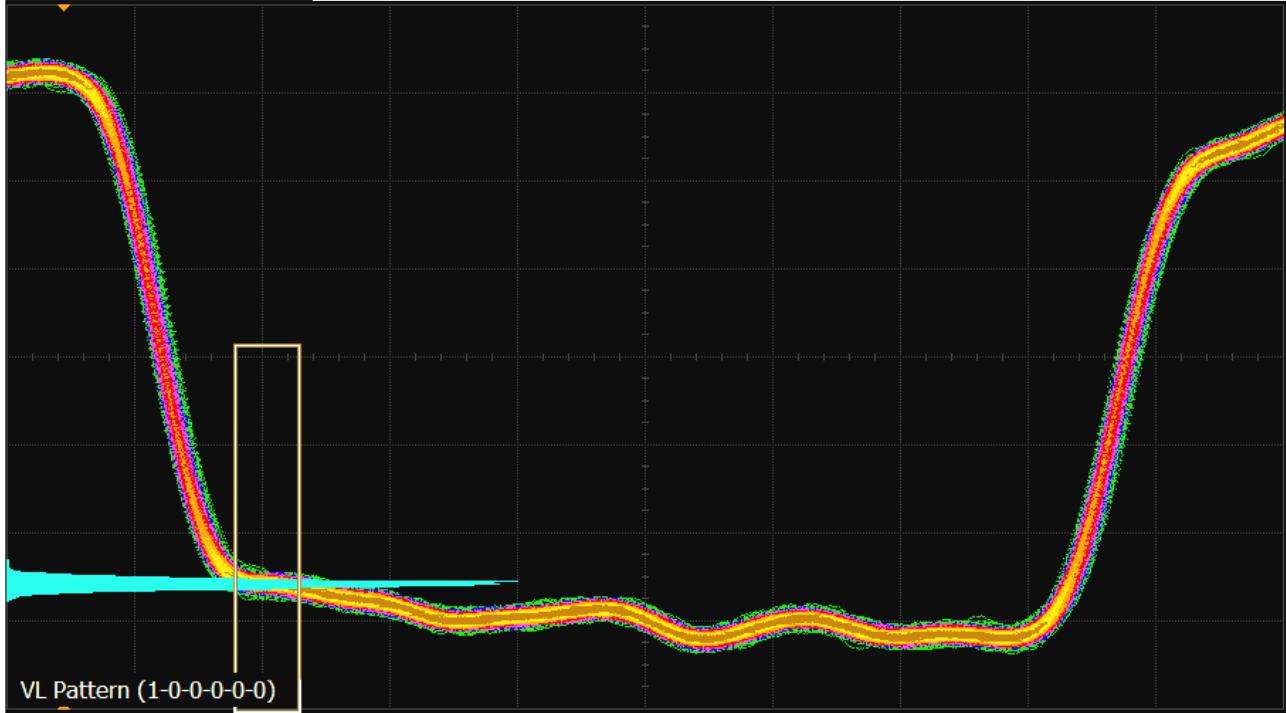
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: <= 250 mdB PreEmphasis(Pre-emphasis 0) (Worst of 4 Trials) -1.541 dB # Trials Run: 4 Worst Trial: Trial 4

Overall Summary + details of 4 worst trials

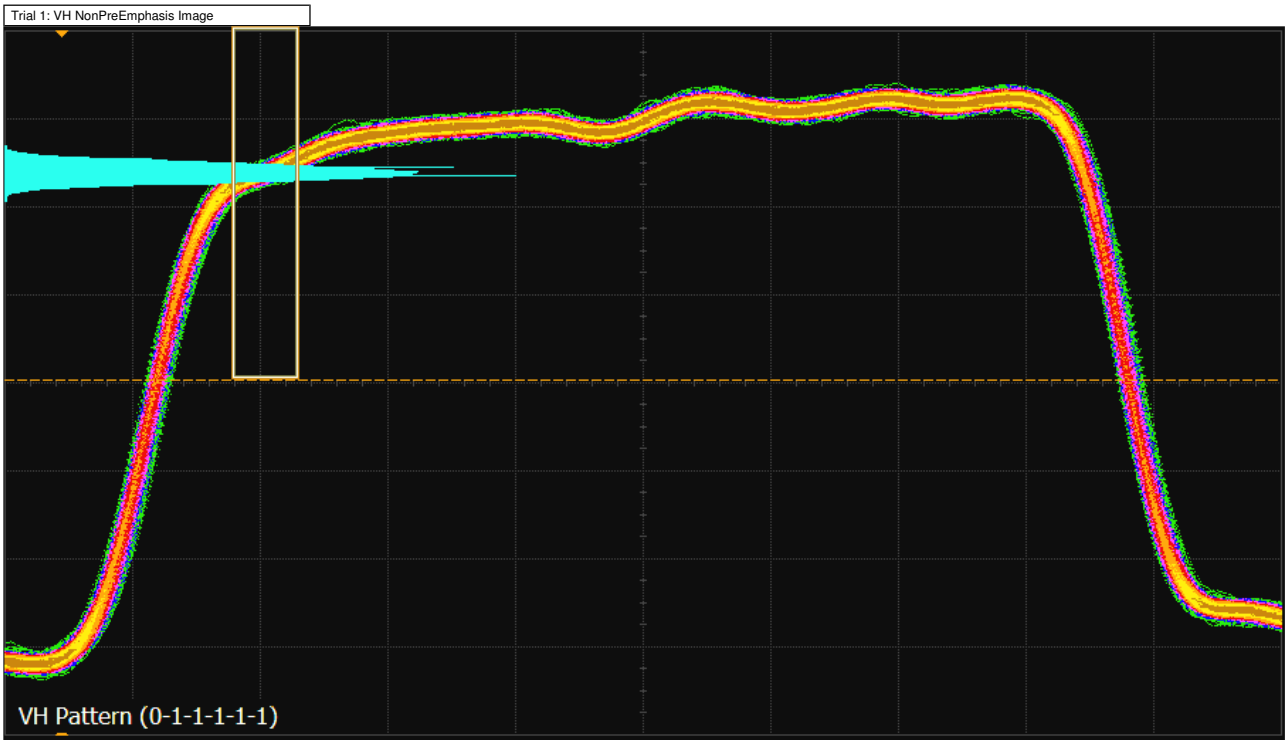
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-1.798 dB	819.2 %											
	StdDev	184.7 mdB	73.89 %											
	Range	439.8 mdB	176.0 %											
	Min	-1.981 dB	716.4 %											
	Max	-1.541 dB	892.4 %											
	Sum	-7.193 dB	3.277 k%											
✓	Trial 1	-1.828 dB	831.2% (See image)	(See image)	(See image)	1000	636.038 mV	785.031 mV	-1.828 dB	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-1.842 dB	836.8% (See image)	(See image)	(See image)	1000	469.987 mV	581.046 mV	-1.842 dB	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-1.981 dB	892.4% (See image)	(See image)	(See image)	1000	324.957 mV	408.211 mV	-1.981 dB	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4 (Worst)	-1.541 dB	716.4% (See image)	(See image)	(See image)	1000	822.088 mV	981.714 mV	-1.541 dB	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

Trial 1

Trial 1: VL NonPreEmphasis Image

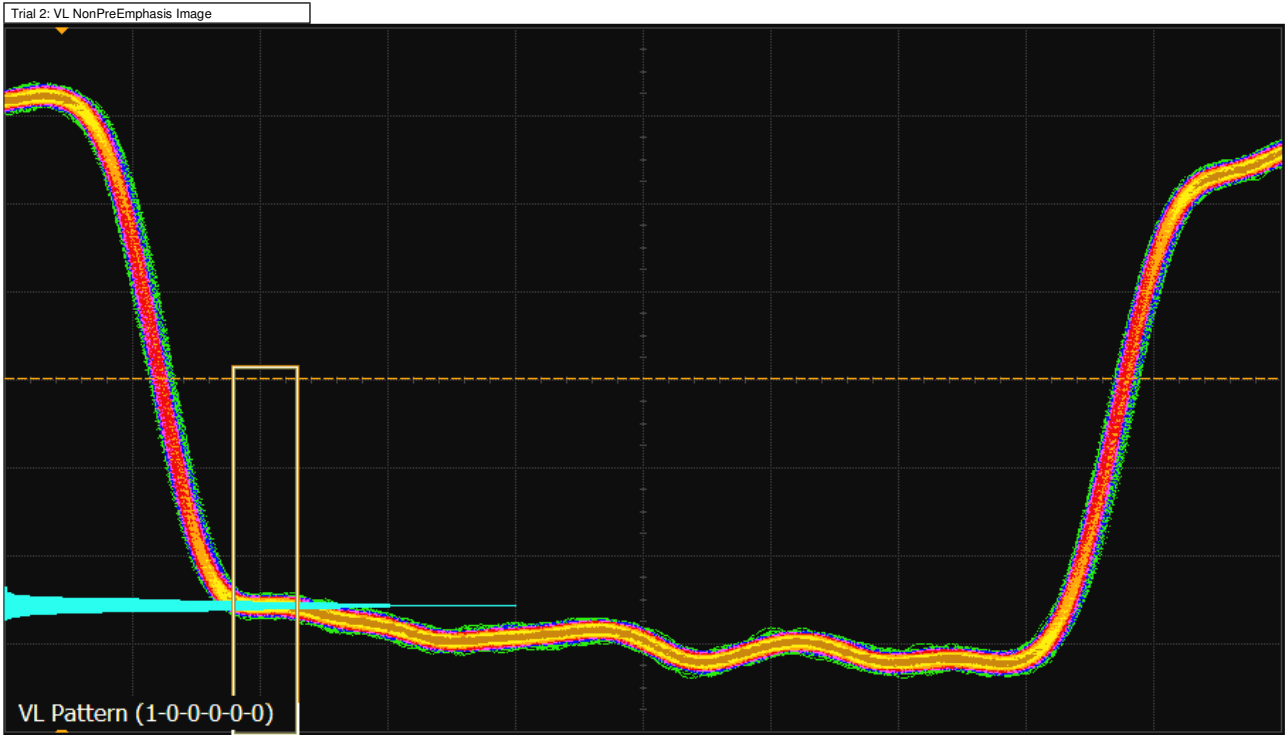


Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	122.0 ps/div	555.6 ps	132.0 mV/div	-7.900 mV

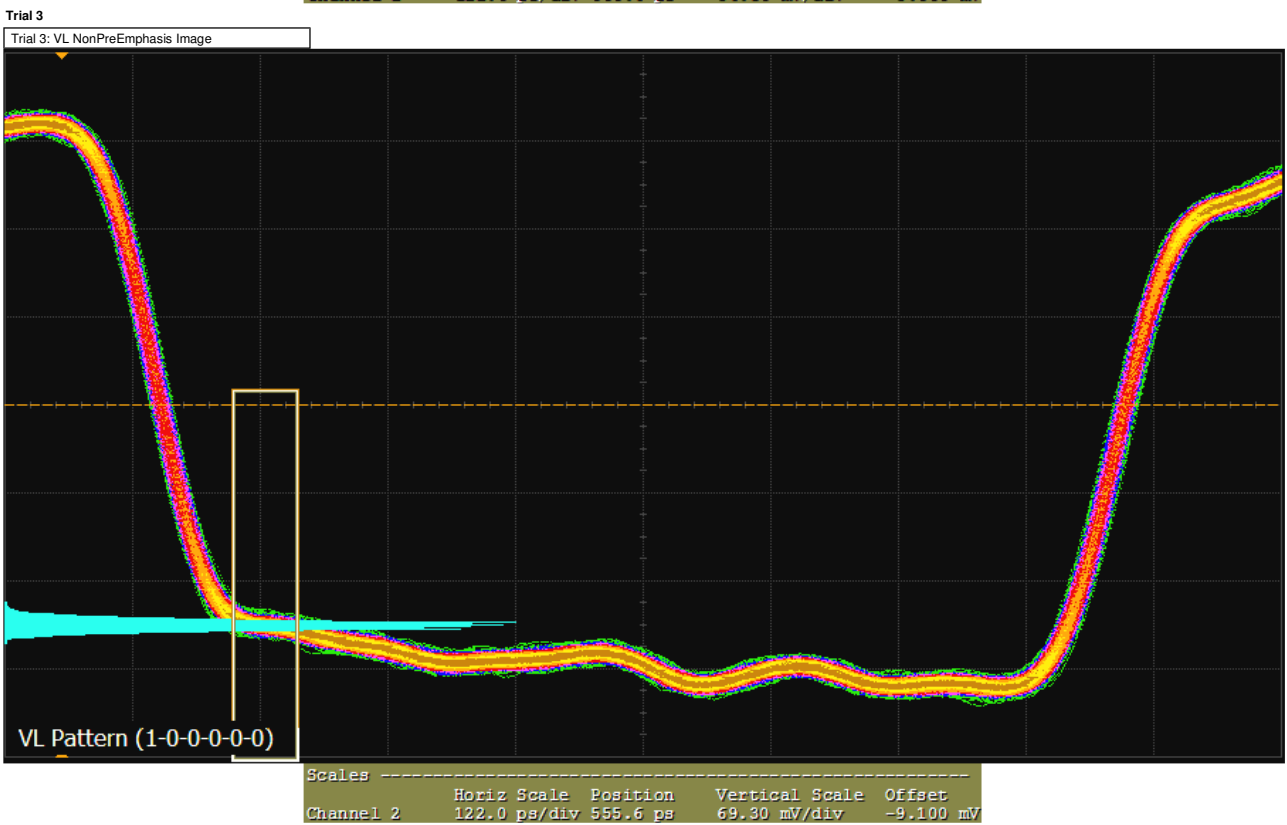
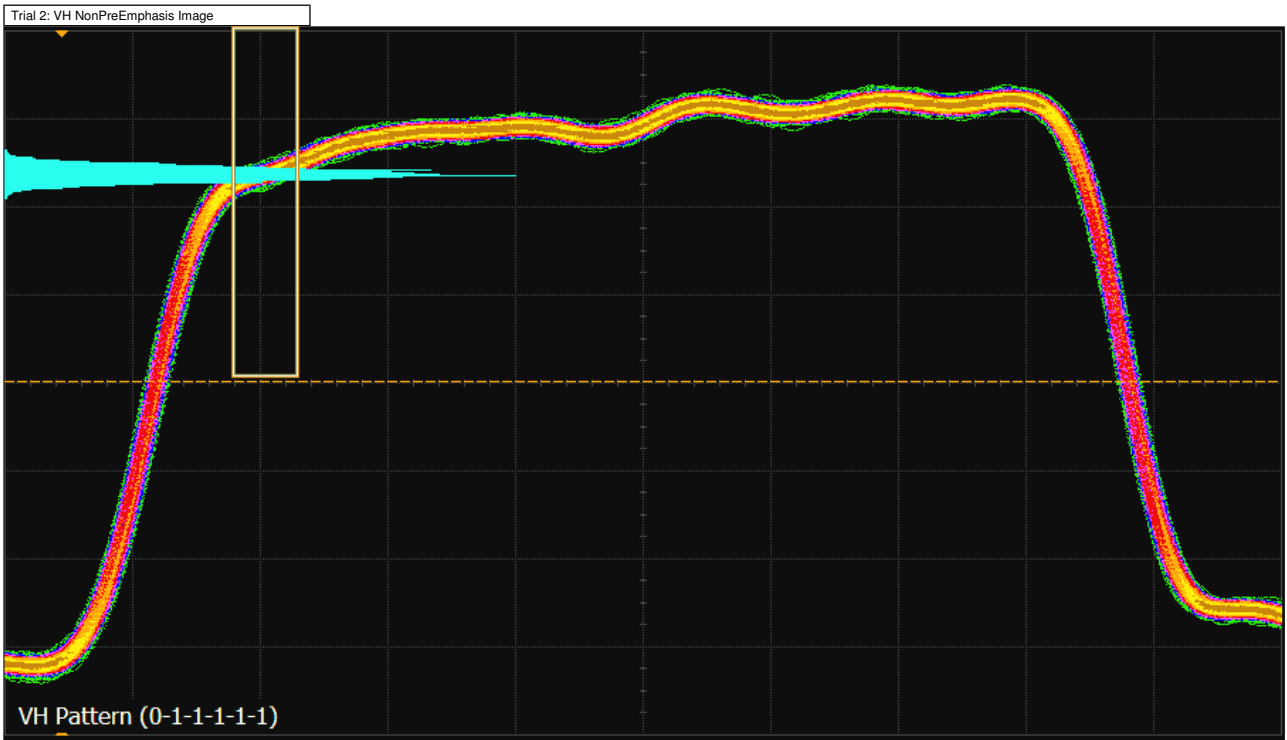


Scales -----				
	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	132.0 mV/div	-7.900 mV

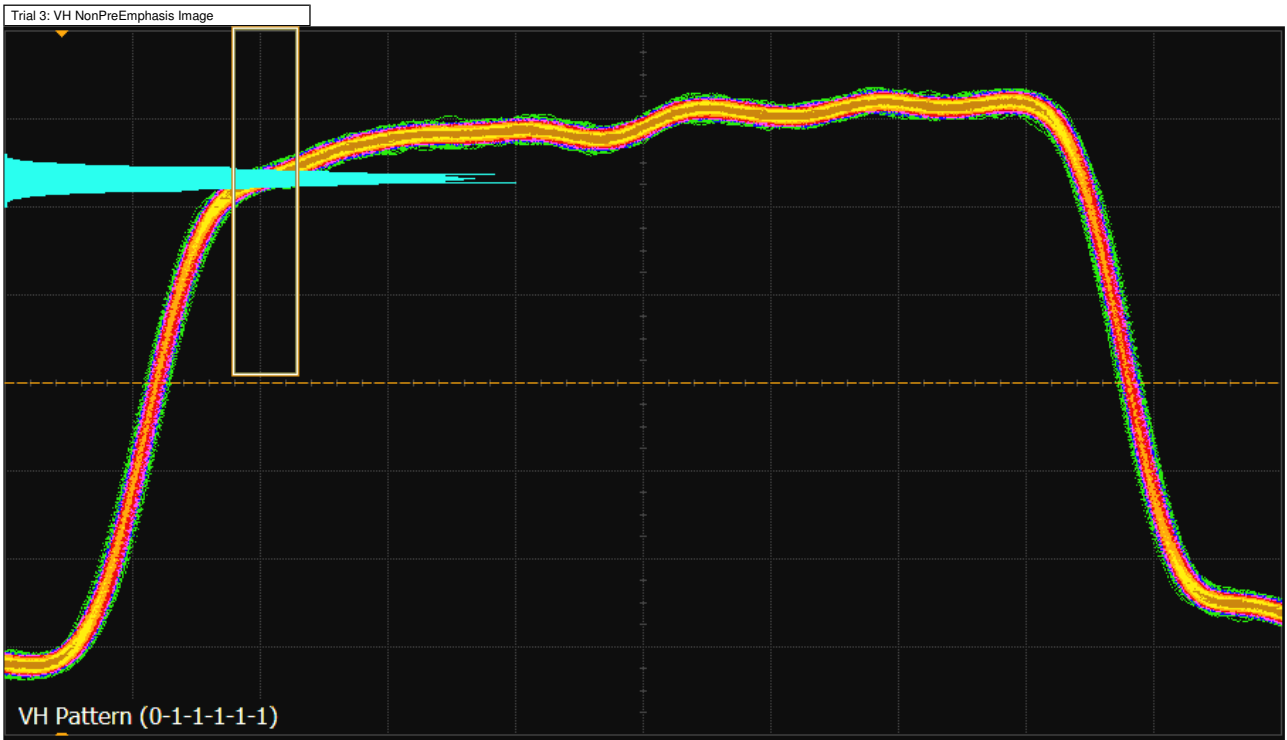
Trial 2



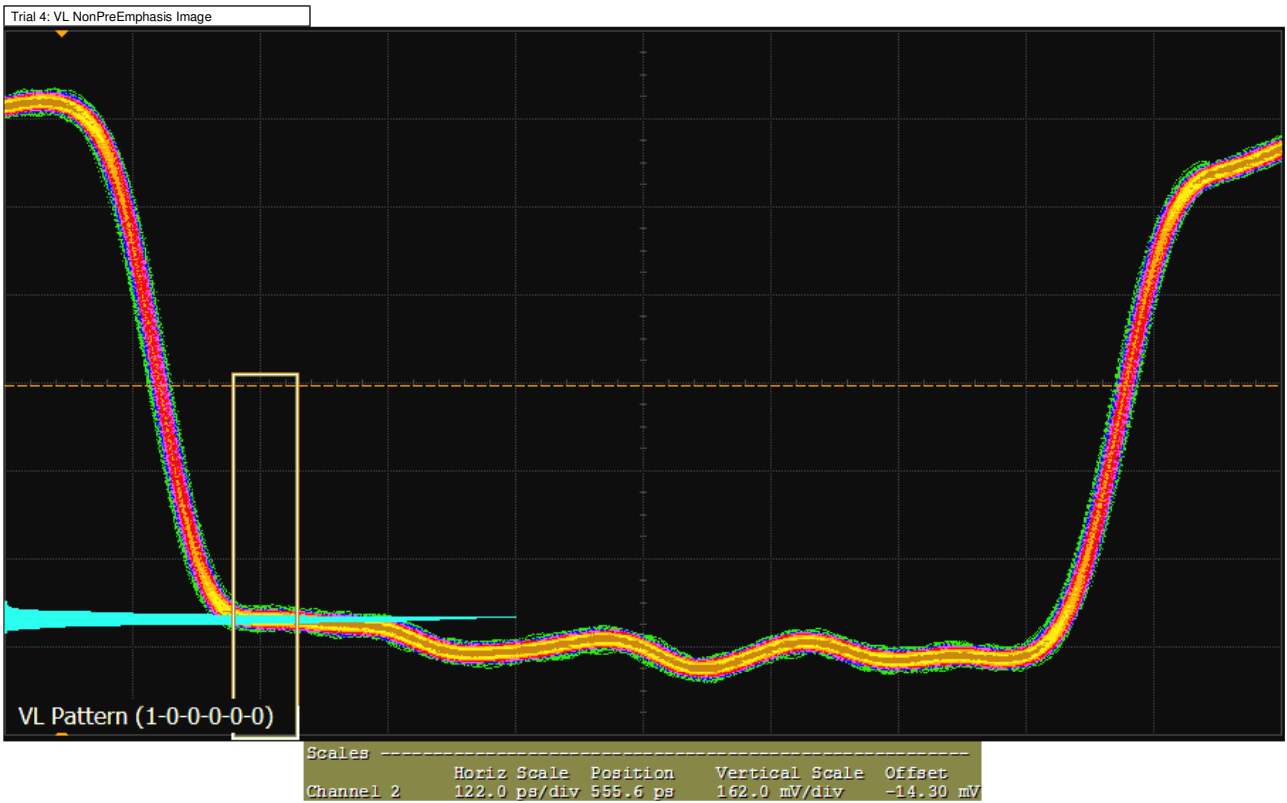
Scales -----				
	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	96.80 mV/div	-9.500 mV

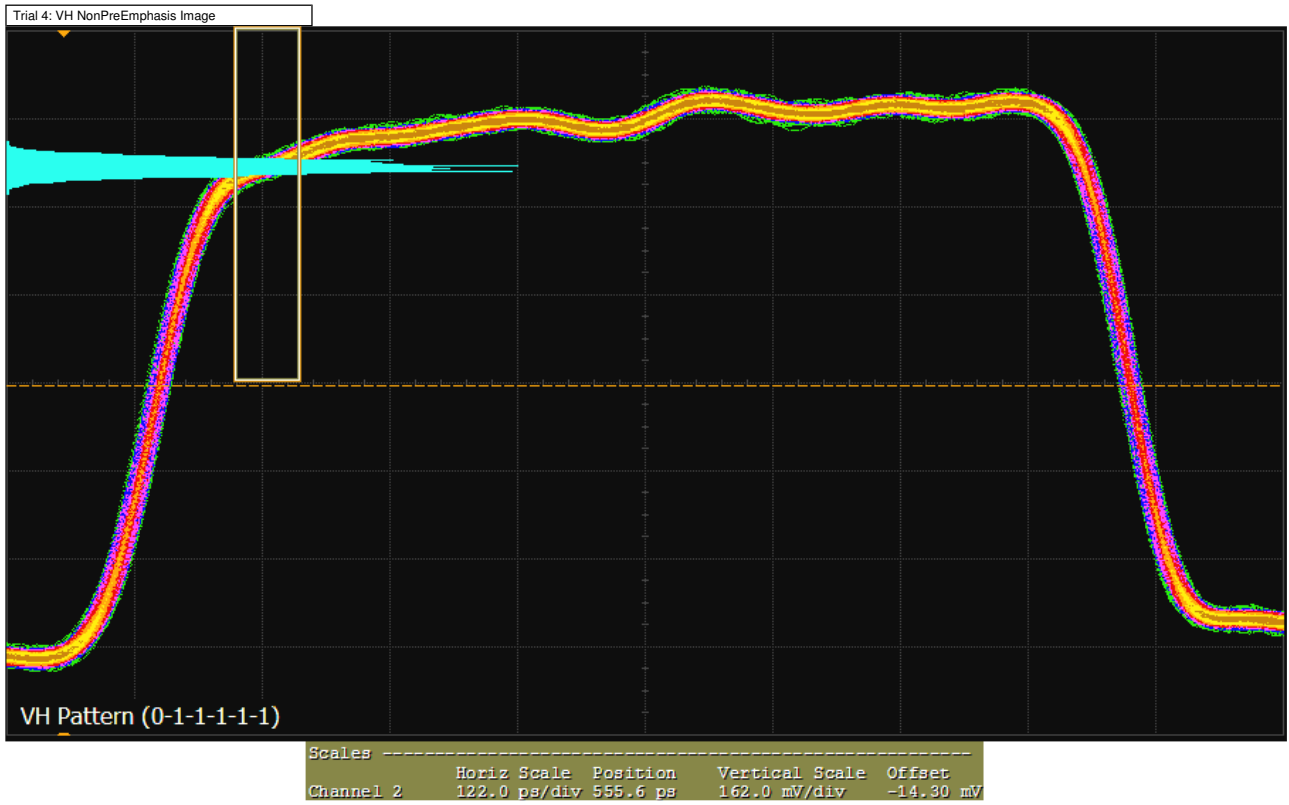






Trial 4





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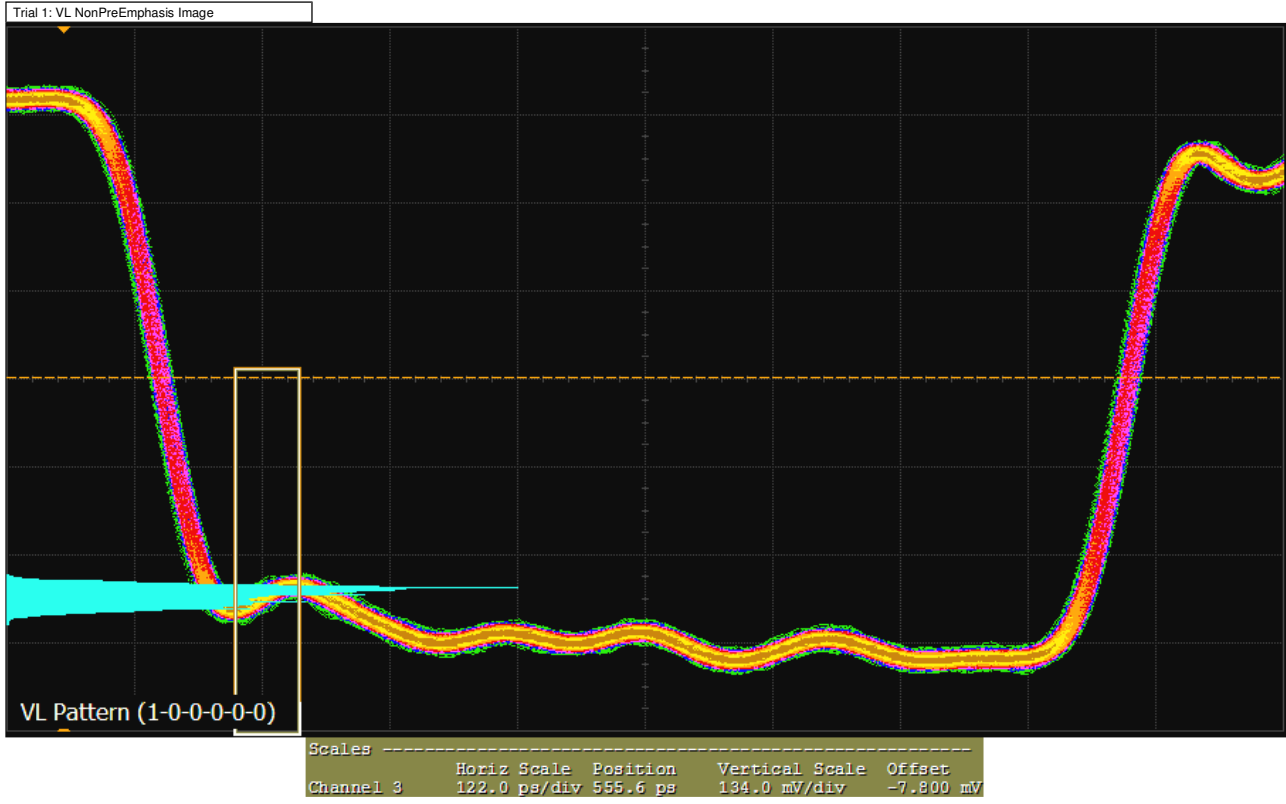
✓ Lane 2 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

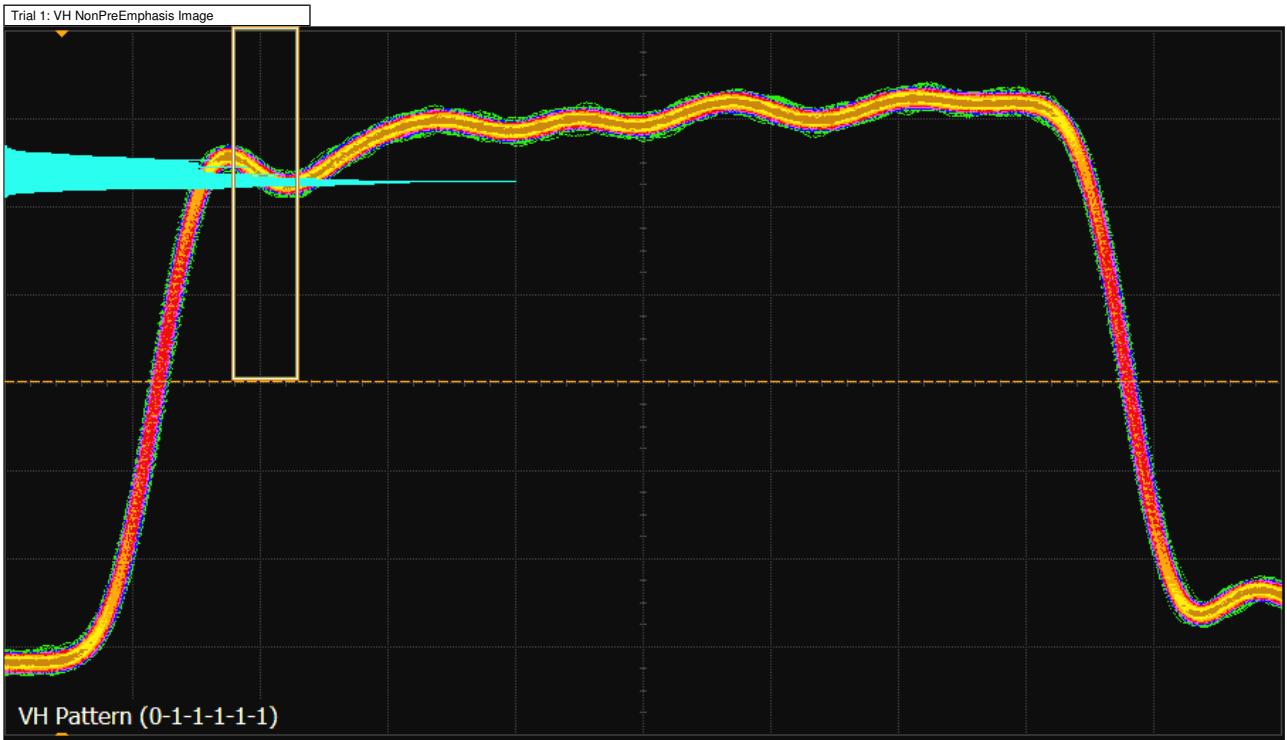
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: <= 250 mdB PreEmphasis(Pre-emphasis 0) (Worst of 4 Trials) -1.789 dB # Trials Run: 4 Worst Trial: Trial 4

Overall Summary + details of 4 worst trials

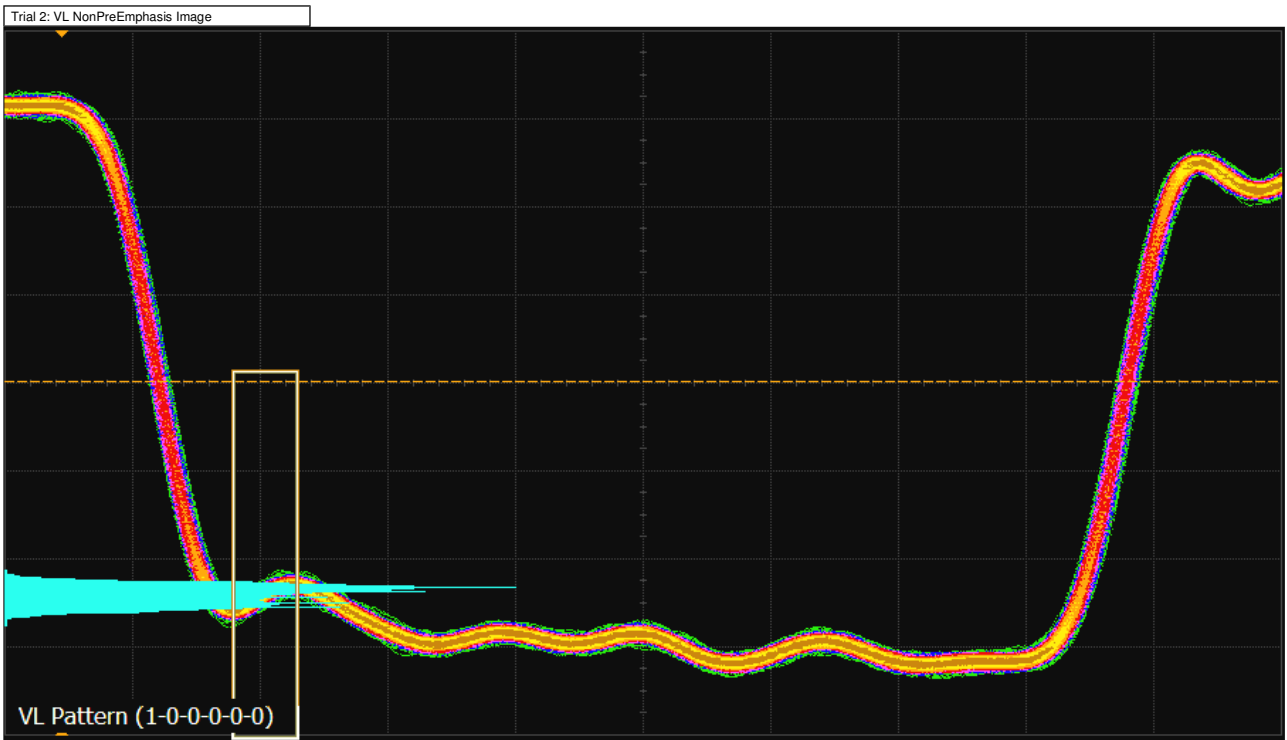
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-2.074 dB	929.8 %											
	StdDev	221.5 mdB	88.60 %											
	Range	528.9 mdB	211.6 %											
	Min	-2.318 dB	815.6 %											
	Max	-1.789 dB	1.027 k%											
	Sum	-8.297 dB	3.719 k%											
✓	Trial 1	-2.043 dB	917.2%	(See image)	(See image)	1000	632.436 mV	800.097 mV	-2.043 dB	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-2.148 dB	959.2%	(See image)	(See image)	1000	464.156 mV	594.375 mV	-2.148 dB	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-2.318 dB	103E+01%	(See image)	(See image)	1000	325.536 mV	425.095 mV	-2.318 dB	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4 (Worst)	-1.789 dB	815.6%	(See image)	(See image)	1000	808.729 mV	993.677 mV	-1.789 dB	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

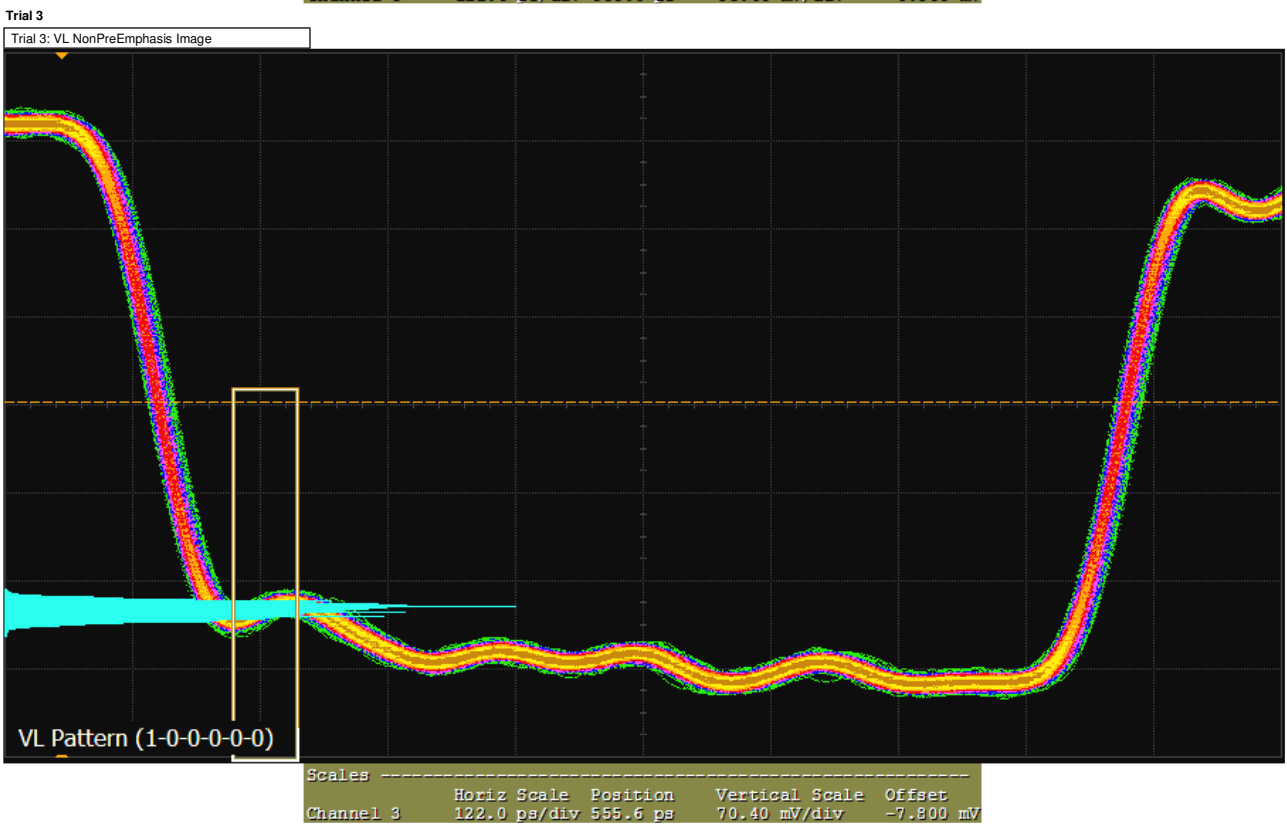
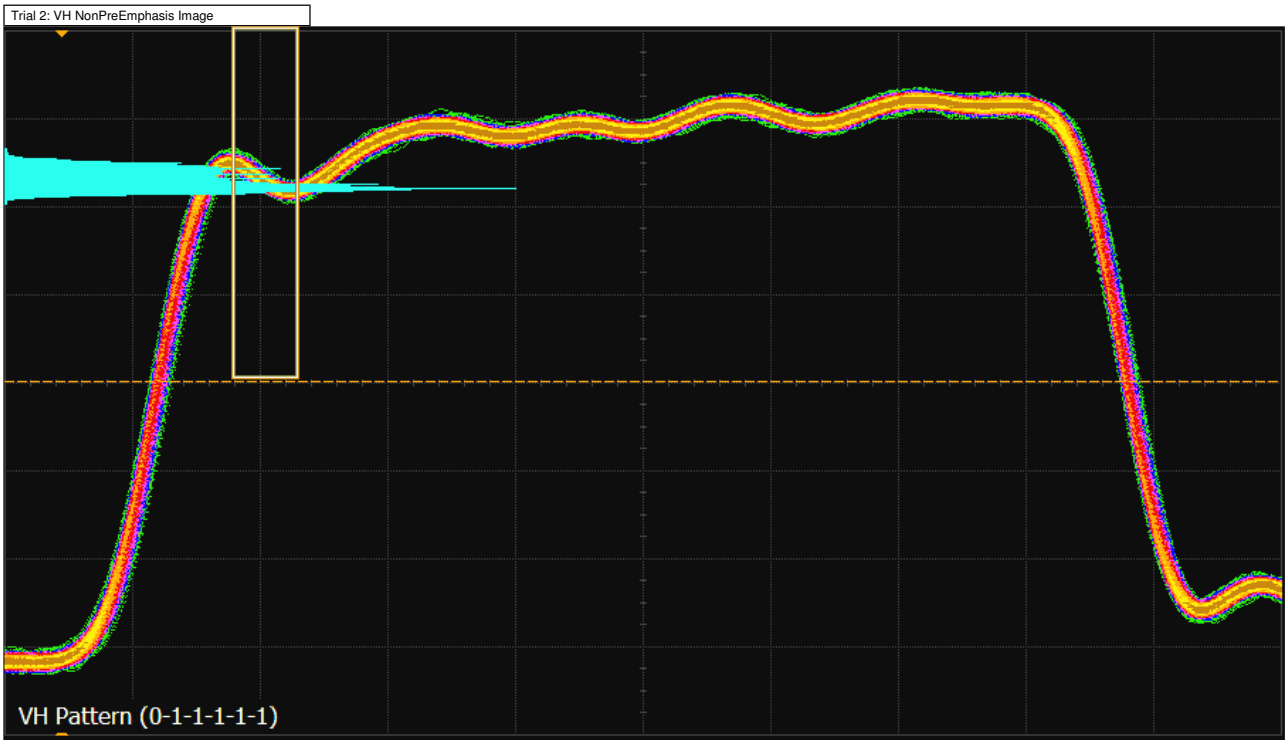
Trial 1

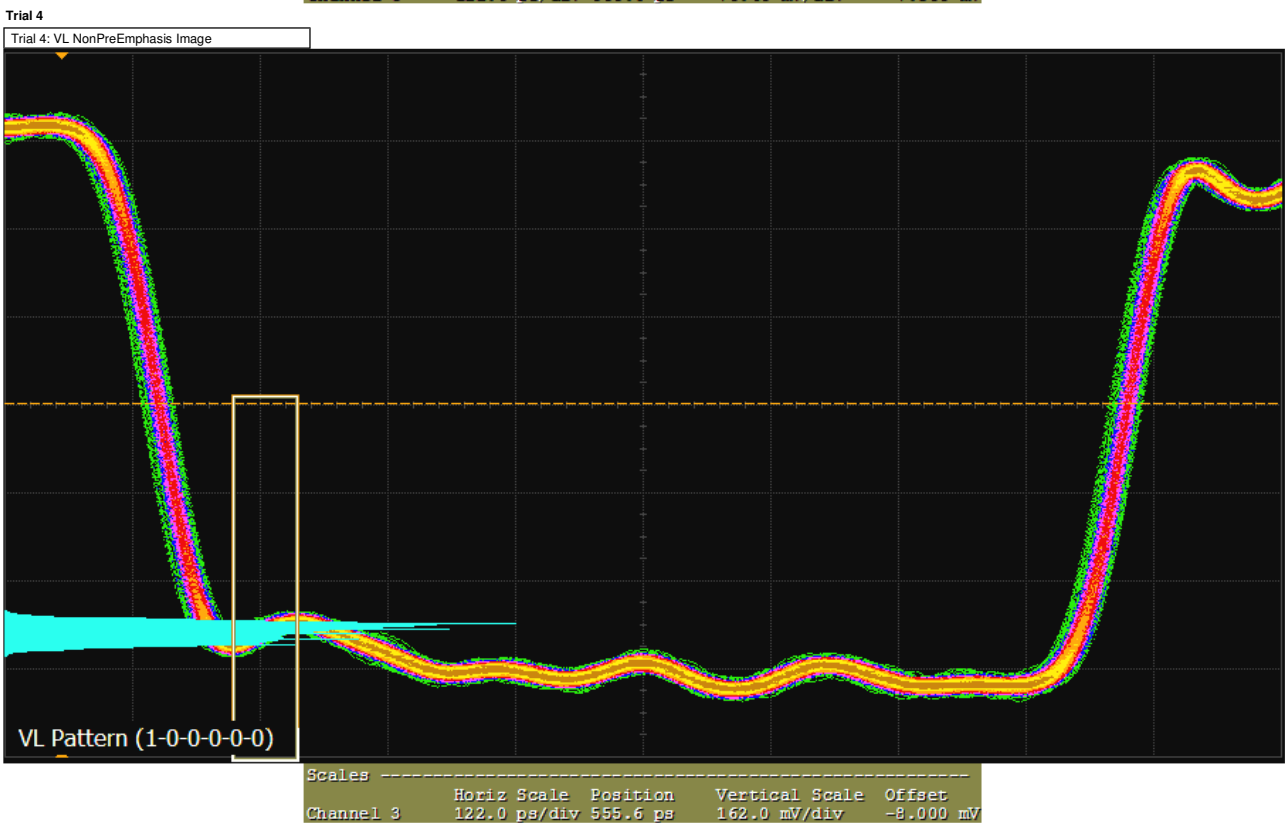
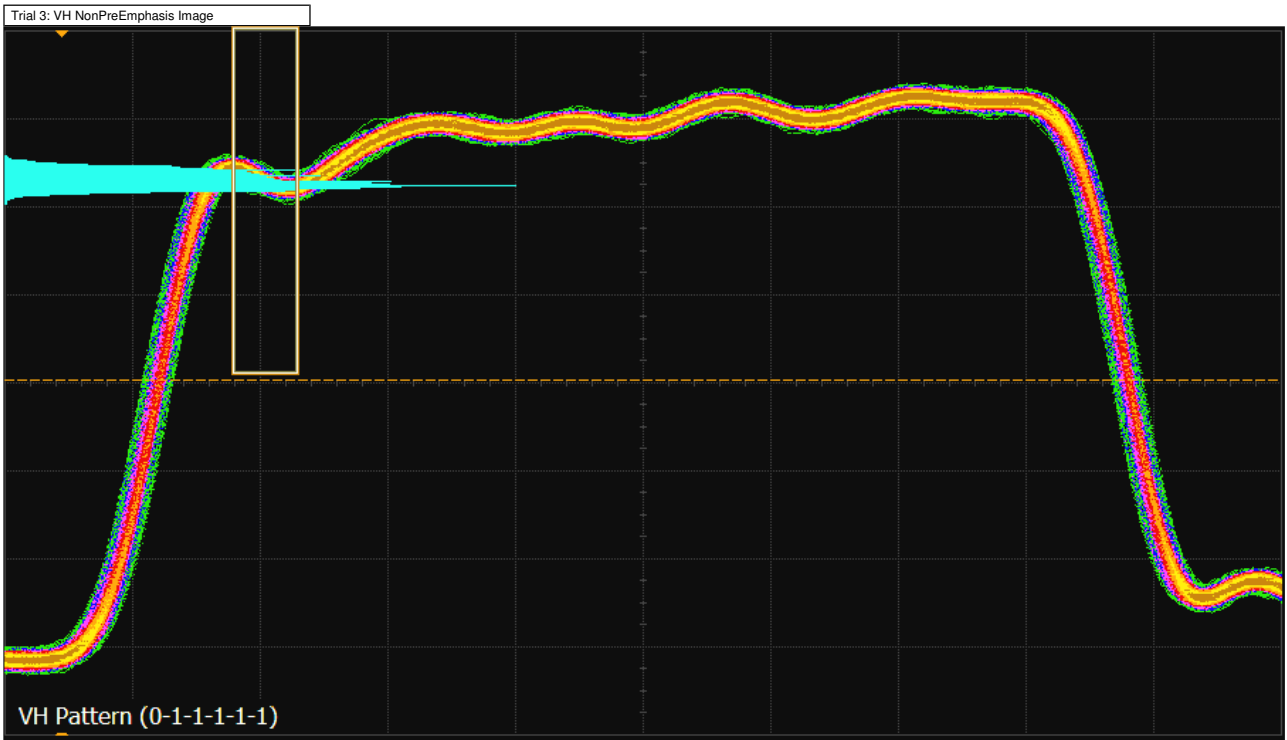


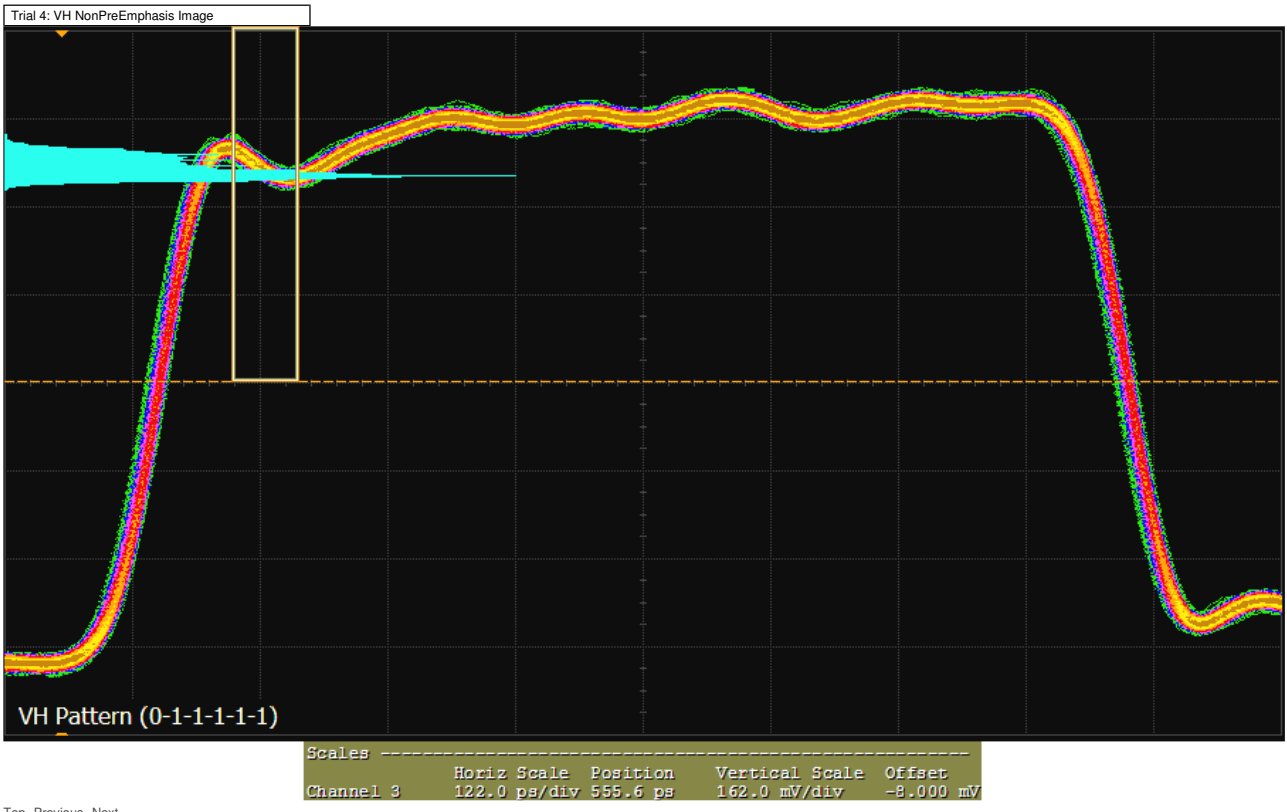


Trial 2











✓ Lane 3 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

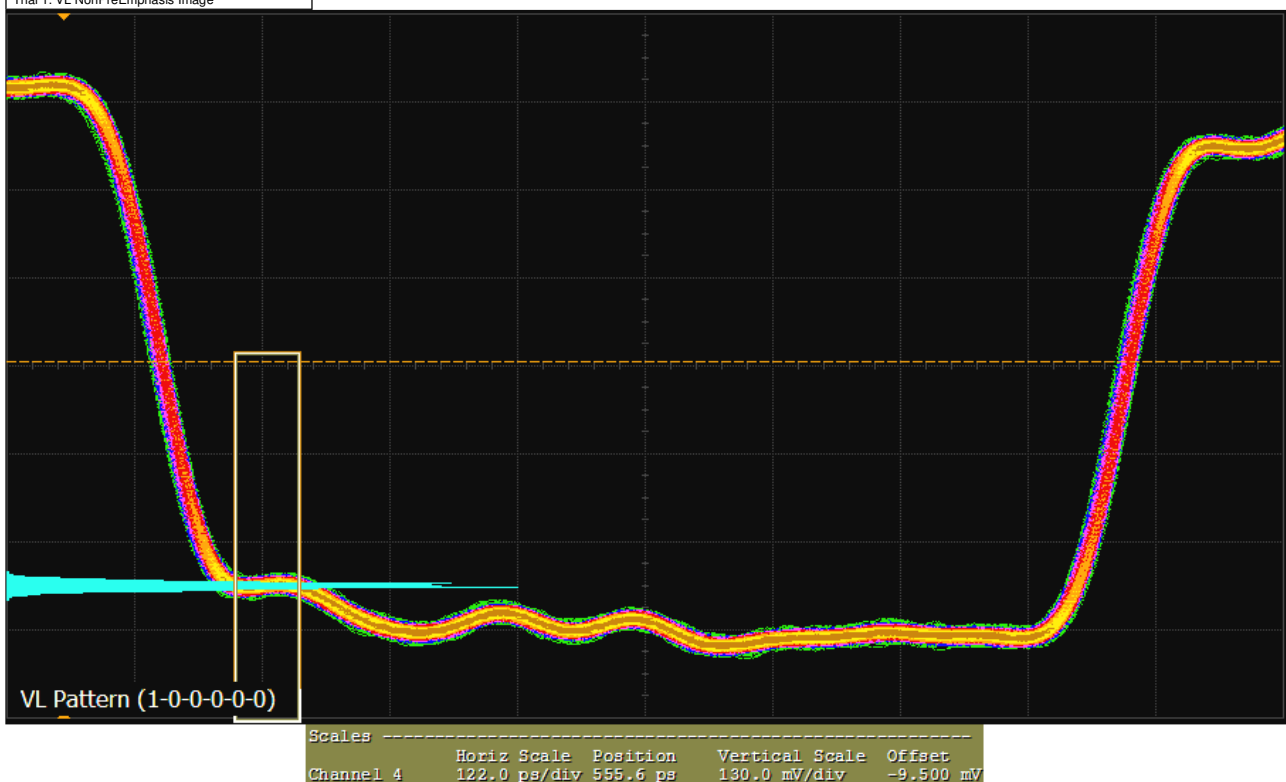
Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
**Pass Limits:** <= 250 mdB | **PreEmphasis(Pre-emphasis 0) (Worst of 4 Trials)** -1.785 dB | **# Trials Run:** 4 | **Worst Trial:** Trial 1

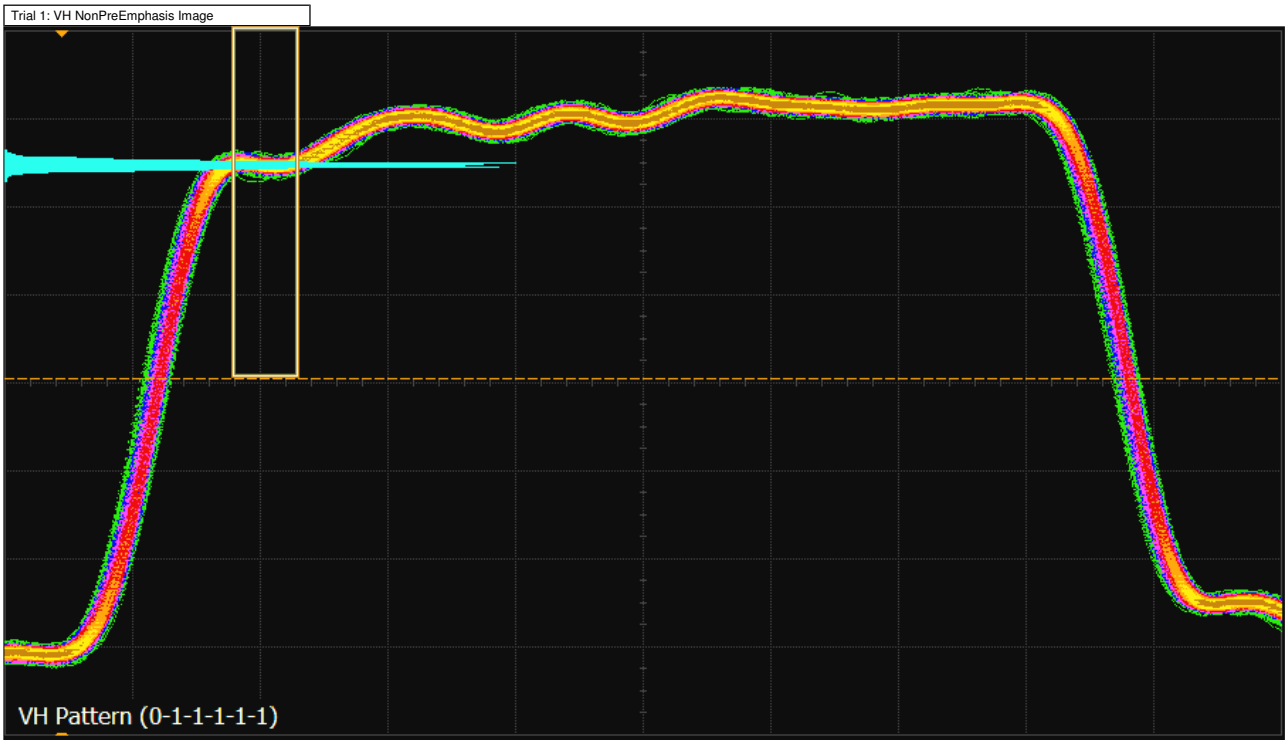
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	<i>-1.916 dB</i>	<i>866.4 %</i>											
	<i>StdDev</i>	<i>115.8 mdB</i>	<i>46.35 %</i>											
	<i>Range</i>	<i>273.9 mdB</i>	<i>109.6 %</i>											
	<i>Min</i>	<i>-2.059 dB</i>	<i>814.0 %</i>											
	<i>Max</i>	<i>-1.785 dB</i>	<i>923.6 %</i>											
	<i>Sum</i>	<i>-7.665 dB</i>	<i>3.466 k%</i>											
✓	Trial 1 (Worst)	-1.785 dB	814.0% (See image)	(See image)	(See image)	1000	646.689 mV	794.263 mV	-1.785 dB	5.4 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-1.946 dB	878.4% (See image)	(See image)	(See image)	1000	463.007 mV	579.270 mV	-1.946 dB	5.4 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-2.059 dB	923.6% (See image)	(See image)	(See image)	1000	317.273 mV	402.157 mV	-2.059 dB	5.4 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	-1.874 dB	849.6% (See image)	(See image)	(See image)	1000	809.137 mV	1.003986 V	-1.874 dB	5.4 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

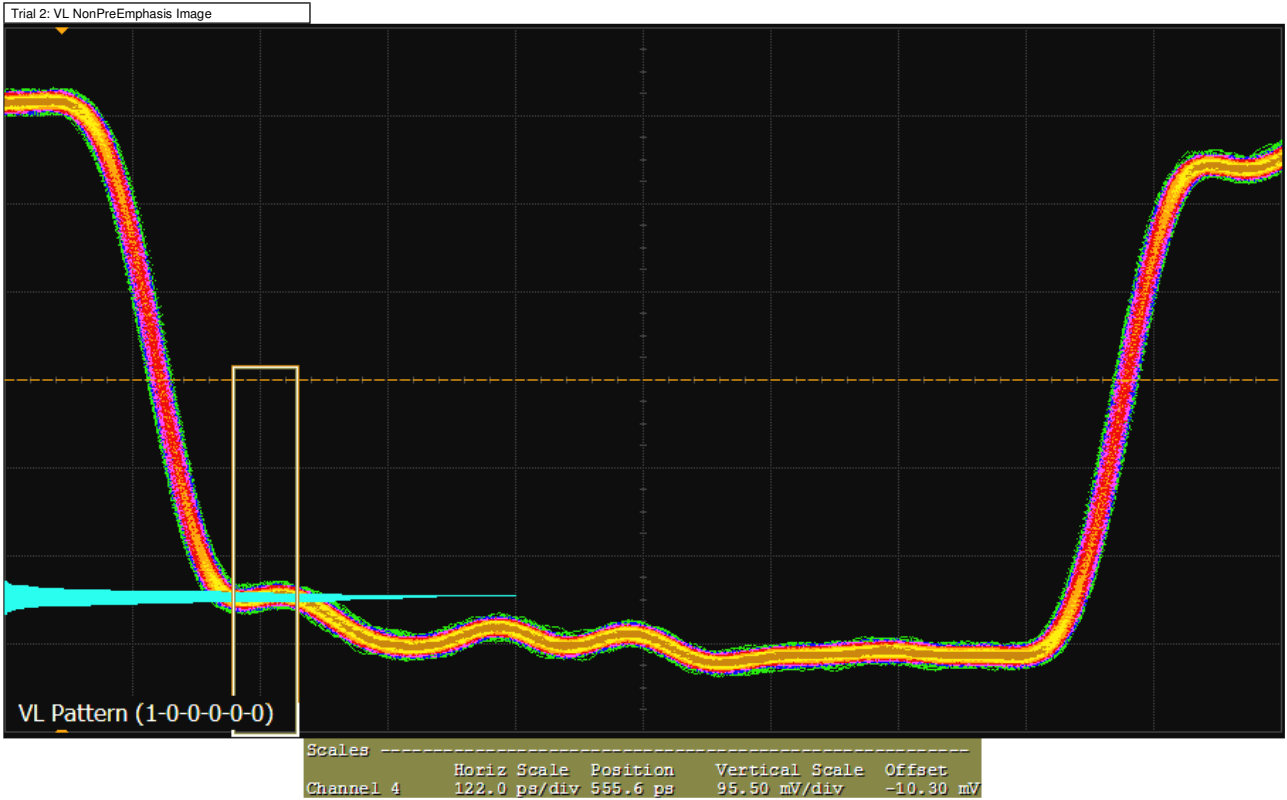
Trial 1

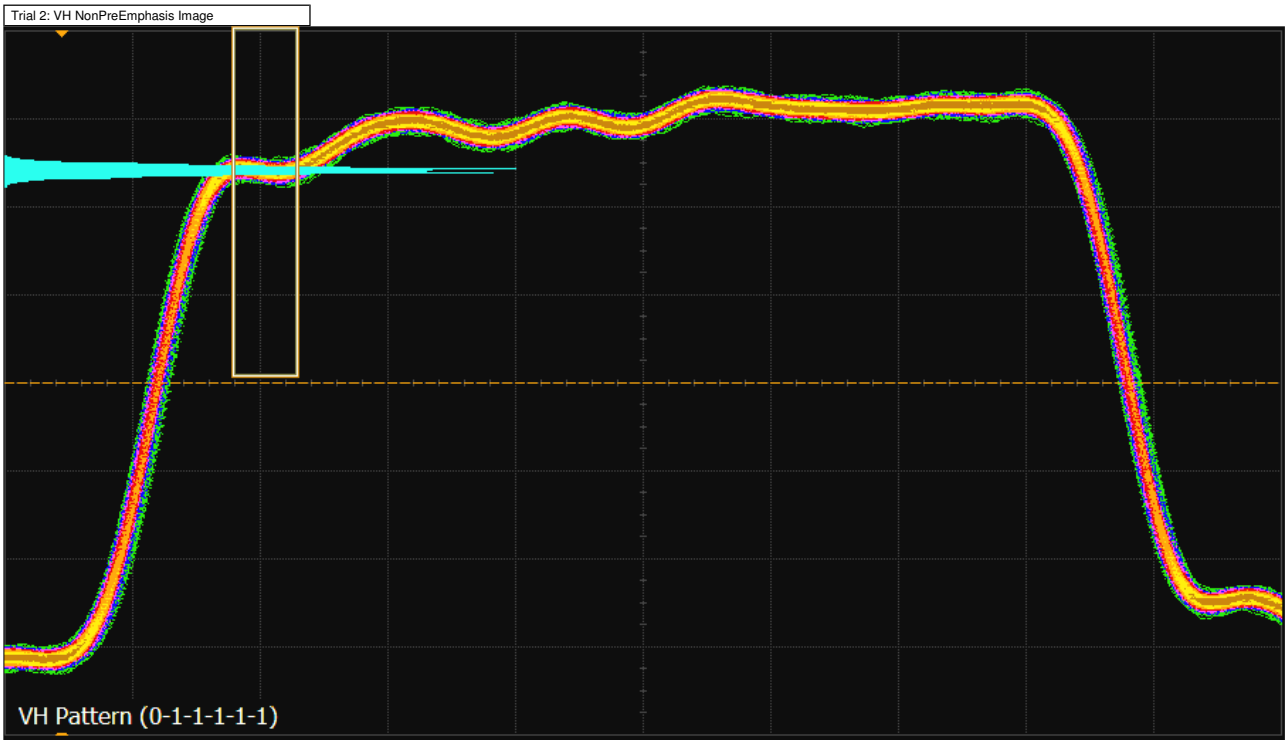
Trial 1: VL NonPreEmphasis Image





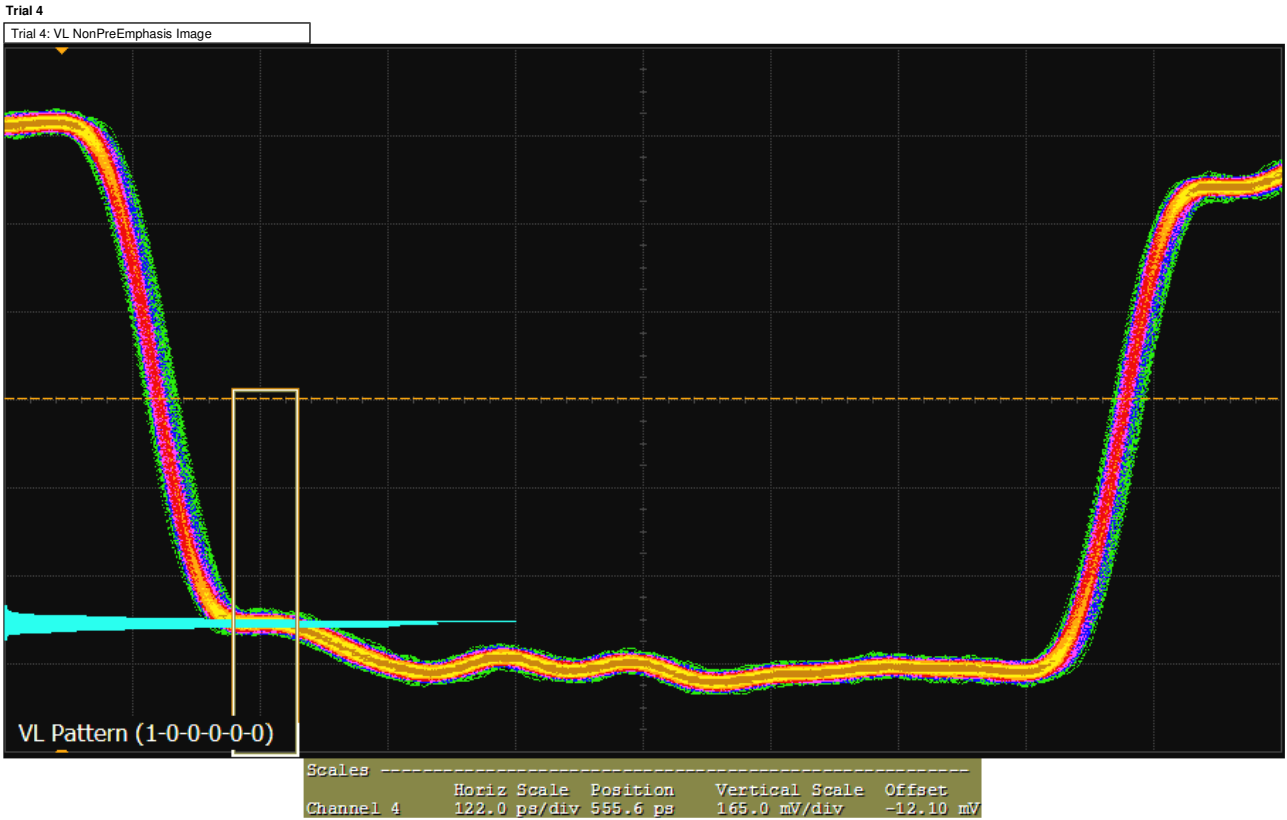
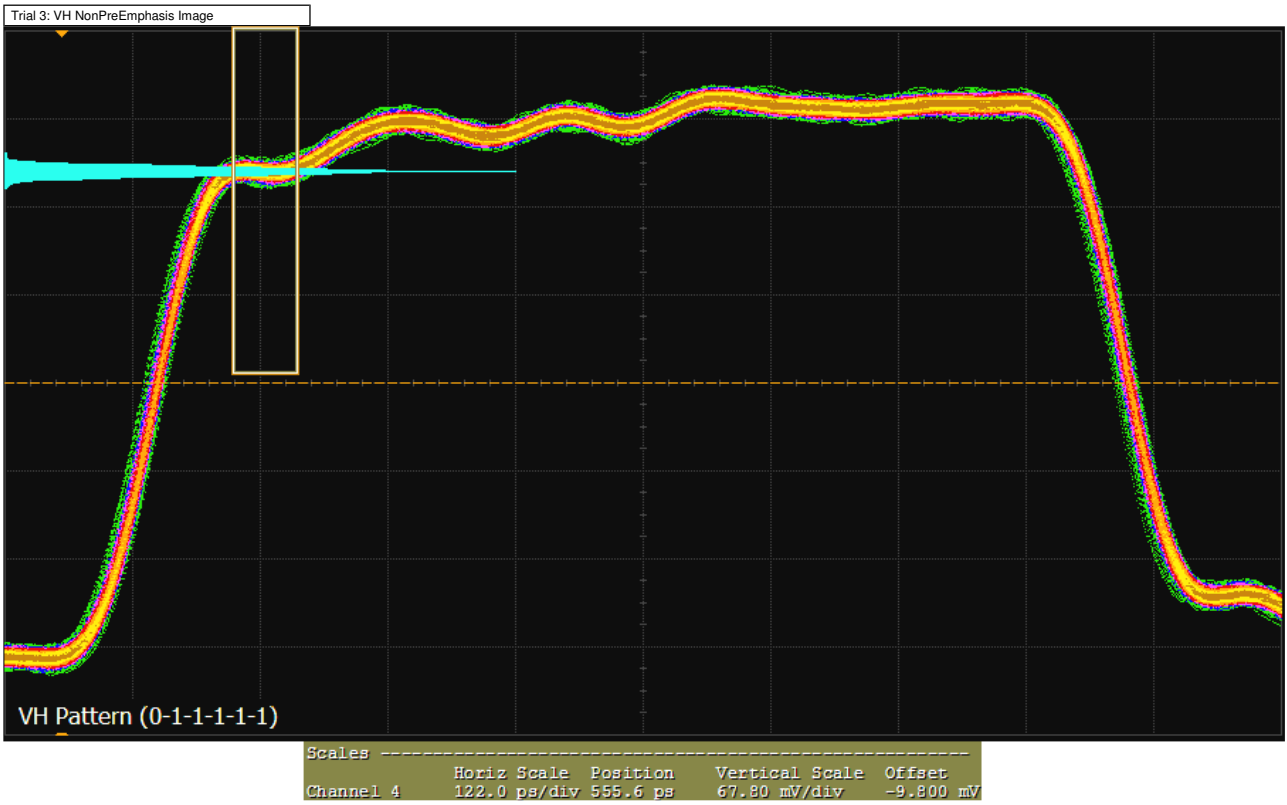
Trial 2

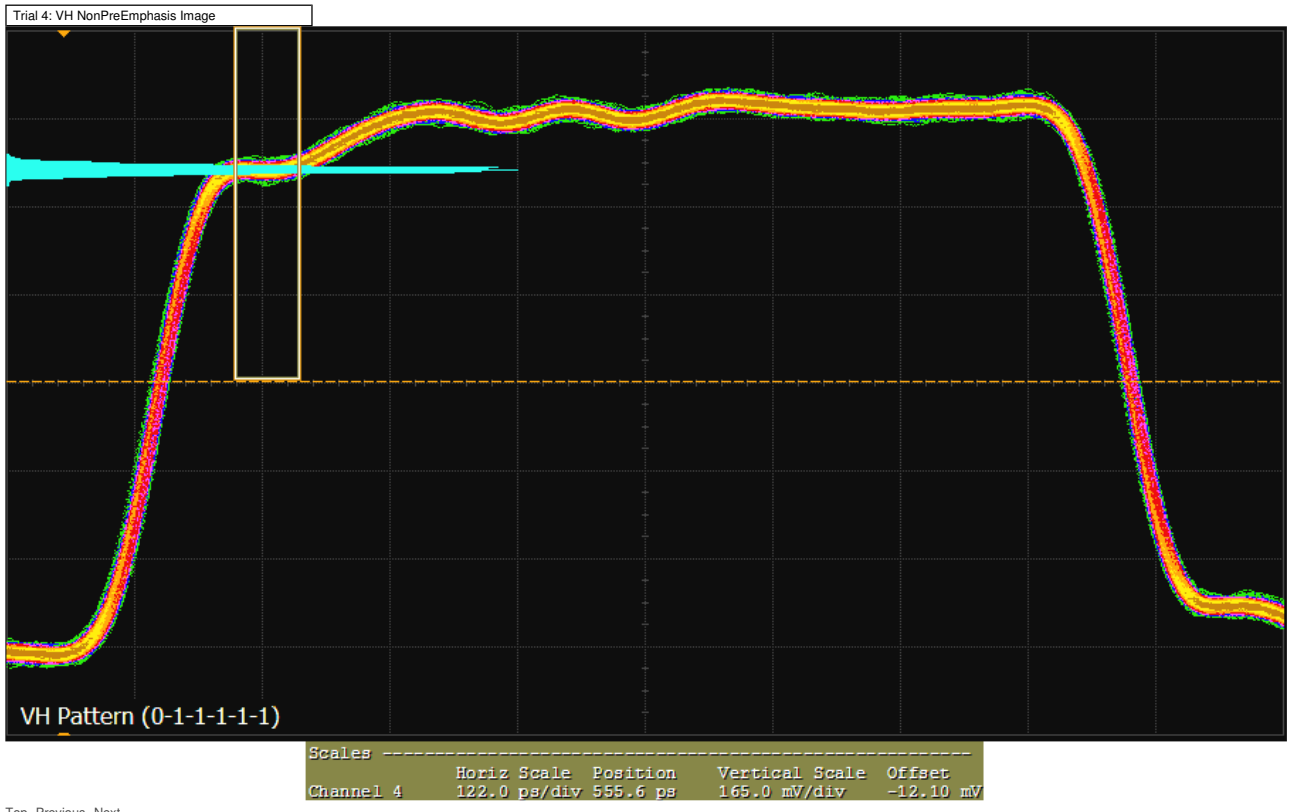




Trial 3







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✓ Lane 0 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)
 Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass
 Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

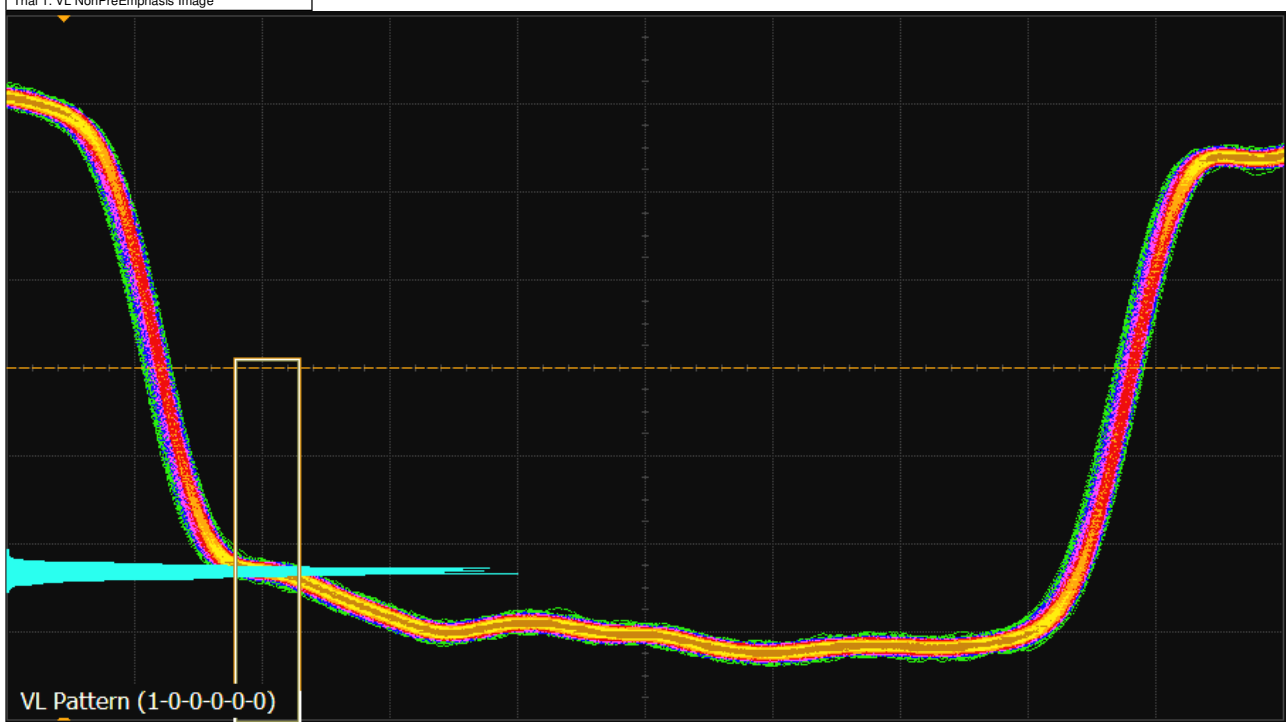
Pass Limits: >= 2.000 dB
PreEmphasis (Pre-emphasis 1) (Worst of 3 Trials) 5.464 dB
# Trials Run: 3
Worst Trial: Trial 1

Overall Summary + details of 3 worst trials

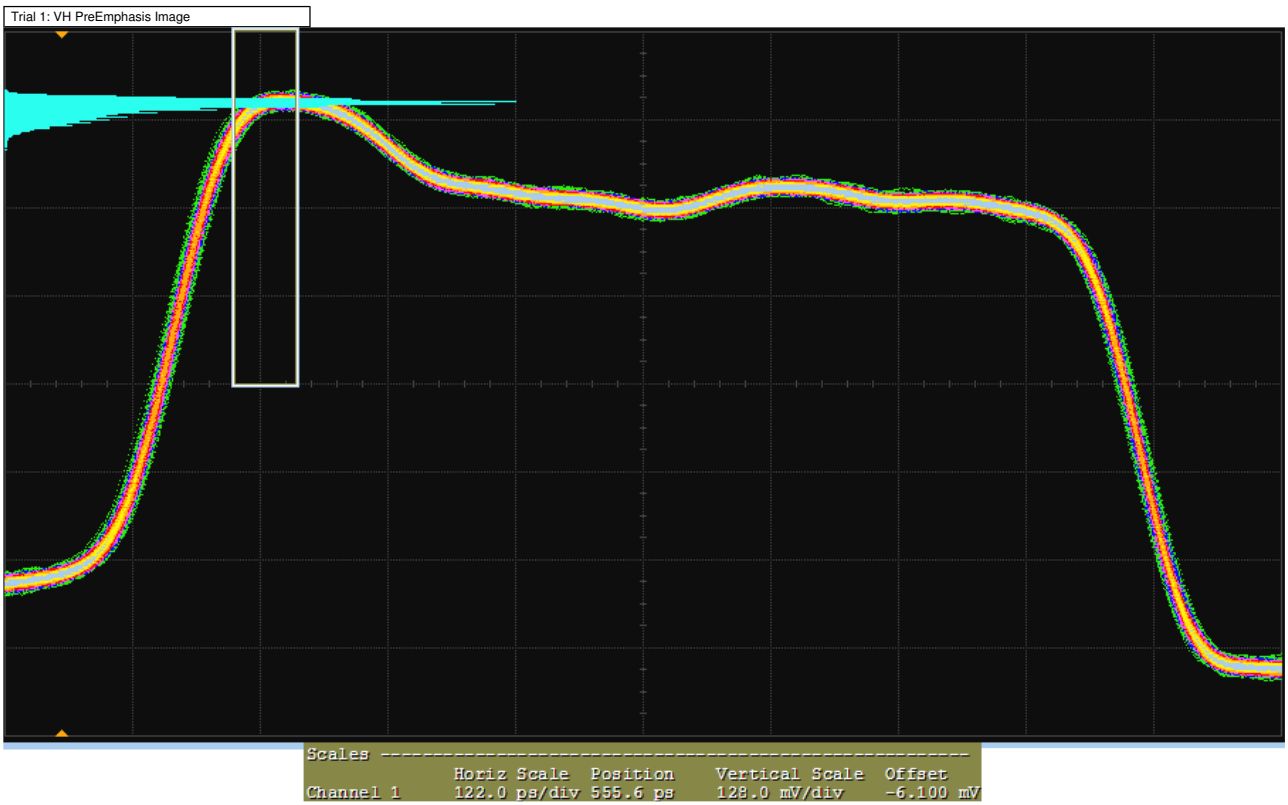
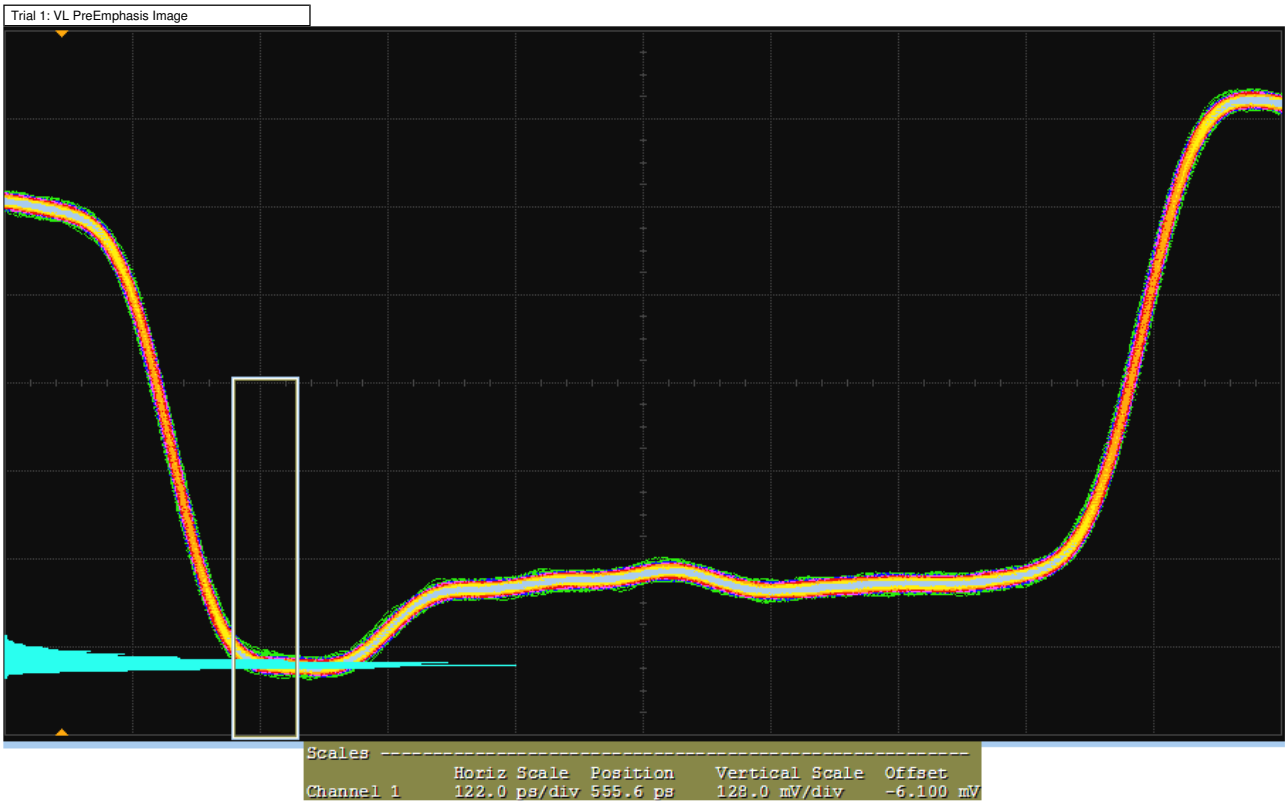
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	5.883 dB	194.2 %													
	StdDev	363.2 mdB	18.16 %													
	Range	631.7 mdB	31.60 %													
	Min	5.464 dB	173.2 %													
	Max	6.096 dB	204.8 %													
	Sum	17.65 dB	582.5 %													
✓	Trial 1 (Worst)	5.464 dB	173.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	846.755 mV	587.262 mV	3.179 dB	5.4 Gbps	2	Swing Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 2	6.096 dB	204.8% (See image)	(See image)	(See image)	(See image)	(See image)	1000	730.967 mV	483.377 mV	3.592 dB	5.4 Gbps	1	Swing Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	6.090 dB	204.5% (See image)	(See image)	(See image)	(See image)	(See image)	1000	508.945 mV	341.692 mV	3.461 dB	5.4 Gbps	0	Swing Pre-emphasis 1	SSC Disabled	Level 0

Trial 1

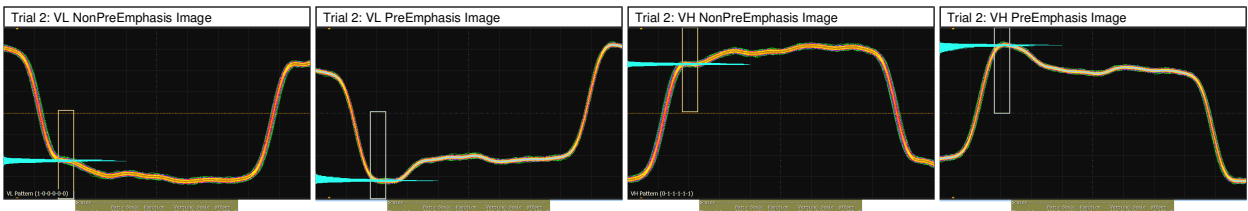
Trial 1: VL NonPreEmphasis Image



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	130.0 mV/div	-9.200 mV

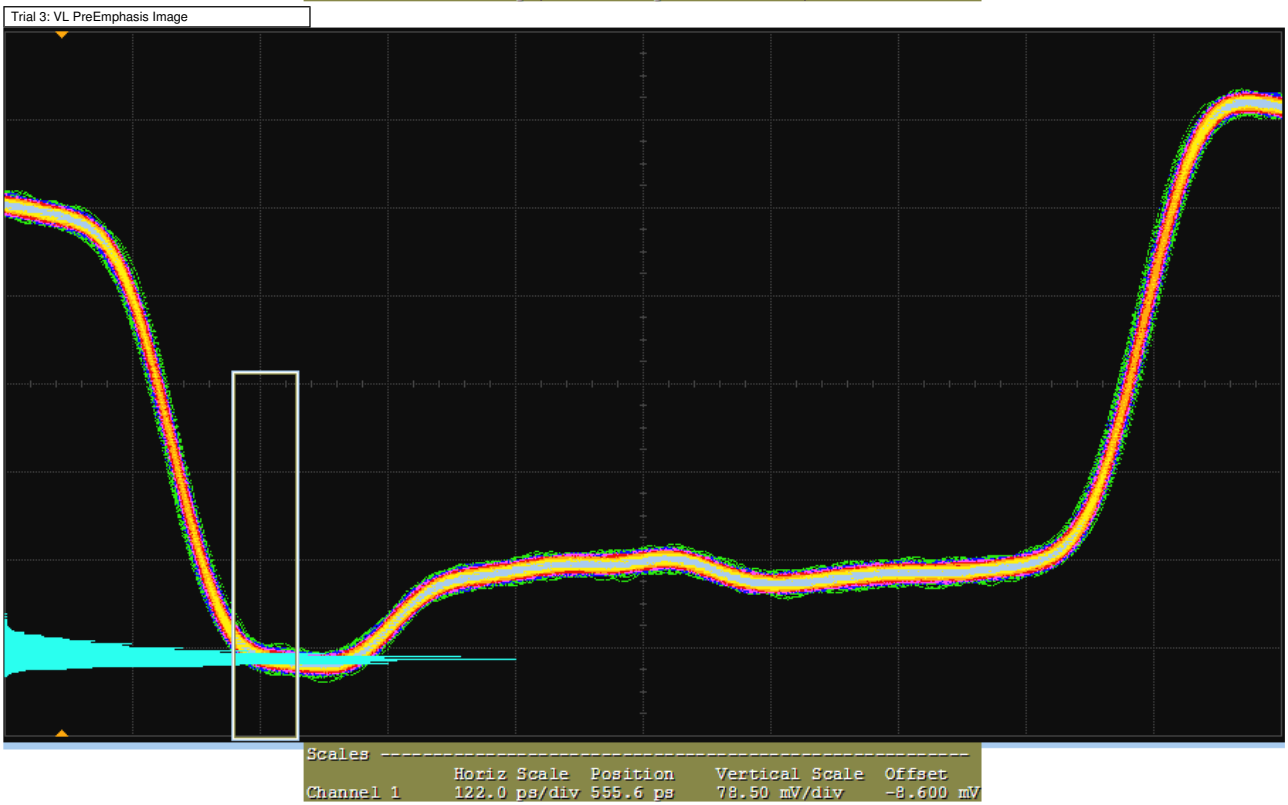
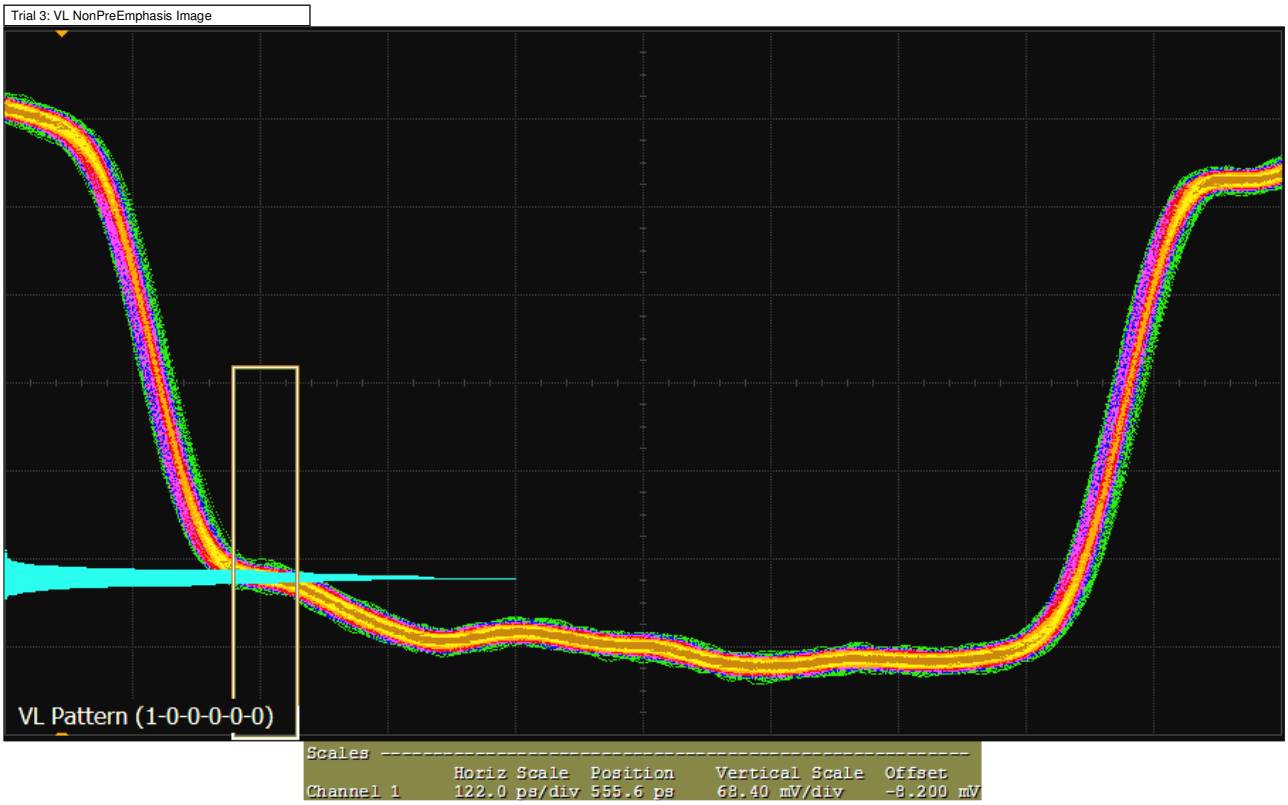


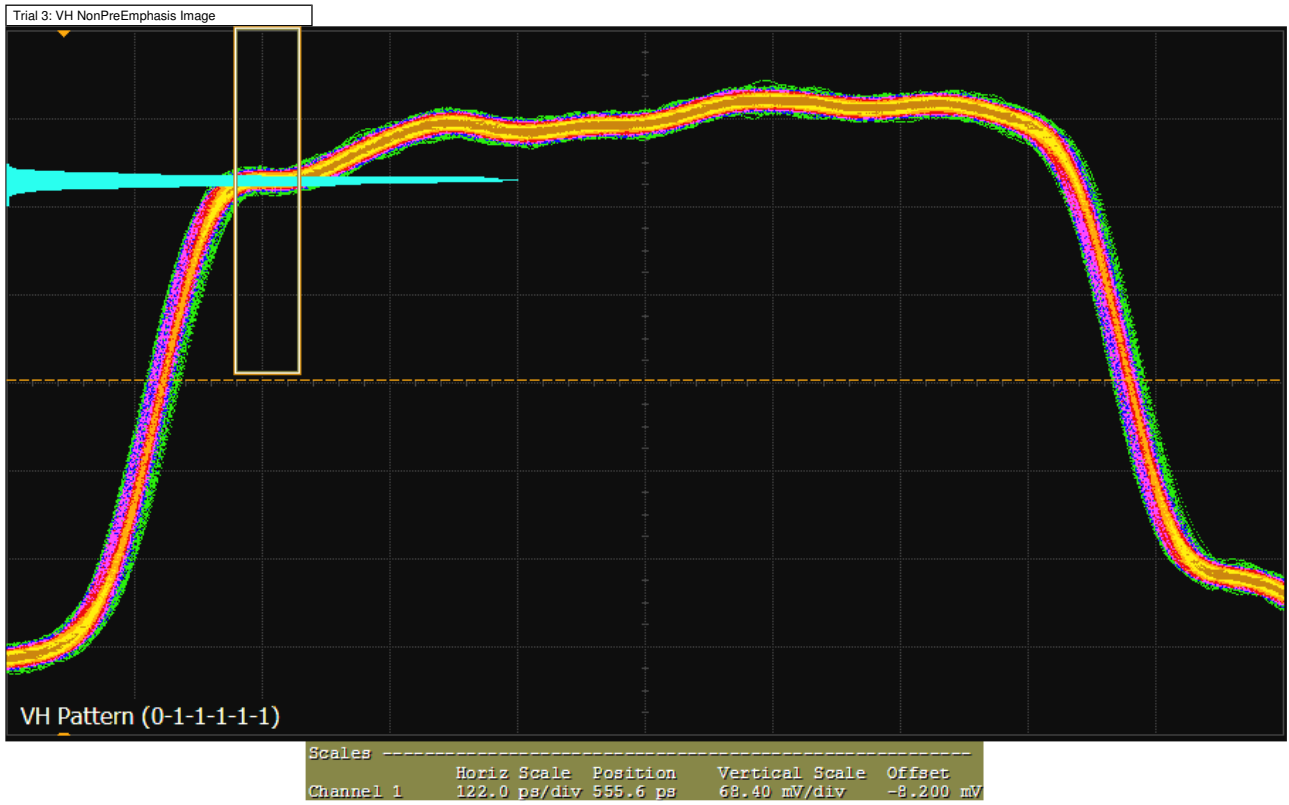
Trial 2



Trial 3







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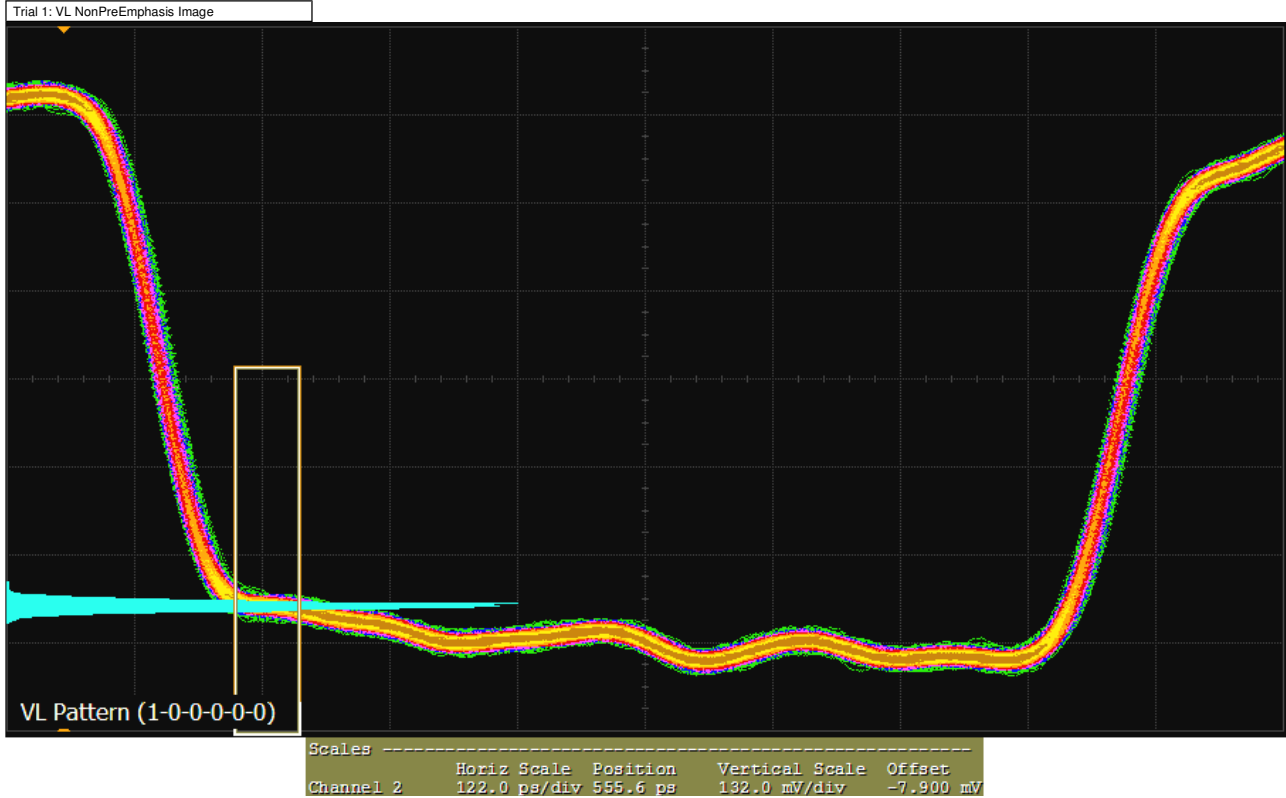
**✘ Lane 1 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

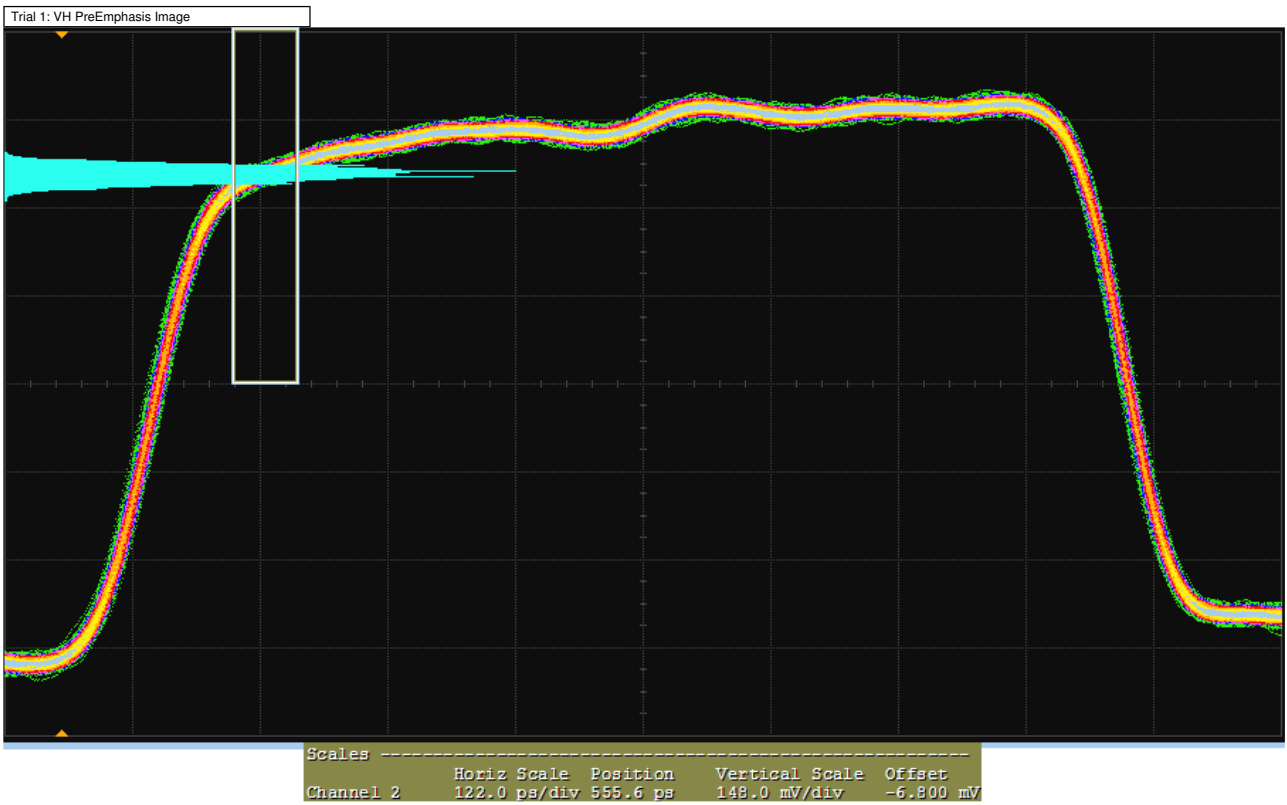
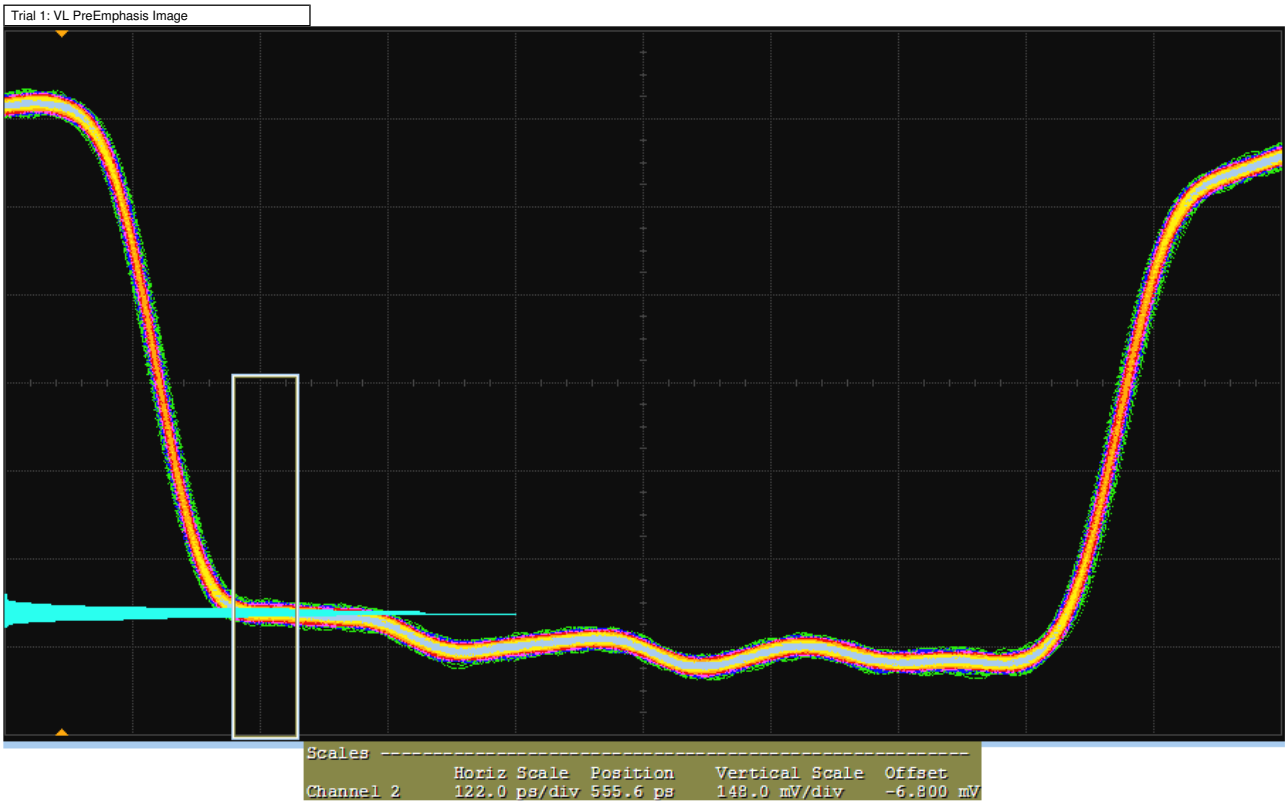
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 2.000 dB** | **PreEmphasis(Pre-emphasis 1) (Worst of 3 Trials) -53 mdB** | **# Trials Run: 3** | **Worst Trial: Trial 3**

Overall Summary + details of 3 worst trials

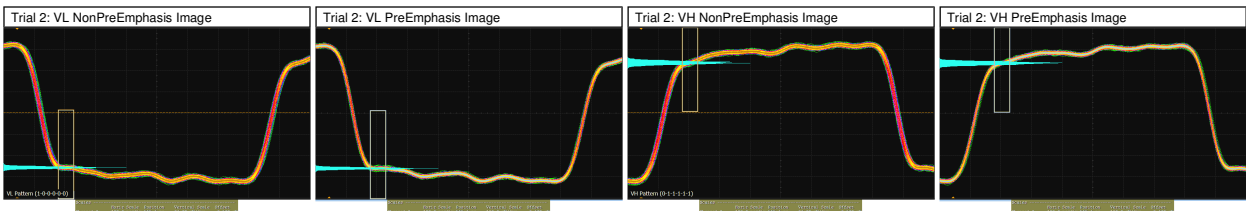
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	52.60 mdB	-97.38 %													
	StdDev	92.15 mdB	4.588 %													
	Range	168.7 mdB	8.400 %													
	Min	-53.17 mdB	-102.7 %													
	Max	115.5 mdB	-94.25 %													
	Sum	157.8 mdB	-292.2 %													
✘	Trial 1	95 mdB	-95.3% (See image)	(See image)	(See image)	(See image)	(See image)	1000	729.531 mV	890.581 mV	-1.733 dB	5.4 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 2	115 mdB	-94.3% (See image)	(See image)	(See image)	(See image)	(See image)	1000	584.648 mV	713.255 mV	-1.727 dB	5.4 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 3 (Worst)	-53 mdB	-102.7% (See image)	(See image)	(See image)	(See image)	(See image)	1000	396.794 mV	501.513 mV	-2.034 dB	5.4 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0

Trial 1

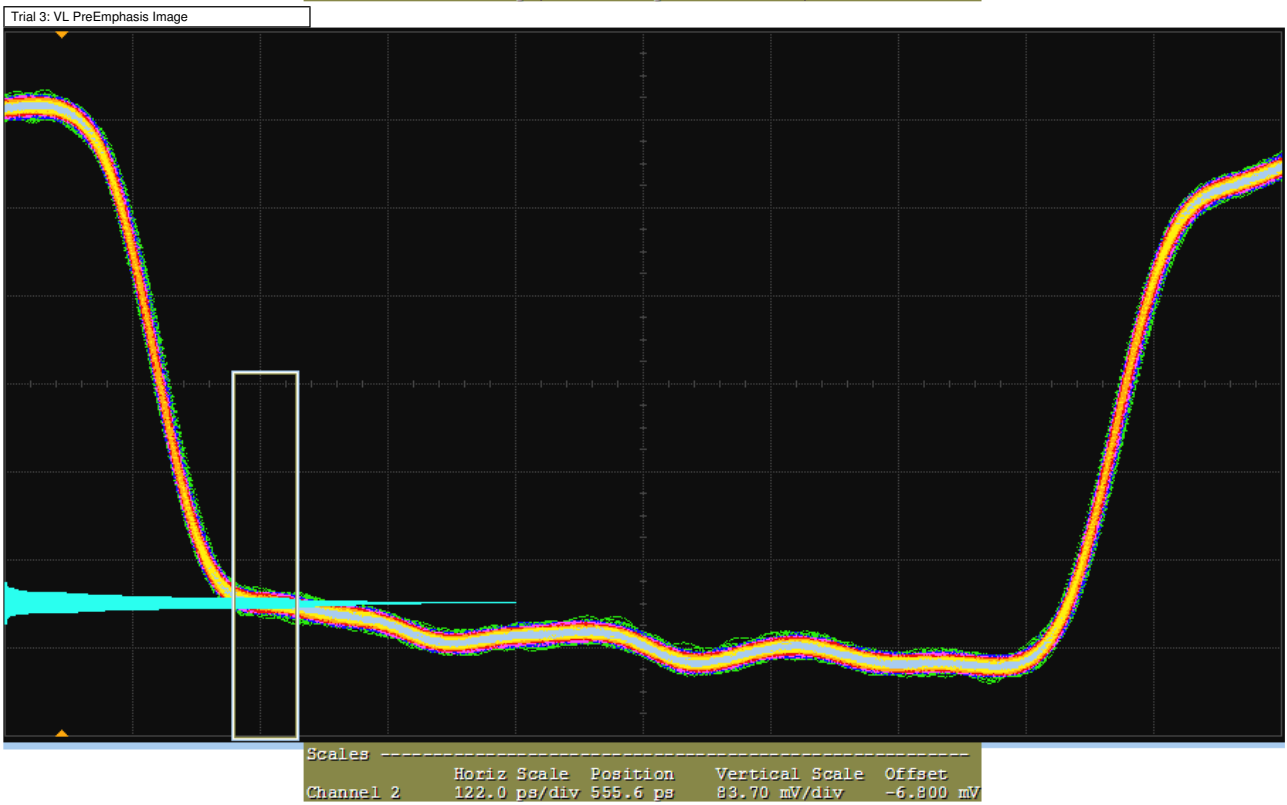
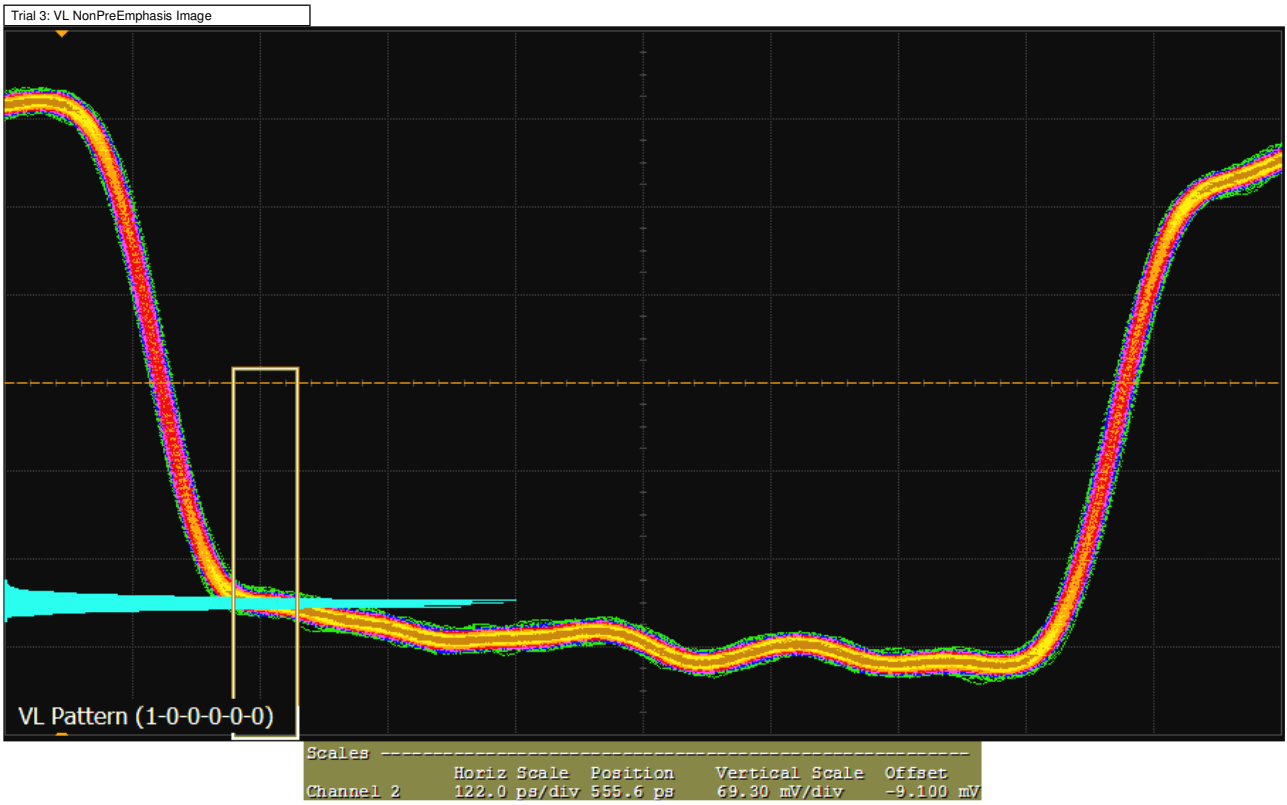


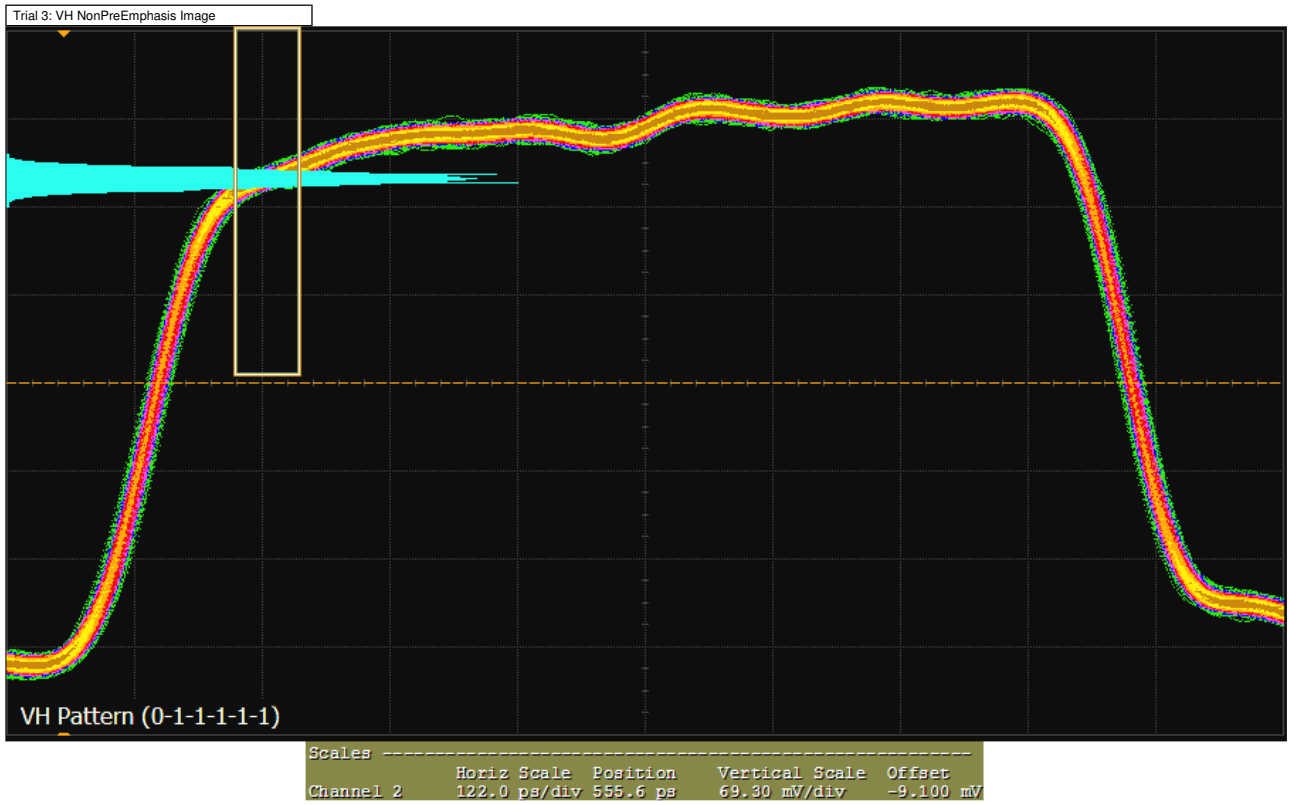


Trial 2



Trial 3





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✓ Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

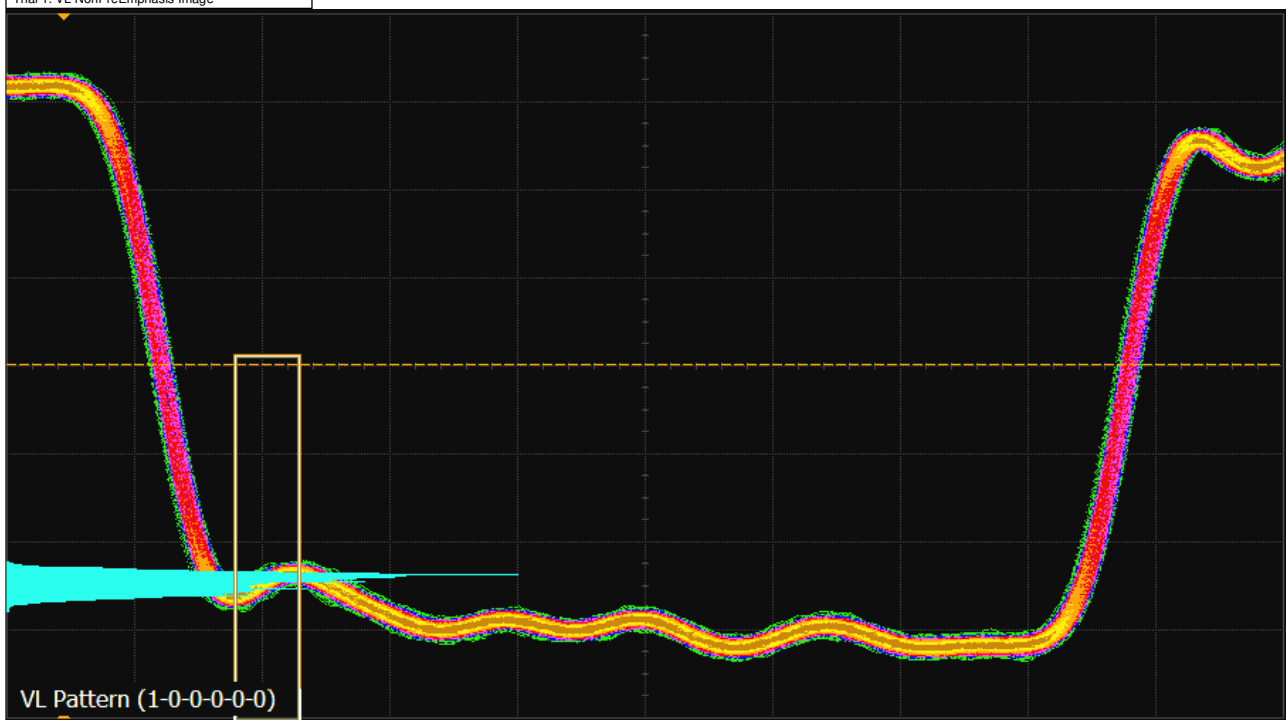
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 2.000 dB PreEmphasis(Pre-emphasis 1) (Worst of 3 Trials) 3.622 dB # Trials Run: 3 Worst Trial: Trial 1

Overall Summary + details of 3 worst trials

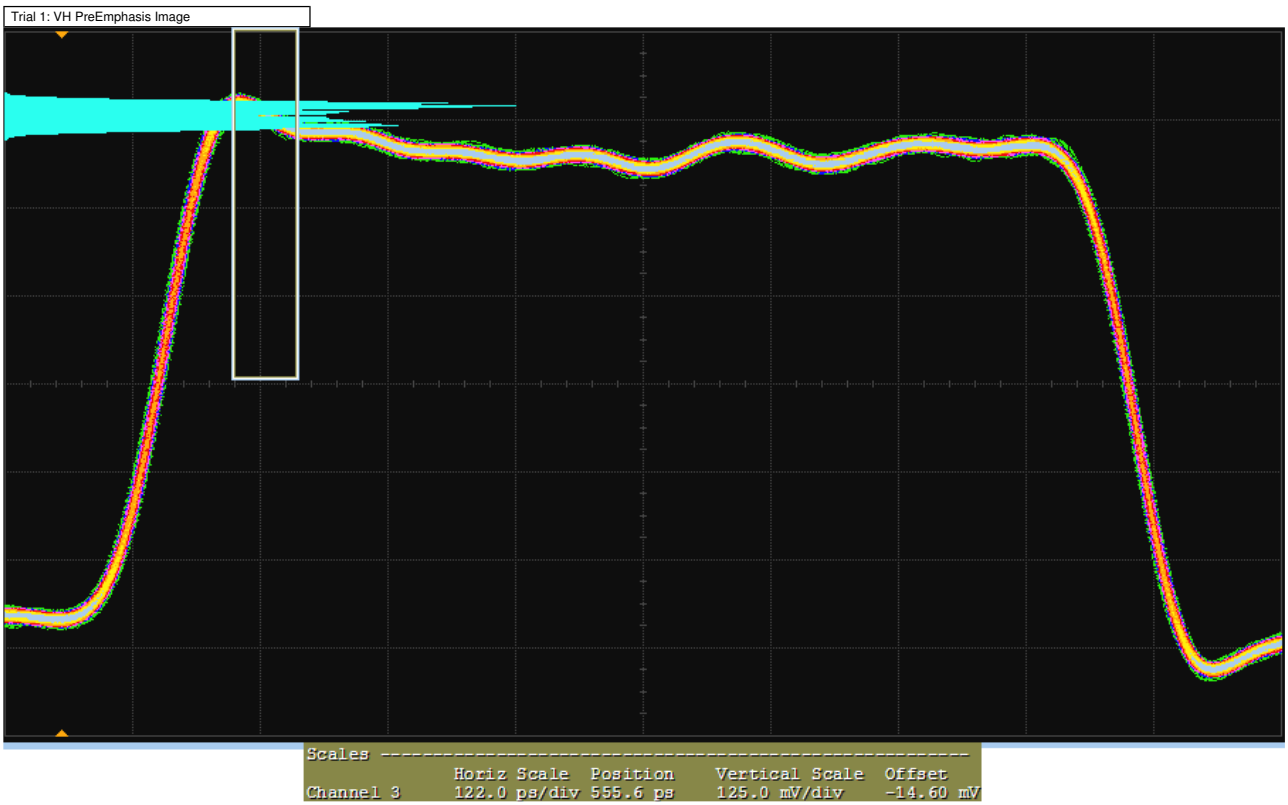
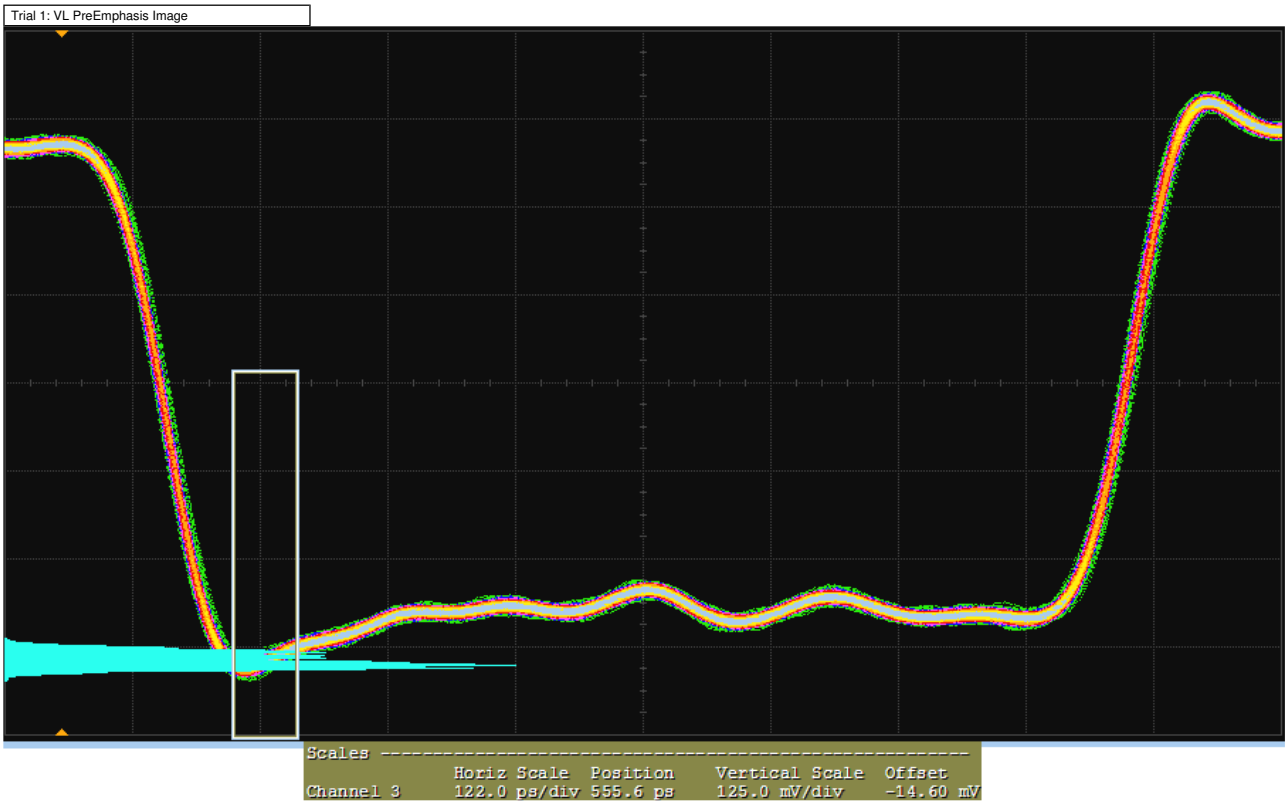
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	3.850 dB	92.50 %													
	StdDev	197.8 mdB	9.901 %													
	Range	356.4 mdB	17.85 %													
	Min	3.622 dB	81.10 %													
	Max	3.979 dB	98.95 %													
	Sum	11.55 dB	277.5 %													
✓	Trial 1 (Worst)	3.622 dB	81.1%	(See image)	(See image)	(See image)	(See image)	1000	863.309 mV	719.750 mV	1.580 dB	5.4 Gbps	2	Swing Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 2	3.979 dB	99.0%	(See image)	(See image)	(See image)	(See image)	1000	719.803 mV	583.012 mV	1.831 dB	5.4 Gbps	1	Swing Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	3.949 dB	97.5%	(See image)	(See image)	(See image)	(See image)	1000	499.881 mV	414.278 mV	1.631 dB	5.4 Gbps	0	Swing Pre-emphasis 1	SSC Disabled	Level 0

Trial 1

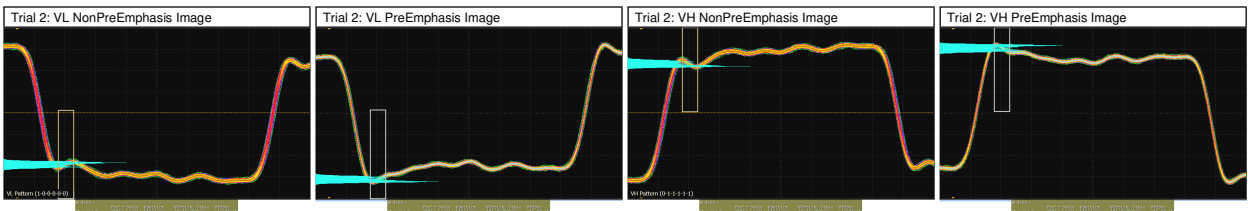
Trial 1: VL NonPreEmphasis Image



Channel	Horiz Scale	Position	Vertical Scale	Offset
3	122.0 ps/div	555.6 ps	134.0 mV/div	-7.800 mV

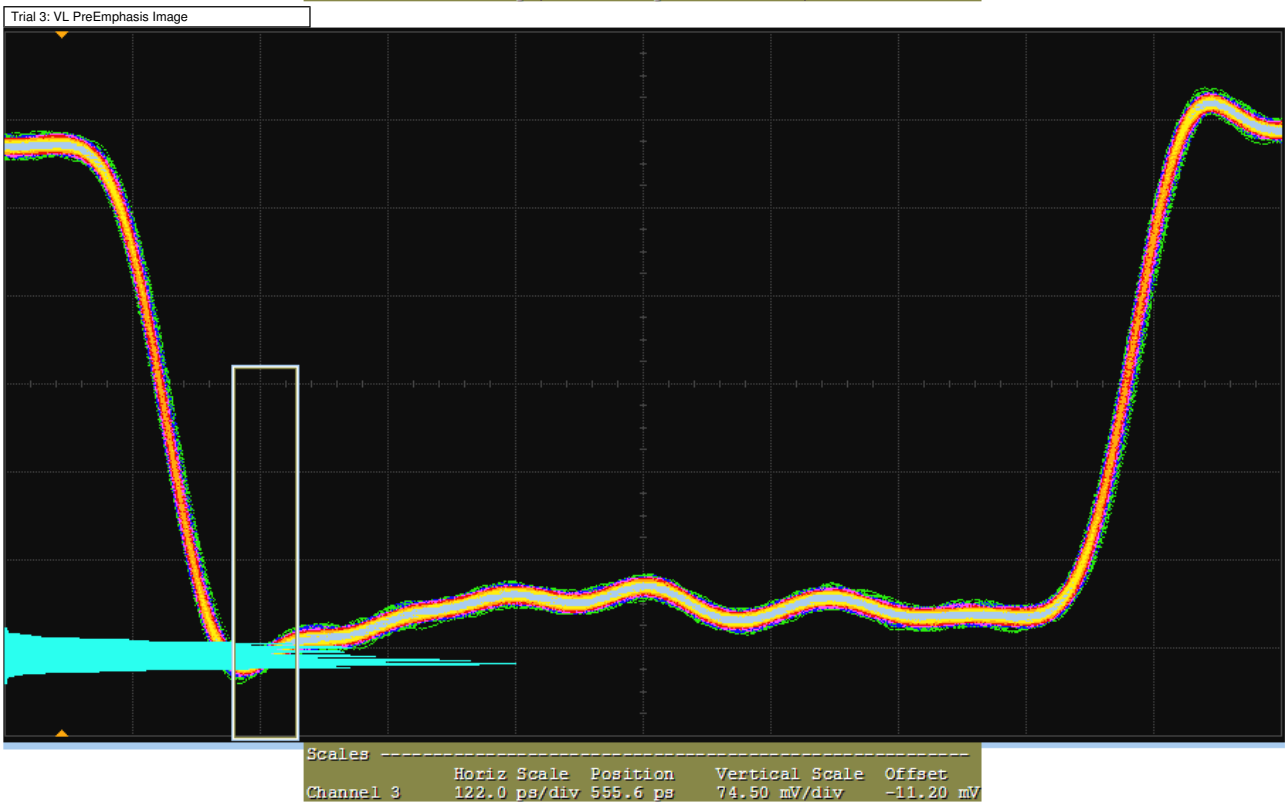
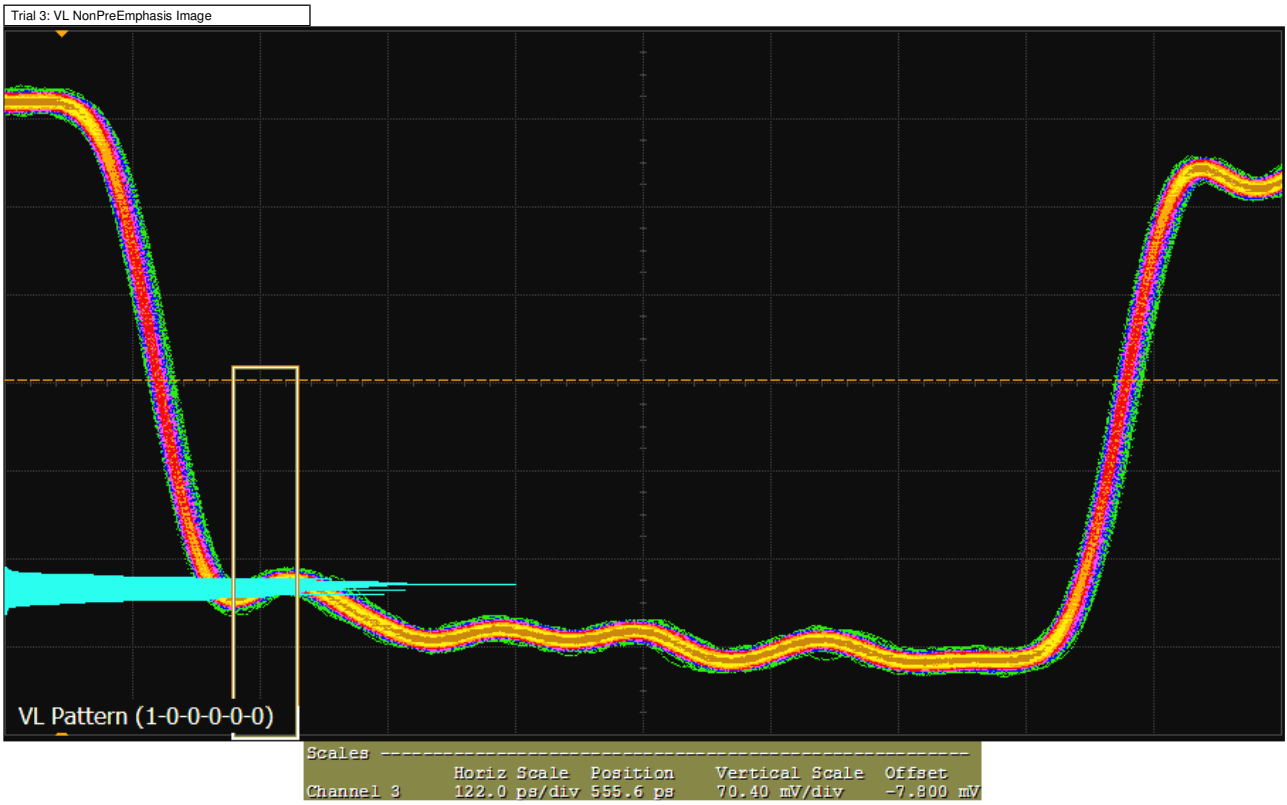


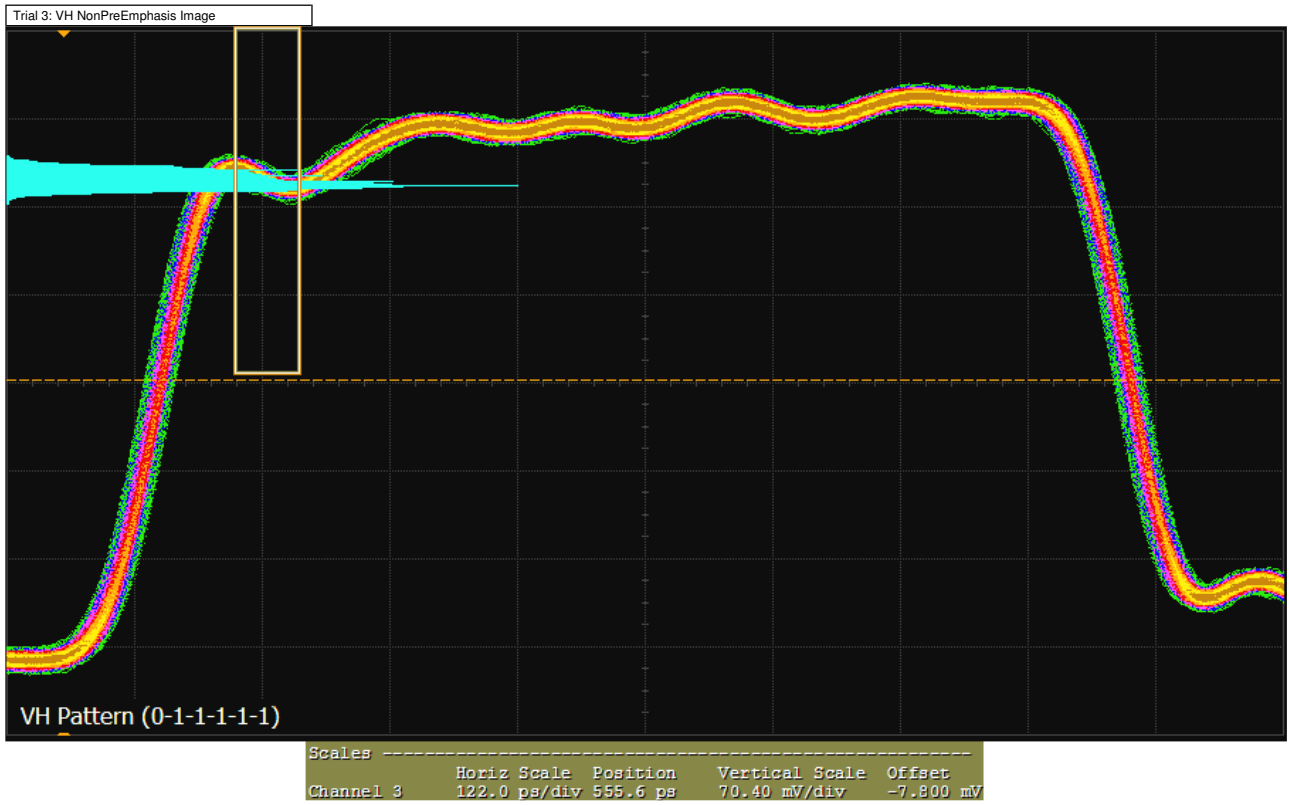
Trial 2



Trial 3







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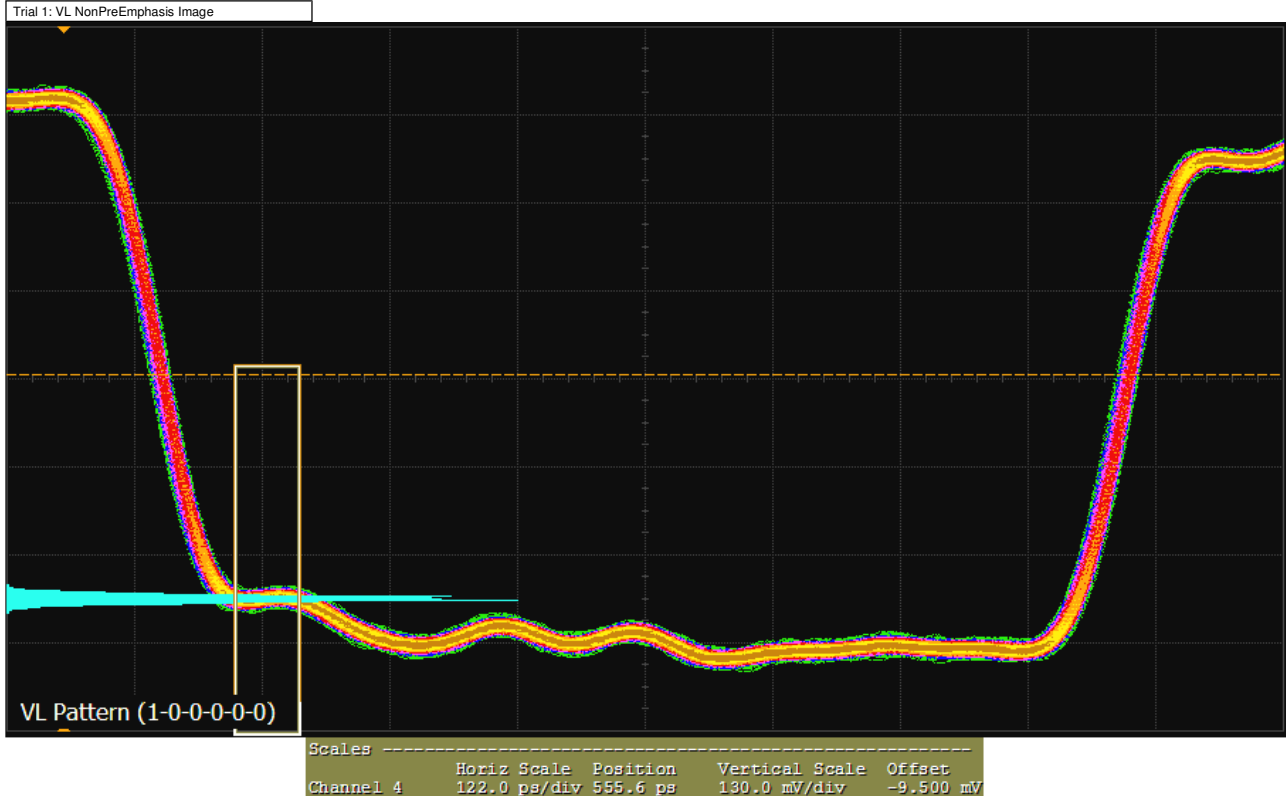
**✘ Lane 3 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

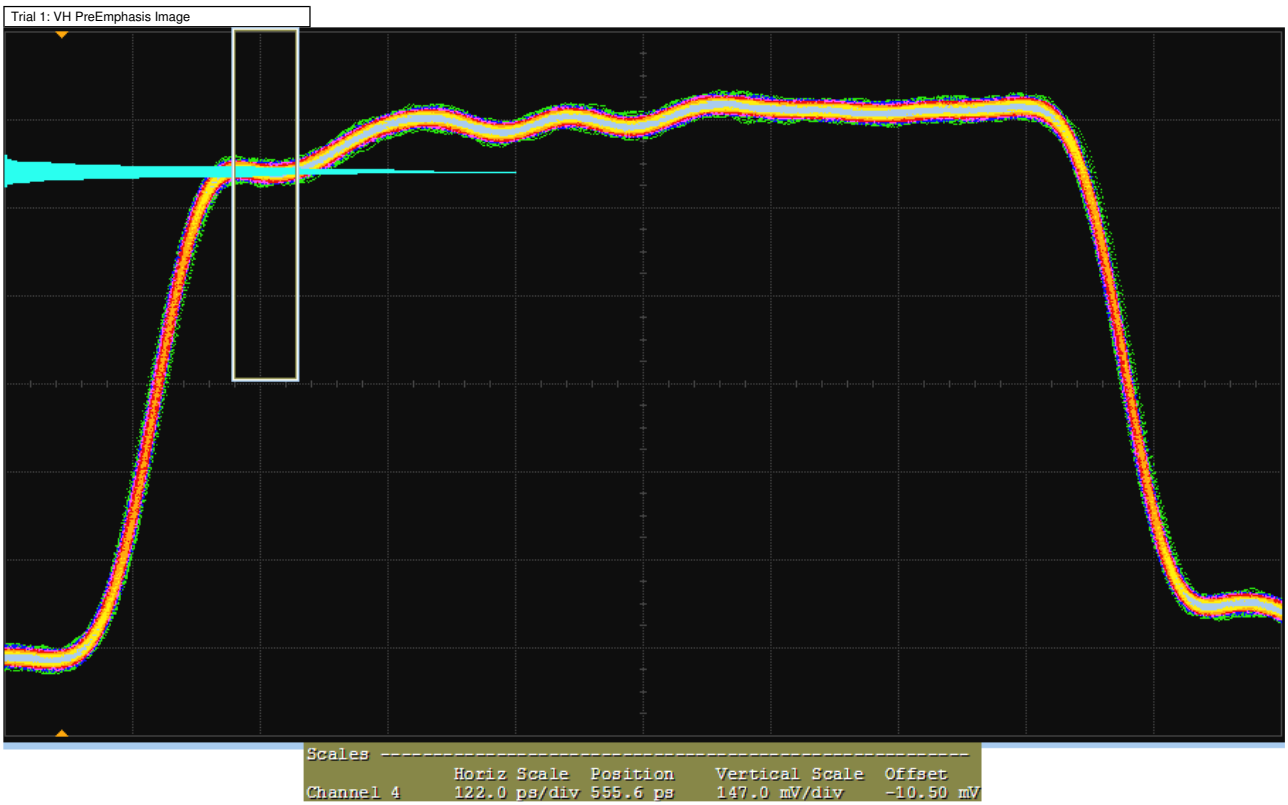
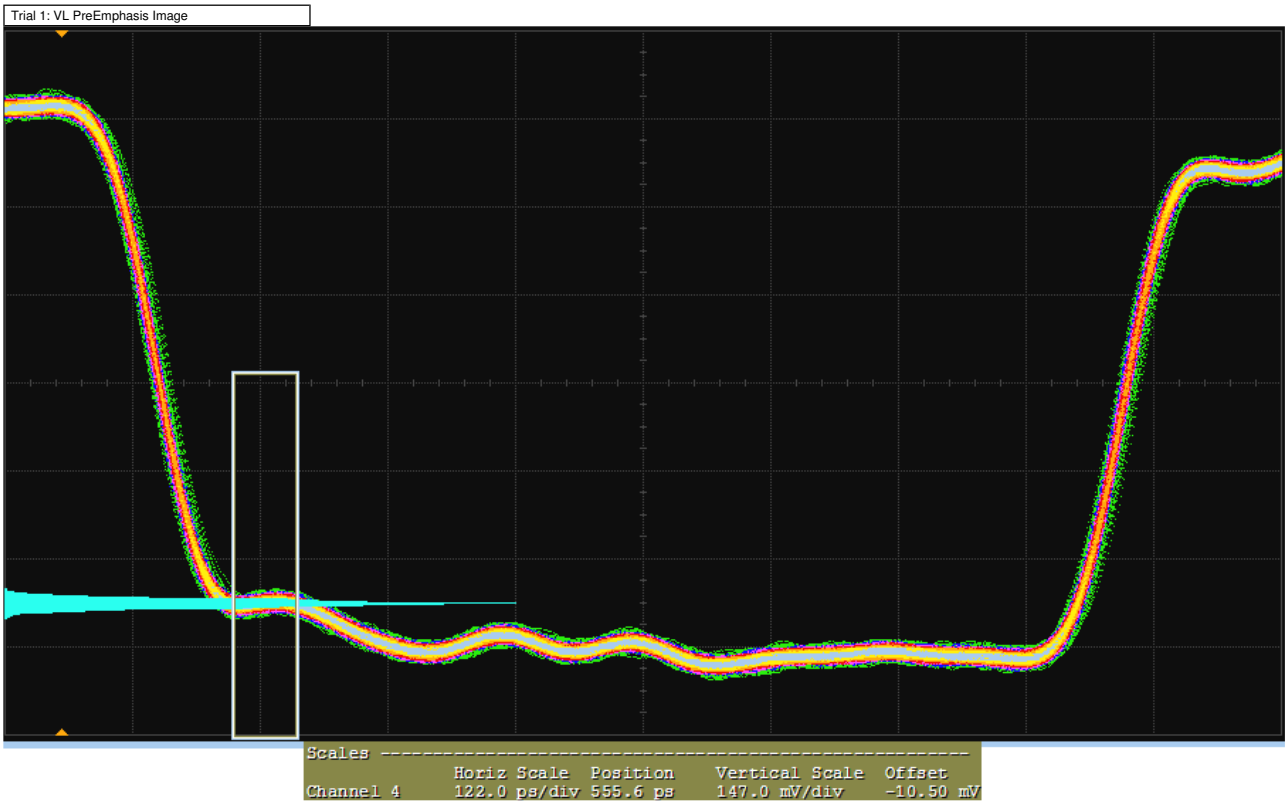
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 2.000 dB** | **PreEmphasis(Pre-emphasis 1) (Worst of 3 Trials) -109 mdB** | **# Trials Run: 3** | **Worst Trial: Trial 1**

Overall Summary + details of 3 worst trials

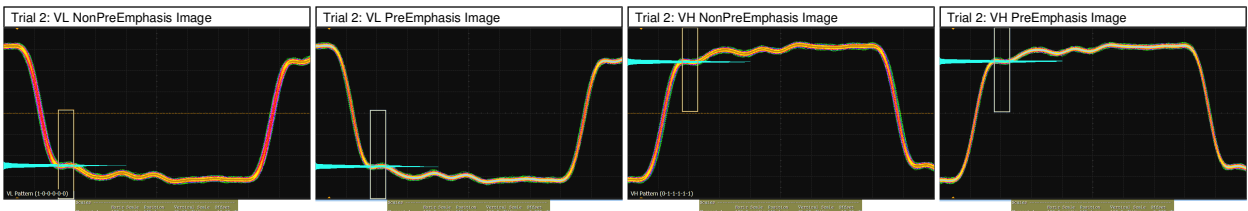
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-25.87 mdB	-101.3 %													
	StdDev	94.48 mdB	4.730 %													
	Range	185.7 mdB	9.300 %													
	Min	-108.7 mdB	-105.5 %													
	Max	77.02 mdB	-96.15 %													
	Sum	-77.62 mdB	-303.9 %													
✘	Trial 1 (Worst)	-109 mdB	105.5%	(See image)	(See image)	(See image)	(See image)	1000	717.814 mV	892.722 mV	-1.894 dB	5.4 Gbps	2	Swing Pre-emphasis 1	SSC Disabled	Level 0
✘	Trial 2	77 mdB	-96.2%	(See image)	(See image)	(See image)	(See image)	1000	574.172 mV	712.006 mV	-1.869 dB	5.4 Gbps	1	Swing Pre-emphasis 1	SSC Disabled	Level 0
✘	Trial 3	-46 mdB	102.3%	(See image)	(See image)	(See image)	(See image)	1000	389.967 mV	496.921 mV	-2.105 dB	5.4 Gbps	0	Swing Pre-emphasis 1	SSC Disabled	Level 0

Trial 1

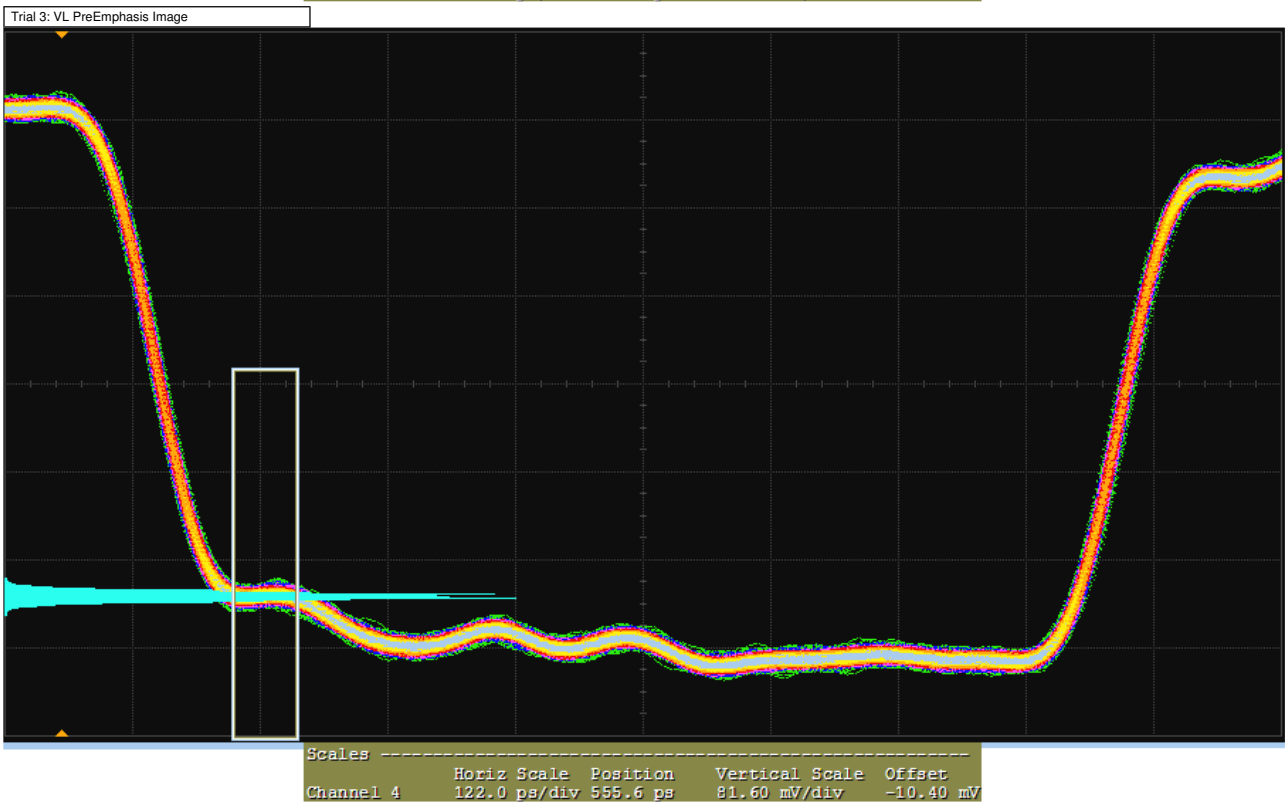
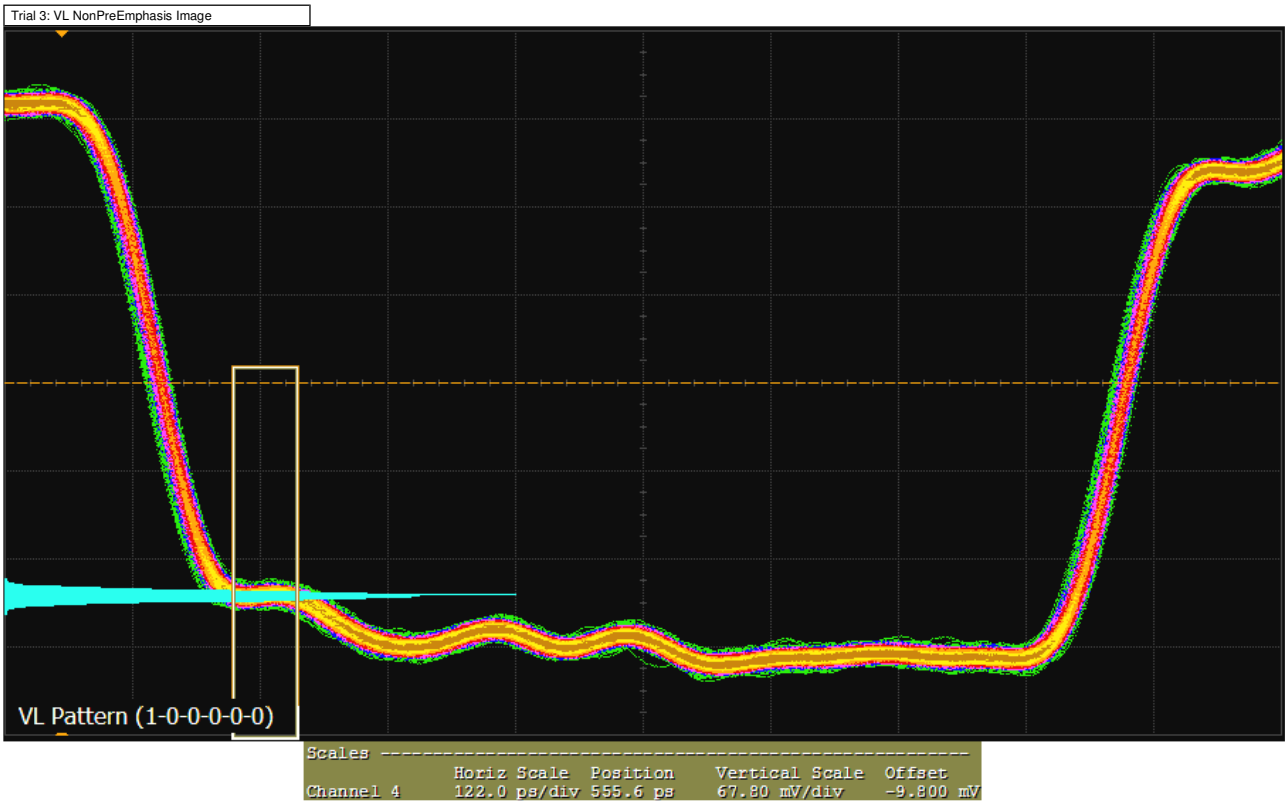


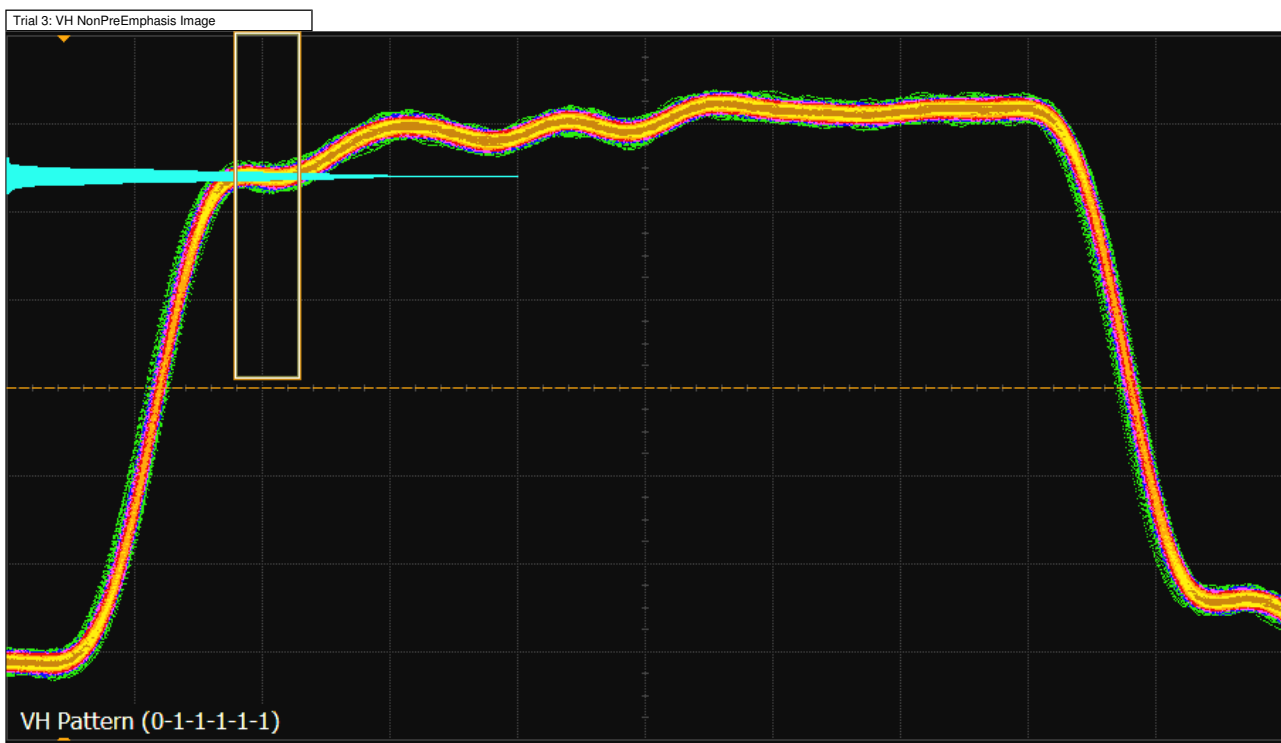


Trial 2



Trial 3





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✓ Lane 0 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2) *Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification*

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range 744 m

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 789.302 mV | VSwing Non-Transition Bit(Pre-emphasis 1) 587.262 mV | VSwing Non-Transition Bit(Pre-emphasis 2) (no value)

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) | VSwing Non-Transition Bit(Max) 587.262 mV | VSwing Non-Transition Bit(Min) 587.262 mV | BitRate 5.4 Gbps | Level Swing 2

PreEmphasis Pre-emphasis 1 | SSC SSC Disabled | PostCursor2 Level 0

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✓ Lane 1 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2) *Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification*

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range 1.134

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 785.031 mV | VSwing Non-Transition Bit(Pre-emphasis 1) 890.581 mV | VSwing Non-Transition Bit(Pre-emphasis 2) (no value)

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) | VSwing Non-Transition Bit(Max) 890.581 mV | VSwing Non-Transition Bit(Min) 890.581 mV | BitRate 5.4 Gbps | Level Swing 2

PreEmphasis Pre-emphasis 1 | SSC SSC Disabled | PostCursor2 Level 0

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✓ Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2) *Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification*

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range 900 m

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 800.097 mV | VSwing Non-Transition Bit(Pre-emphasis 1) 719.750 mV | VSwing Non-Transition Bit(Pre-emphasis 2) (no value)

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) | VSwing Non-Transition Bit(Max) 719.750 mV | VSwing Non-Transition Bit(Min) 719.750 mV | BitRate 5.4 Gbps | Level Swing 2

PreEmphasis Pre-emphasis 1 | SSC SSC Disabled | PostCursor2 Level 0

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✓ Lane 3 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2) *Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification*

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range 1.124

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 794.263 mV | VSwing Non-Transition Bit(Pre-emphasis 1) 892.722 mV | VSwing Non-Transition Bit(Pre-emphasis 2) (no value)

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) | VSwing Non-Transition Bit(Max) 892.722 mV | VSwing Non-Transition Bit(Min) 892.722 mV | BitRate 5.4 Gbps | Level Swing 2

PreEmphasis Pre-emphasis 1 | SSC SSC Disabled | PostCursor2 Level 0

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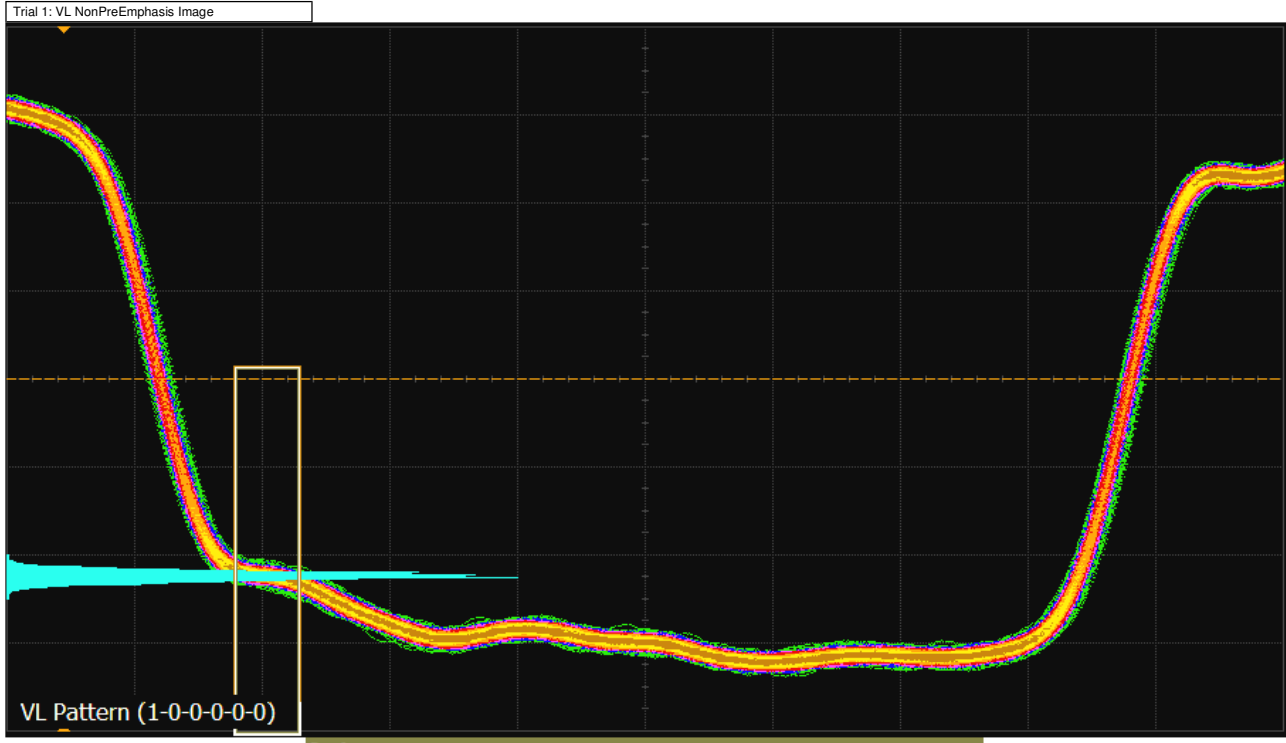
**✘ Lane 0 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 2 Trials) -2.523 dB** | **# Trials Run: 2** | **Worst Trial: Trial 1**

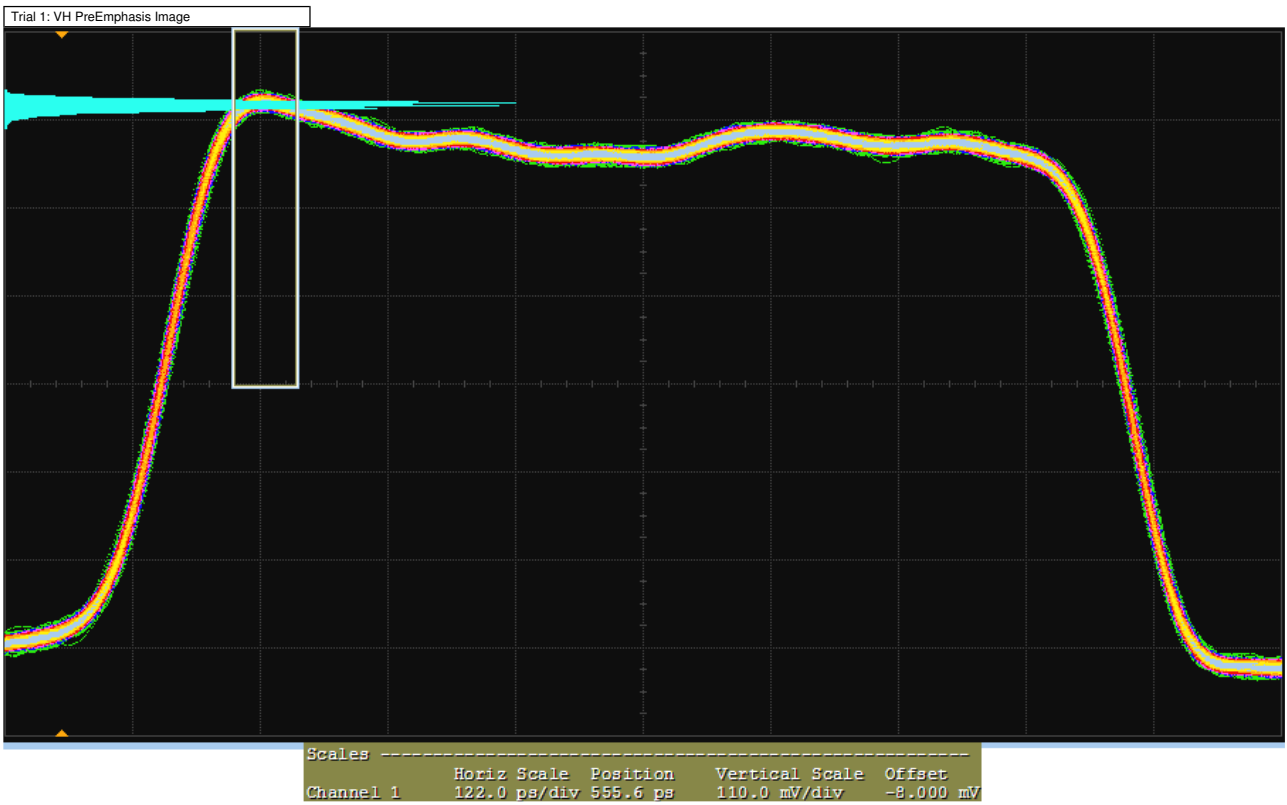
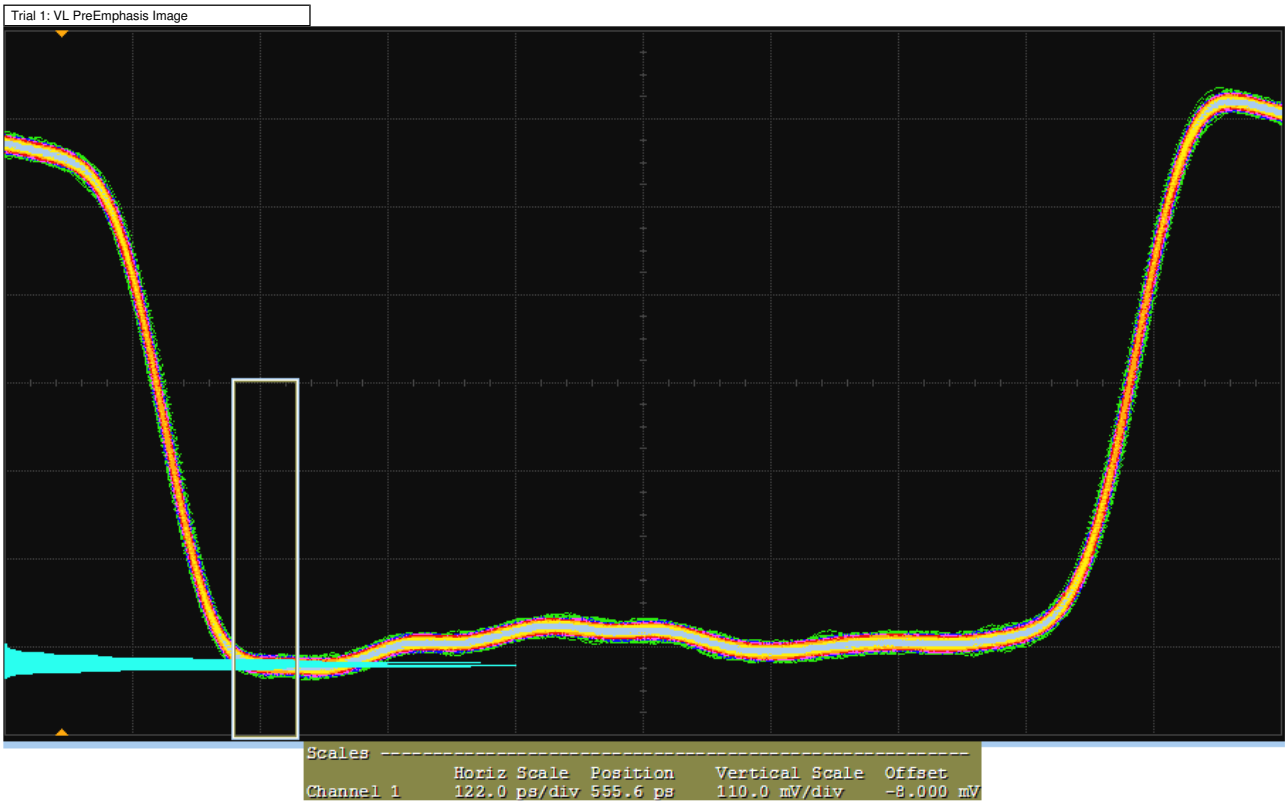
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	V Swing PreEmphasis (Transition Bit)	V Swing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-2.456 dB	-253.5 %													
	StdDev	93.52 mdB	5.878 %													
	Range	132.3 mdB	8.313 %													
	Min	-2.523 dB	-257.7 %													
	Max	-2.390 dB	-249.4 %													
	Sum	-4.913 dB	-507.1 %													
✘	Trial 1 (Worst)	-2.523 dB	-257.7%	(See image)	(See image)	(See image)	(See image)	1000	750.188 mV	663.263 mV	1.070 dB	5.4 Gbps	1	Swing Pre-emphasis 2	SSC Disabled	Level 0
✘	Trial 2	-2.390 dB	-249.4%	(See image)	(See image)	(See image)	(See image)	1000	537.010 mV	474.745 mV	1.070 dB	5.4 Gbps	0	Swing Pre-emphasis 2	SSC Disabled	Level 0

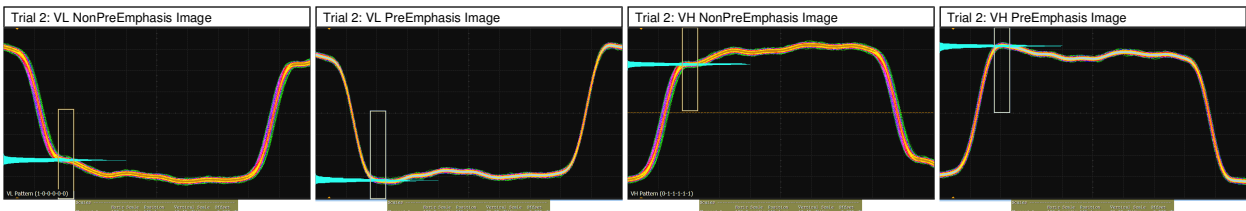
Trial 1



Channel 1	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	96.60 mV/div	-9.000 mV



Trial 2



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✓ Lane 1 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

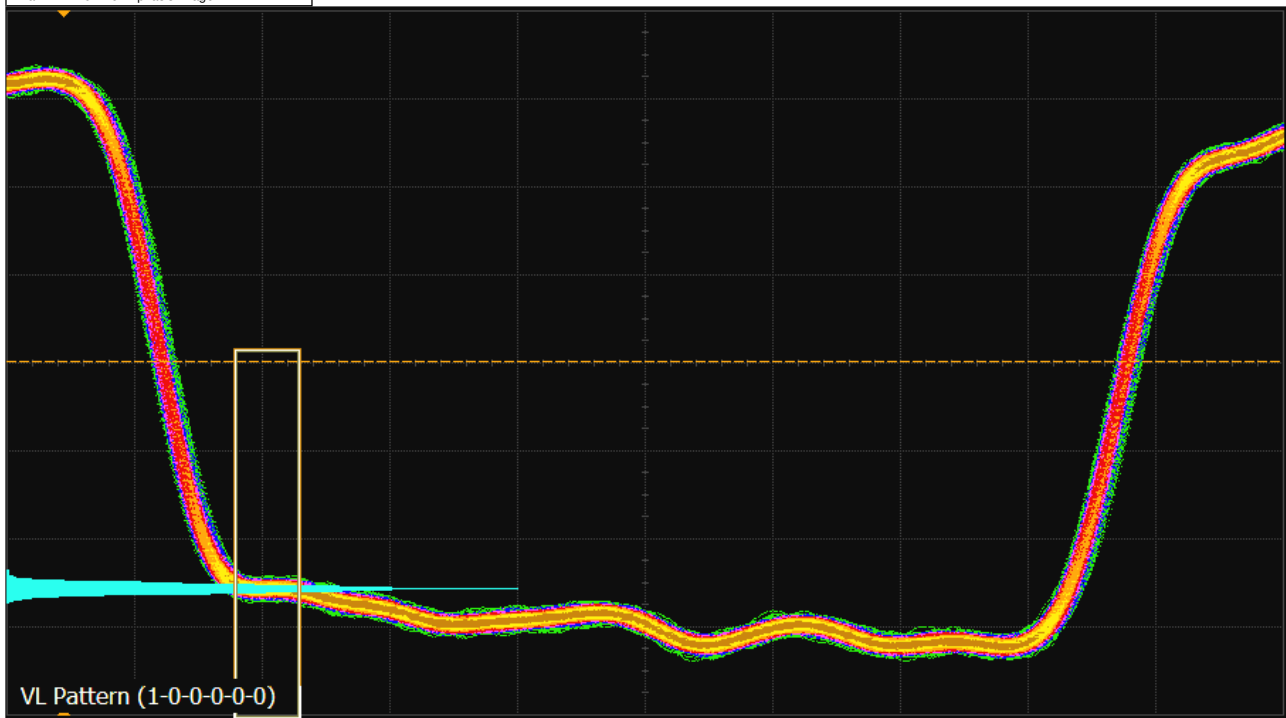
Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
**Pass Limits:** >= 1.600 dB | **PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 2 Trials)** 3.337 dB | **# Trials Run:** 2 | **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

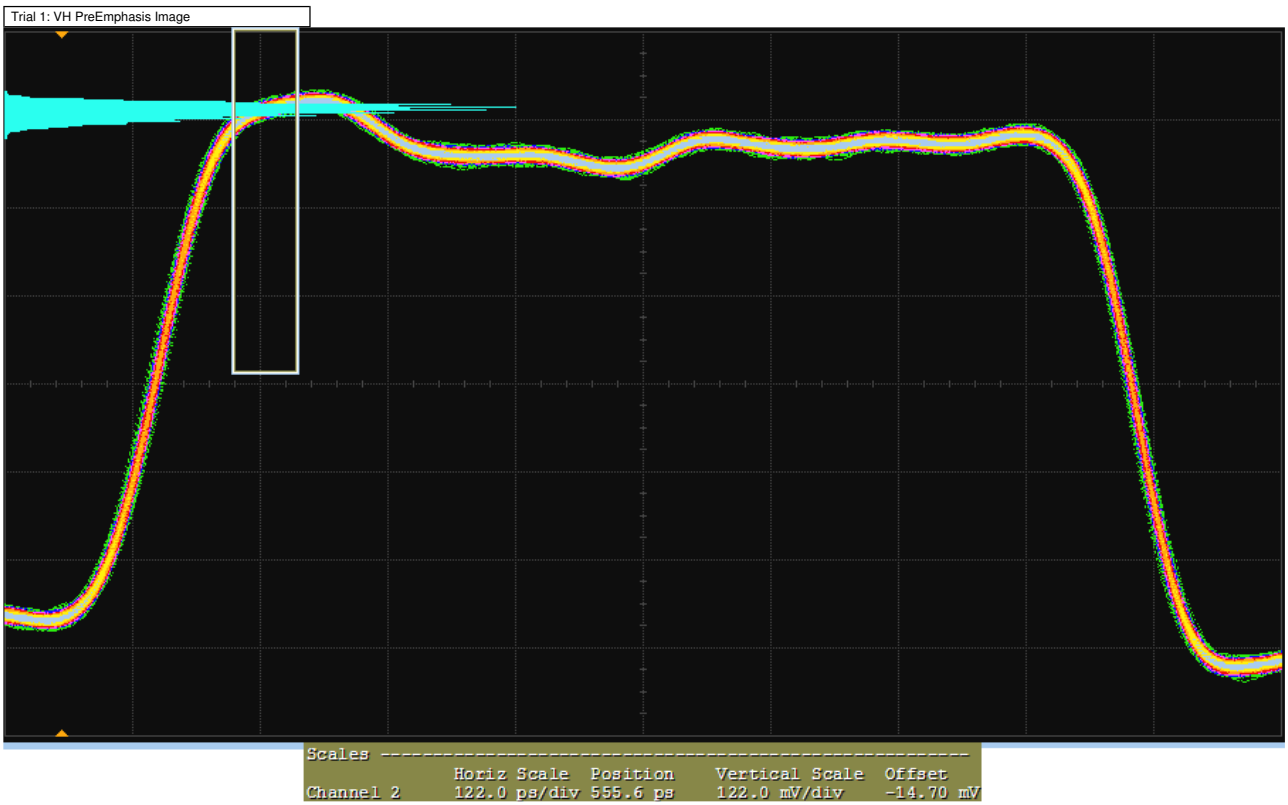
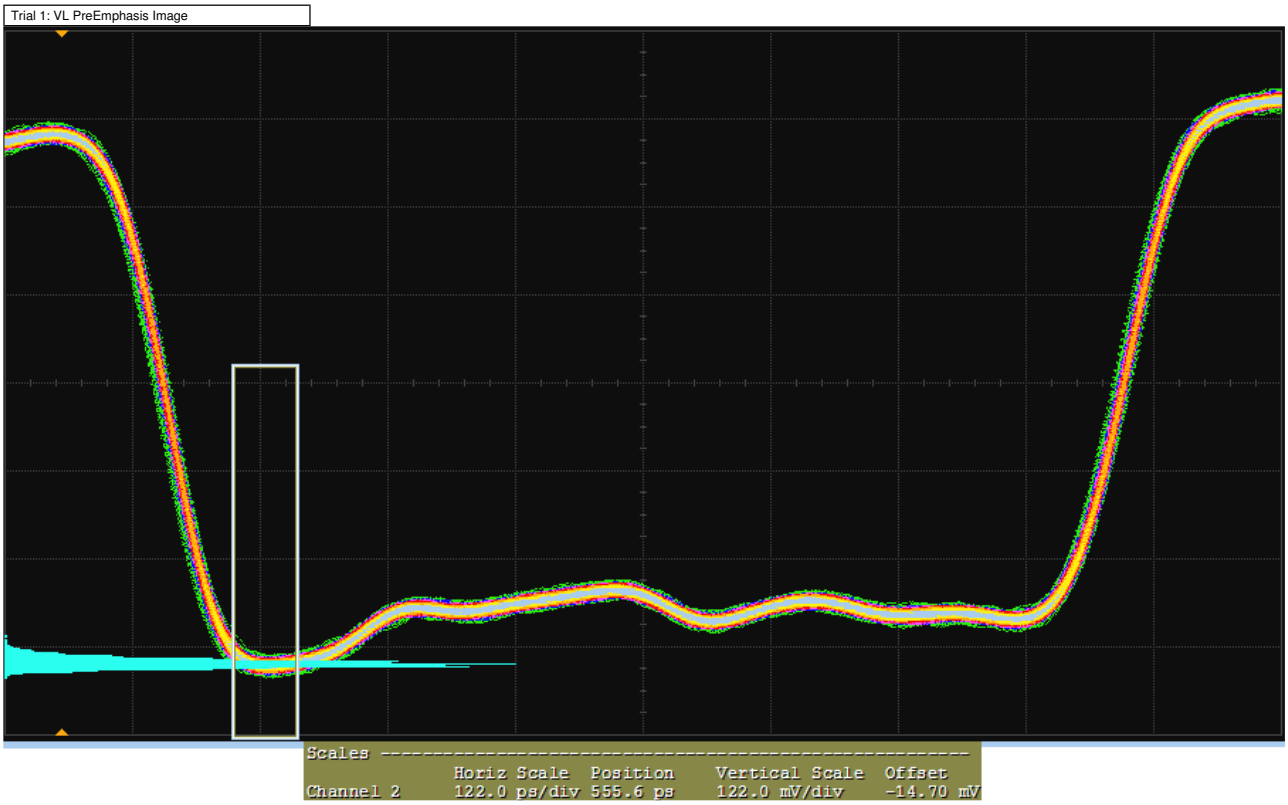
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	3.581 dB	123.8 %													
	StdDev	345.2 mdB	21.57 %													
	Range	488.1 mdB	30.50 %													
	Min	3.337 dB	108.6 %													
	Max	3.825 dB	139.1 %													
	Sum	7.161 dB	247.6 %													
✓	Trial 1 (Worst)	3.337 dB	108.6% (See image)	(See image)	(See image)	(See image)	(See image)	1000	804.647 mV	668.536 mV	1.610 dB	5.4 Gbps	1	Swing Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 2	3.825 dB	139.1% (See image)	(See image)	(See image)	(See image)	(See image)	1000	581.998 mV	473.588 mV	1.790 dB	5.4 Gbps	0	Swing Pre-emphasis 2	SSC Disabled	Level 0

Trial 1

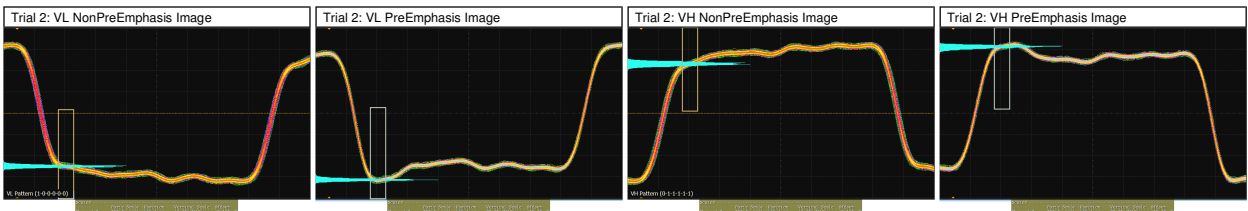
Trial 1: VL NonPreEmphasis Image



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	96.80 mV/div	-9.500 mV



Trial 2



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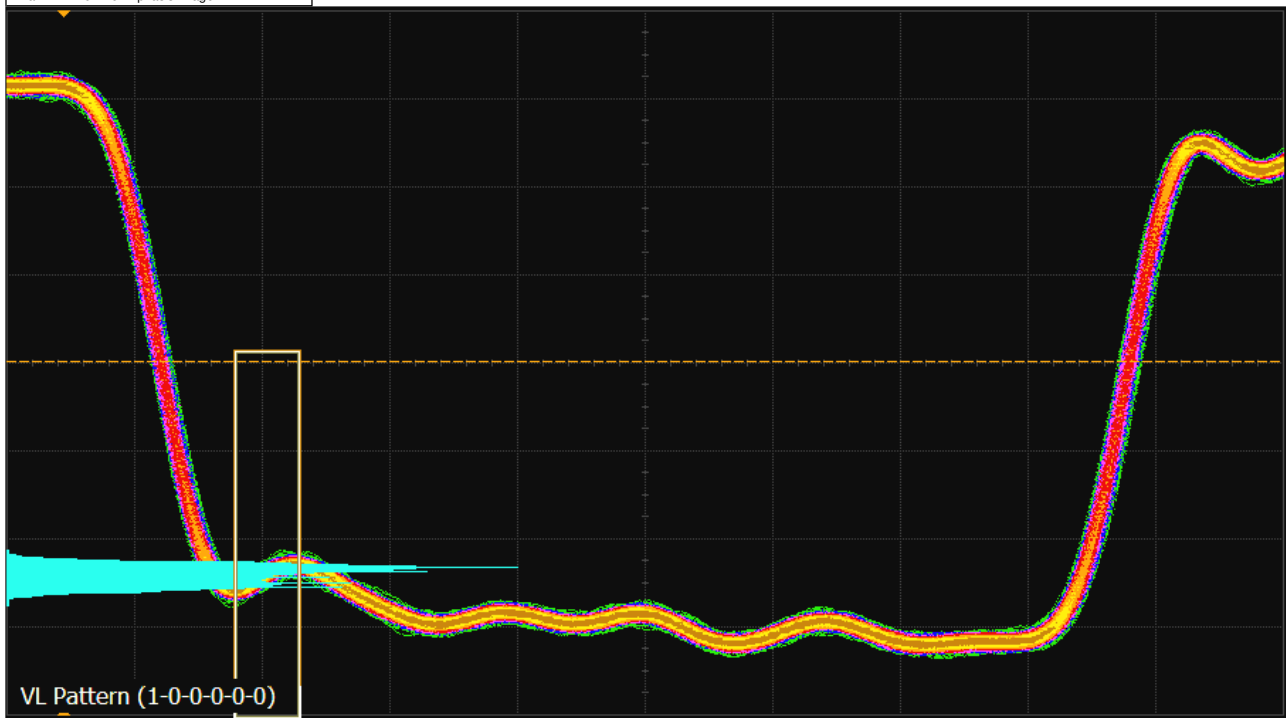
✓	<b>Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)</b>	Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification
Test Summary: Pass	Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.	
Pass Limits: >= 1.600 dB	PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 2 Trials) 2.109 dB	# Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

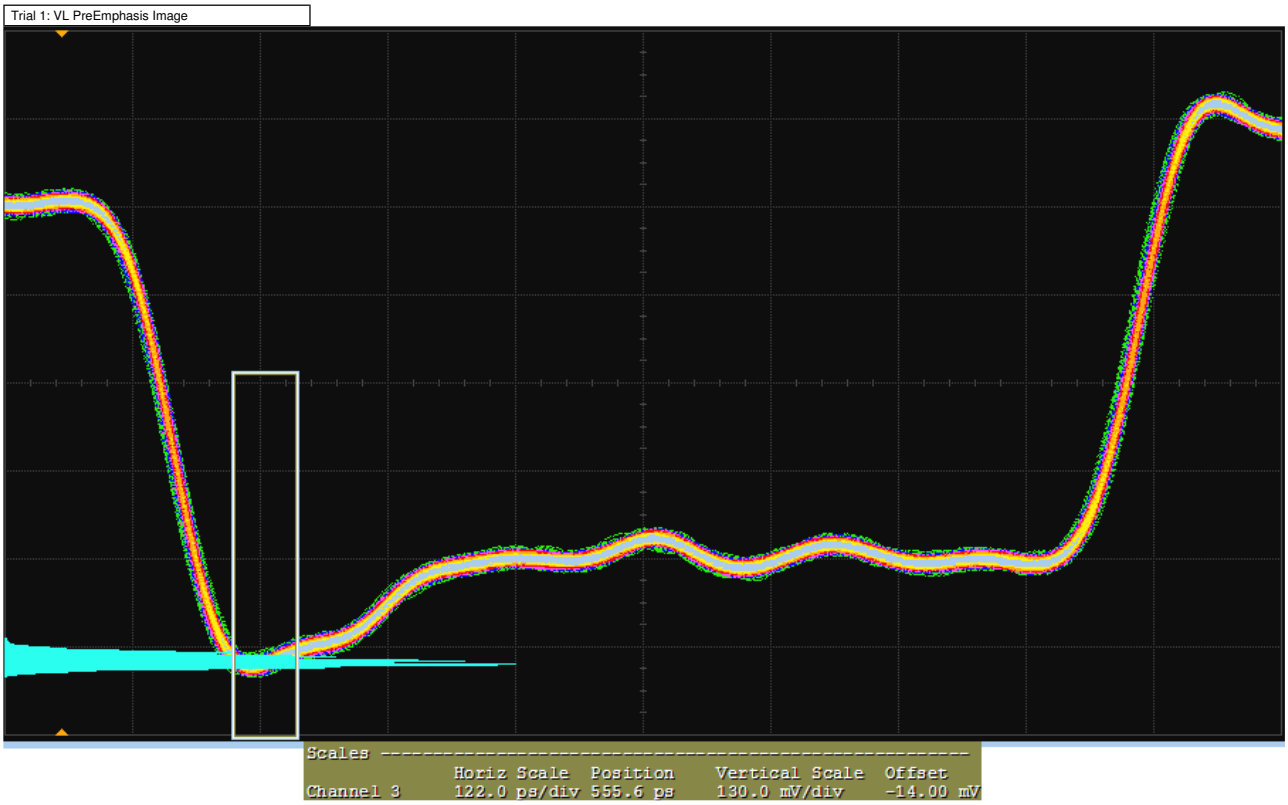
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	V Swing PreEmphasis (Transition Bit)	V Swing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	2.450 dB	53.09 %													
	StdDev	481.5 mdB	30.10 %													
	Range	681.0 mdB	42.56 %													
	Min	2.109 dB	31.81 %													
	Max	2.790 dB	74.38 %													
	Sum	4.899 dB	106.2 %													
✓	Trial 1 (Worst)	2.109 dB	31.8%	(See image)	(See image)	(See image)	(See image)	1000	886.090 mV	562.977 mV	3.940 dB	5.4 Gbps	1	Swing Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 2	2.790 dB	74.4%	(See image)	(See image)	(See image)	(See image)	1000	676.766 mV	406.783 mV	4.422 dB	5.4 Gbps	0	Swing Pre-emphasis 2	SSC Disabled	Level 0

Trial 1

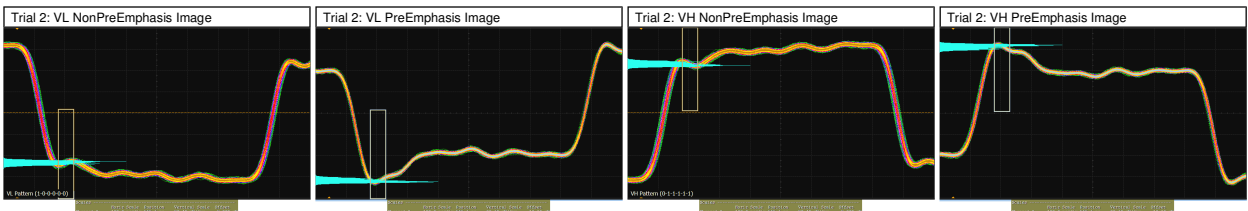
Trial 1: VL NonPreEmphasis Image



Channel	Horiz Scale	Position	Vertical Scale	Offset
3	122.0 ps/div	555.6 ps	98.60 mV/div	-6.900 mV



Trial 2



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**✘ Lane 3 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

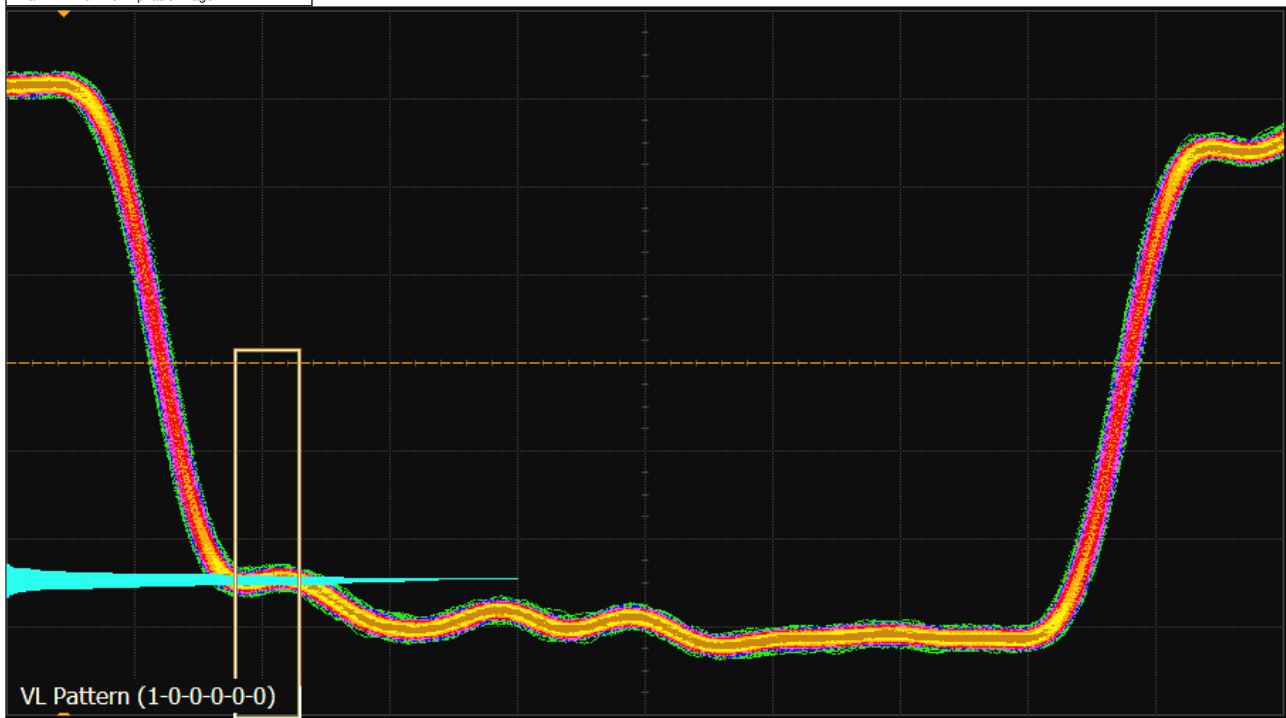
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 2 Trials) 155 mdB** | # Trials Run: **2** | Worst Trial: **Trial 1**

Overall Summary + details of 2 worst trials

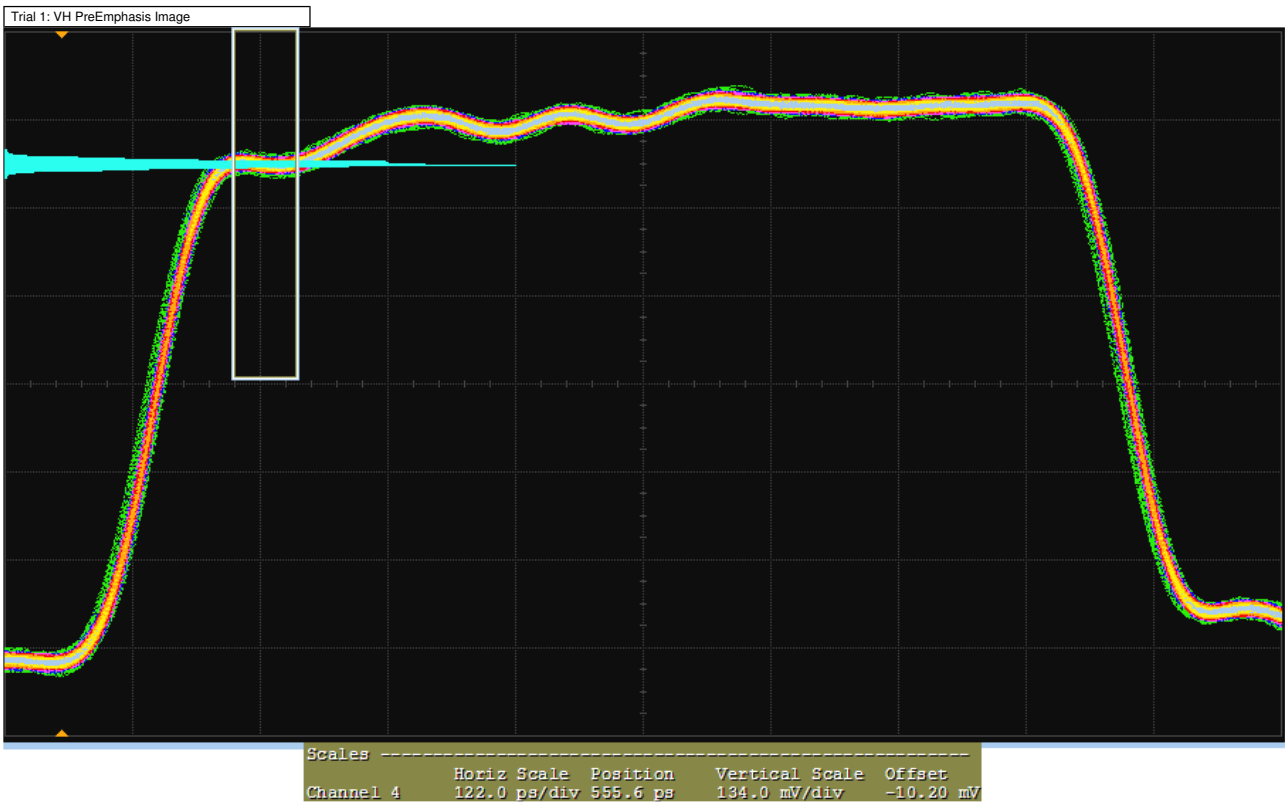
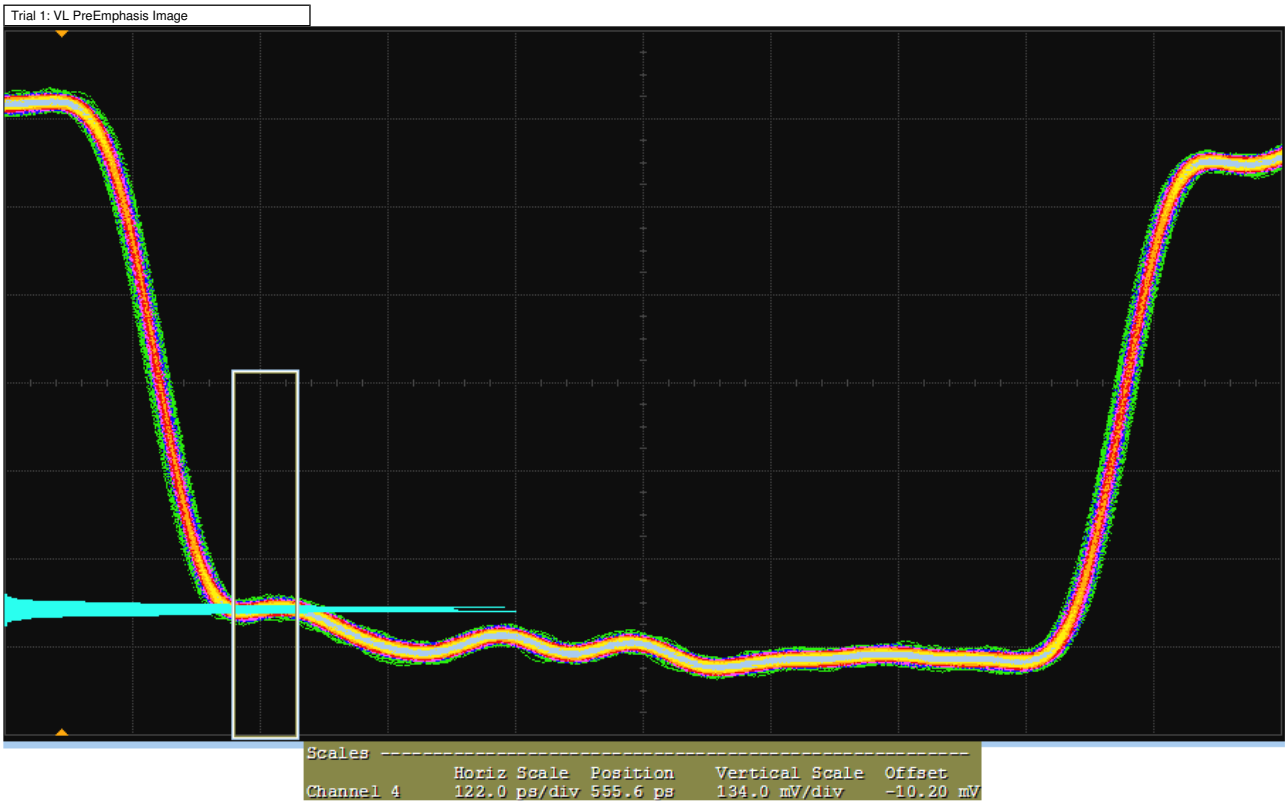
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	221.3 mdB	-86.16 %													
	StdDev	93.80 mdB	5.878 %													
	Range	132.7 mdB	8.313 %													
	Min	155.0 mdB	-90.31 %													
	Max	287.7 mdB	-82.00 %													
	Sum	442.7 mdB	-172.3 %													
✘	Trial 1 (Worst)	155 mdB	-90.3% (See image)	(See image)	(See image)	(See image)	(See image)	1000	679.317 mV	827.493 mV	-1.714 dB	5.4 Gbps	1	Swing Pre-emphasis 2	SSC Disabled	Level 0
✘	Trial 2	288 mdB	-82.0% (See image)	(See image)	(See image)	(See image)	(See image)	1000	469.560 mV	578.852 mV	-1.818 dB	5.4 Gbps	0	Swing Pre-emphasis 2	SSC Disabled	Level 0

Trial 1

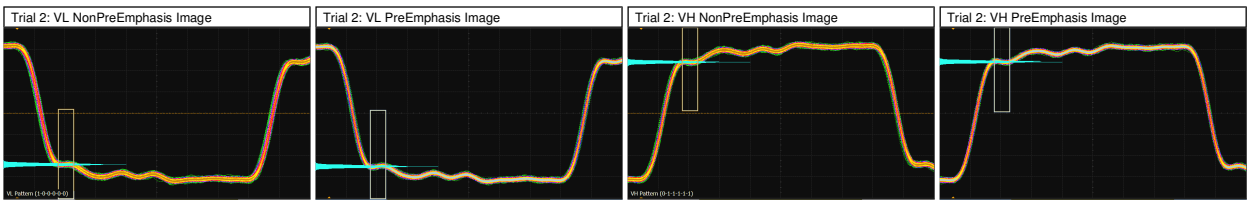
Trial 1: VL NonPreEmphasis Image



Channel	Horiz Scale	Position	Vertical Scale	Offset
4	122.0 ps/div	555.6 ps	95.50 mV/div	-10.30 mV



Trial 2



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✓ Lane 0 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)

Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: **>= 708 m** **Non-Transition Voltage Range 835 m**

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 578.674 mV VSwing Non-Transition Bit(Pre-emphasis 1) 483.377 mV VSwing Non-Transition Bit(Pre-emphasis 2) 663.263 mV

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) VSwing Non-Transition Bit(Max) 663.263 mV VSwing Non-Transition Bit(Min) 483.377 mV BitRate 5.4 Gbps Level Swing 1

PreEmphasis Pre-emphasis 2 SSC SSC Disabled PostCursor2 Level 0

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**✓ Lane 1 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)** *Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification*

Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: **>= 708 m** **Non-Transition Voltage Range 1.151**

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 581.046 mV VSwing Non-Transition Bit(Pre-emphasis 1) 713.255 mV VSwing Non-Transition Bit(Pre-emphasis 2) 668.536 mV

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) VSwing Non-Transition Bit(Max) 713.255 mV VSwing Non-Transition Bit(Min) 668.536 mV BitRate 5.4 Gbps Level Swing 1

PreEmphasis Pre-emphasis 2 SSC SSC Disabled PostCursor2 Level 0

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**✓ Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)** *Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification*

Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: **>= 708 m** **Non-Transition Voltage Range 947 m**

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 594.375 mV VSwing Non-Transition Bit(Pre-emphasis 1) 583.012 mV VSwing Non-Transition Bit(Pre-emphasis 2) 562.977 mV

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) VSwing Non-Transition Bit(Max) 583.012 mV VSwing Non-Transition Bit(Min) 562.977 mV BitRate 5.4 Gbps Level Swing 1

PreEmphasis Pre-emphasis 2 SSC SSC Disabled PostCursor2 Level 0

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**✓ Lane 3 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)** *Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification*

Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: **>= 708 m** **Non-Transition Voltage Range 1.229**

**Result Details**

VSwing Non-Transition Bit(Pre-emphasis 0) 579.270 mV VSwing Non-Transition Bit(Pre-emphasis 1) 712.006 mV VSwing Non-Transition Bit(Pre-emphasis 2) 827.493 mV

VSwing Non-Transition Bit(Pre-emphasis 3) (no value) VSwing Non-Transition Bit(Max) 827.493 mV VSwing Non-Transition Bit(Min) 712.006 mV BitRate 5.4 Gbps Level Swing 1

PreEmphasis Pre-emphasis 2 SSC SSC Disabled PostCursor2 Level 0

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**✓ Lane 0 - D10.2 Total Jitter Test with No Cable Model (TP3\_EQ)** *Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification*

Test Summary: **Pass** Test Description: To evaluate the Total Jitter with No Cable Model (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: **<= 400.000 mUI** **D10.2 Total Jitter (TP3\_EQ No Cable) 104.600 mUI**

**Result Details**

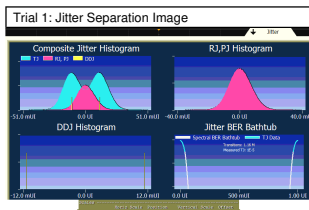
Jitter Separation Image (See image) Edges 1.00000000 M Total Jitter (TJ) 104.6 mUI Total Jitter (TJ) in ps 19.3704 ps Periodic Jitter (PJ rms) 4.1 mUI Periodic Jitter (PJ p-p) 12.9 mUI

Deterministic Jitter (DJ) 33.7 mUI Random Jitter (RJ) 5.8 mUI ISI Jitter (ISI) 0.0000 UI Data Dependent Jitter (DDJ) 22.8 mUI Bit Error Rate (BER) E9 Test Mode Compliance

Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 0

PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1



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**✓ Lane 1 - D10.2 Total Jitter Test with No Cable Model (TP3\_EQ)** *Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification*

Test Summary: **Pass** Test Description: To evaluate the Total Jitter with No Cable Model (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: **<= 400.000 mUI** **D10.2 Total Jitter (TP3\_EQ No Cable) 85.200 mUI**

**Result Details**

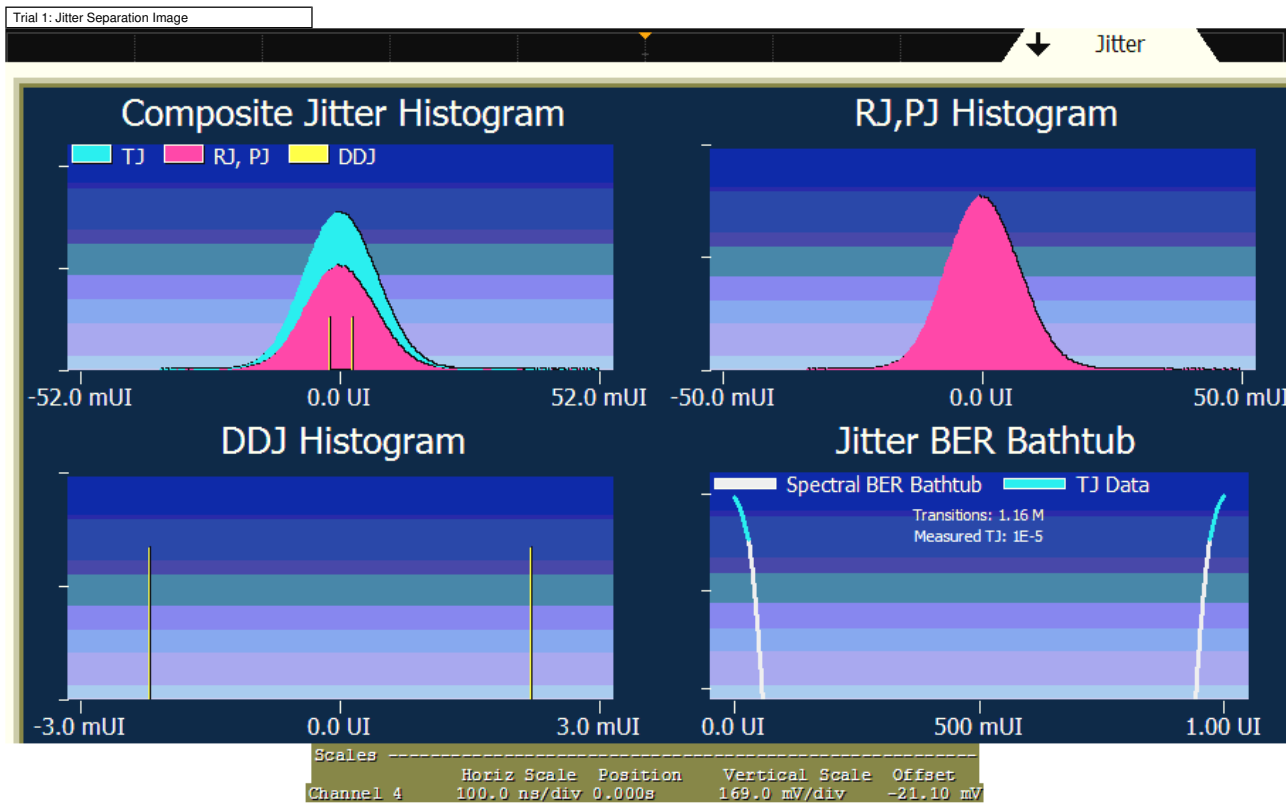
Jitter Separation Image (See image) Edges 1.00000000 M Total Jitter (TJ) 85.2 mUI Total Jitter (TJ) in ps 15.7777 ps Periodic Jitter (PJ rms) 3.9 mUI Periodic Jitter (PJ p-p) 15.1 mUI

Deterministic Jitter (DJ) 17.1 mUI Random Jitter (RJ) 5.6 mUI ISI Jitter (ISI) 0.0000 UI Data Dependent Jitter (DDJ) 4.4 mUI Bit Error Rate (BER) E9 Test Mode Compliance

Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 0

PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1



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✓ Lane 2 - D10.2 Total Jitter Test with No Cable Model (TP3\_EQ) *Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification*

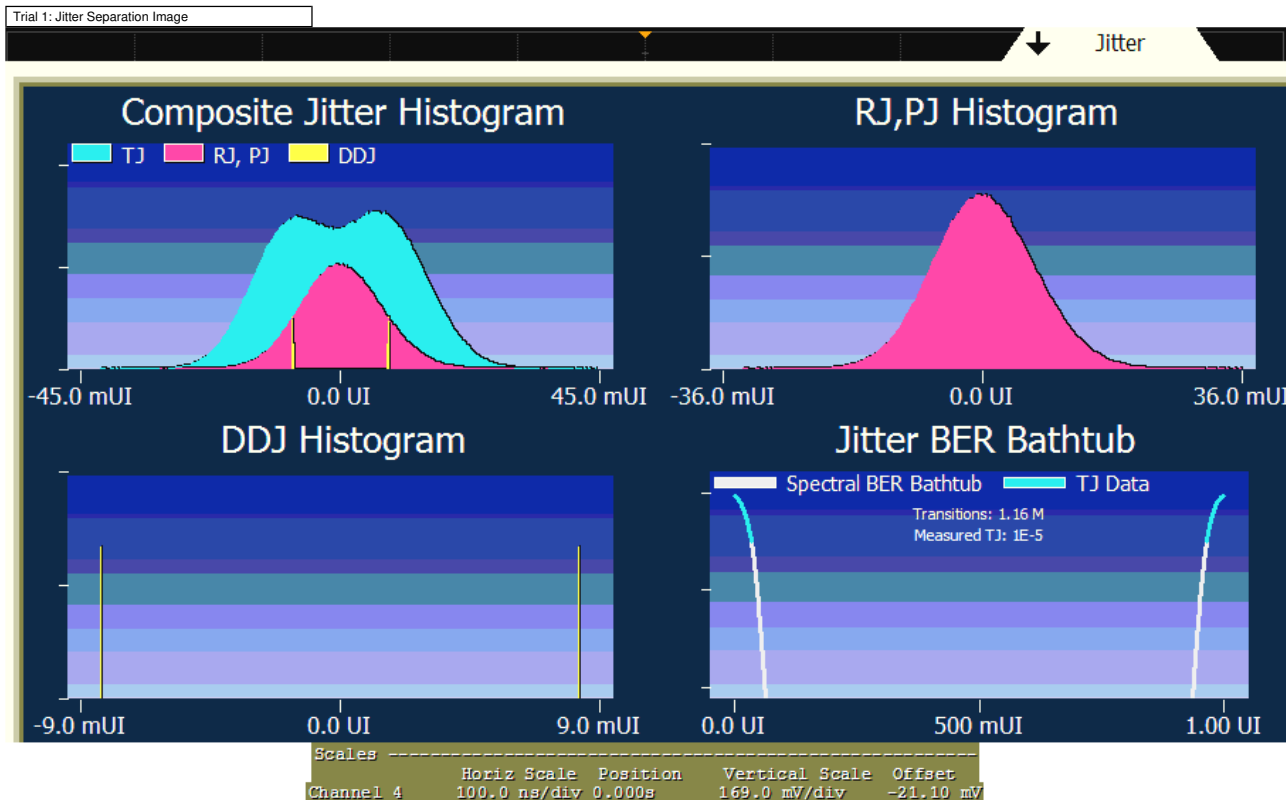
Test Summary: **Pass** Test Description: To evaluate the Total Jitter with No Cable Model (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 400.000 mUI Lane 2 D10.2 Total Jitter (TP3\_EQ No Cable) 96.300 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.00000000 M	Total Jitter (TJ) 96.3 mUI	Total Jitter (TJ) in ps 17.8333 ps	Periodic Jitter (PJ rms) 4.2 mUI	Periodic Jitter (PJ p-p) 13.4 mUI
Deterministic Jitter (DJ) 28.1 mUI	Random Jitter (RJ) 5.6 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 16.6 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

**Trial 1**



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✓ Lane 3 - D10.2 Total Jitter Test with No Cable Model (TP3\_EQ)

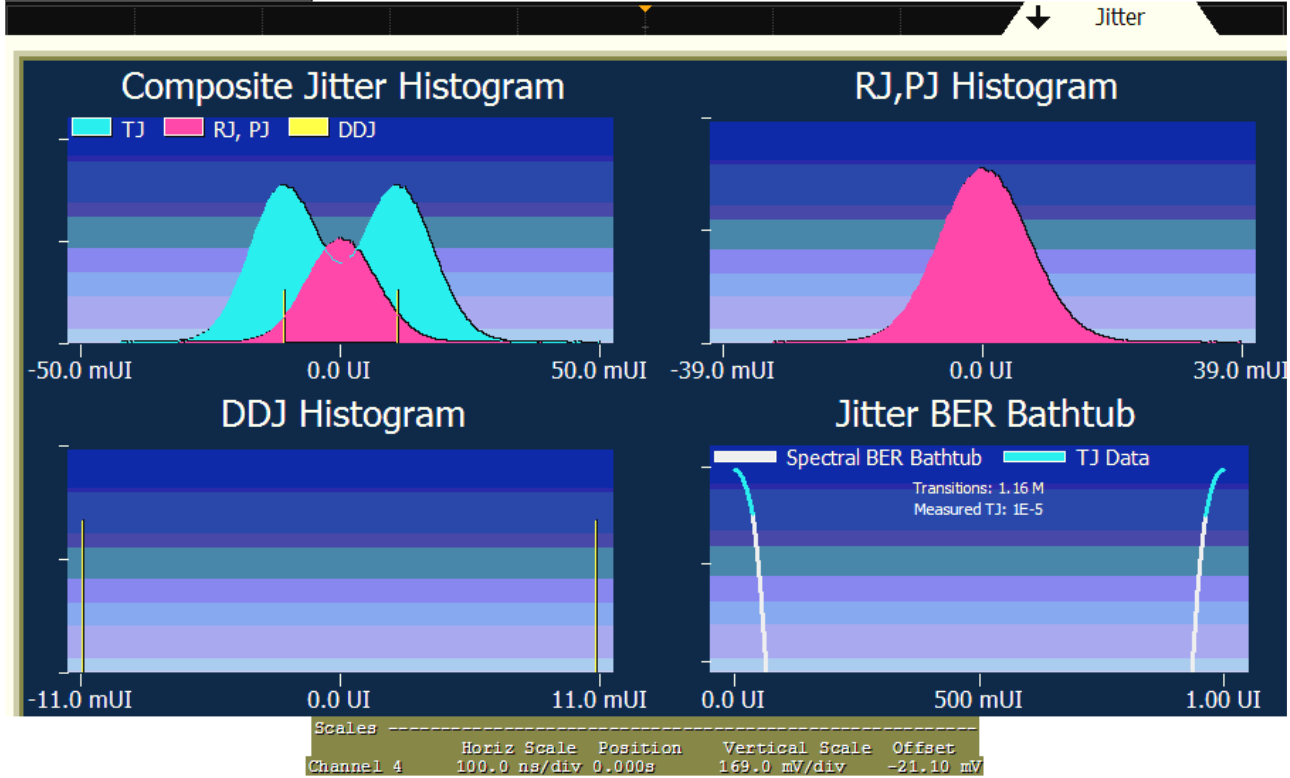
Test Summary: Pass Test Description: To evaluate the Total Jitter with No Cable Model (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 400.000 mUI D10.2 Total Jitter (TP3\_EQ No Cable) 100.400 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.000000000 M	Total Jitter (TJ) 100.4 mUI	Total Jitter (TJ) in ps 18.5926 ps	Periodic Jitter (PJ rms) 3.8 mUI	Periodic Jitter (PJ p-p) 13.1 mUI
Deterministic Jitter (DJ) 33.0 mUI	Random Jitter (RJ) 5.5 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 21.9 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 0 - D10.2 Deterministic Jitter with No Cable (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

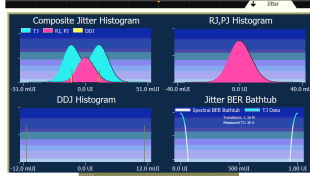
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 250.000 mUI D10.2 Deterministic Jitter (TP3\_EQ No Cable) 33.700 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 104.6 mUI	Total Jitter (TJ) in ps 19.3704 ps	Periodic Jitter (PJ rms) 4.1 mUI	Periodic Jitter (PJ p-p) 12.9 mUI
Deterministic Jitter (DJ) 33.7 mUI	Random Jitter (RJ) 5.8 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 22.8 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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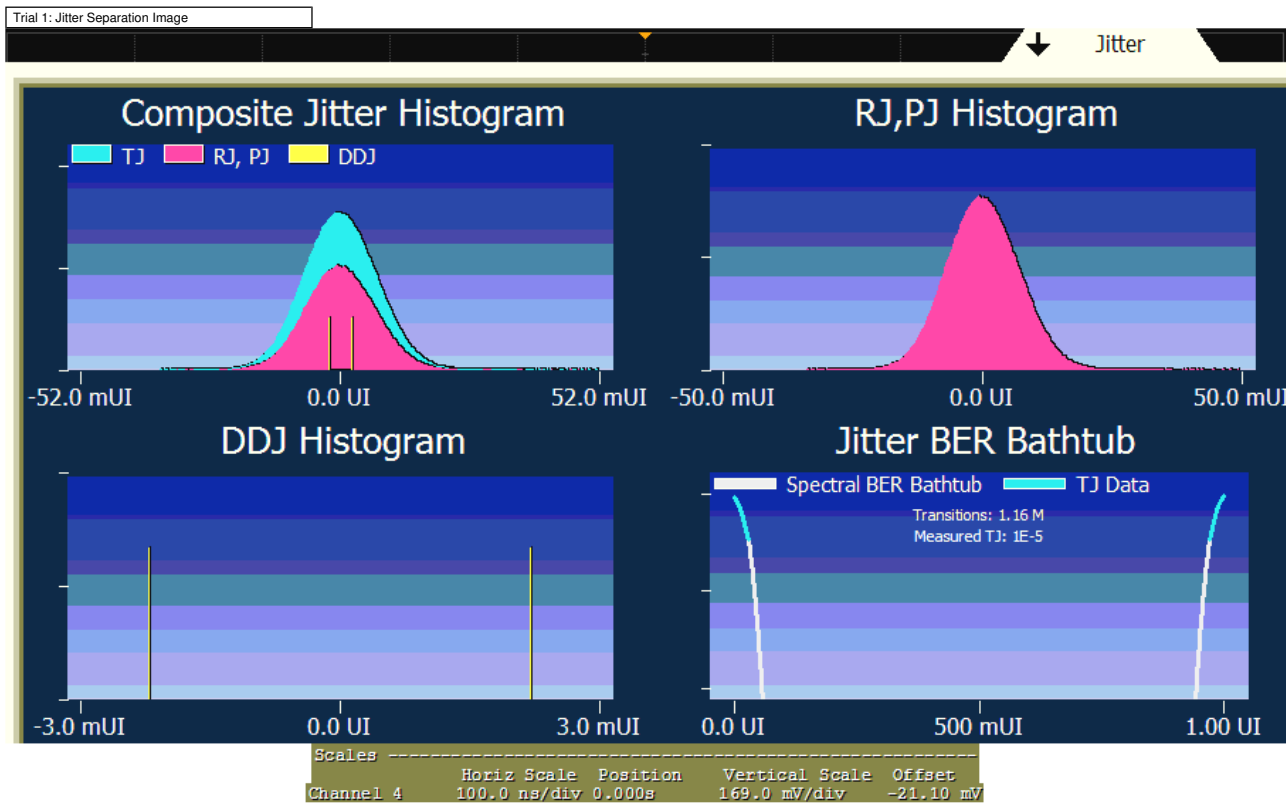
✓ Lane 1 - D10.2 Deterministic Jitter with No Cable (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 250.000 mUI D10.2 Deterministic Jitter (TP3\_EQ No Cable) 17.100 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 85.2 mUI	Total Jitter (TJ) in ps 15.7777 ps	Periodic Jitter (PJ rms) 3.9 mUI	Periodic Jitter (PJ p-p) 15.1 mUI
Deterministic Jitter (DJ) 17.1 mUI	Random Jitter (RJ) 5.6 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 4.4 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1



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✓ Lane 2 - D10.2 Deterministic Jitter with No Cable (TP3\_EQ) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

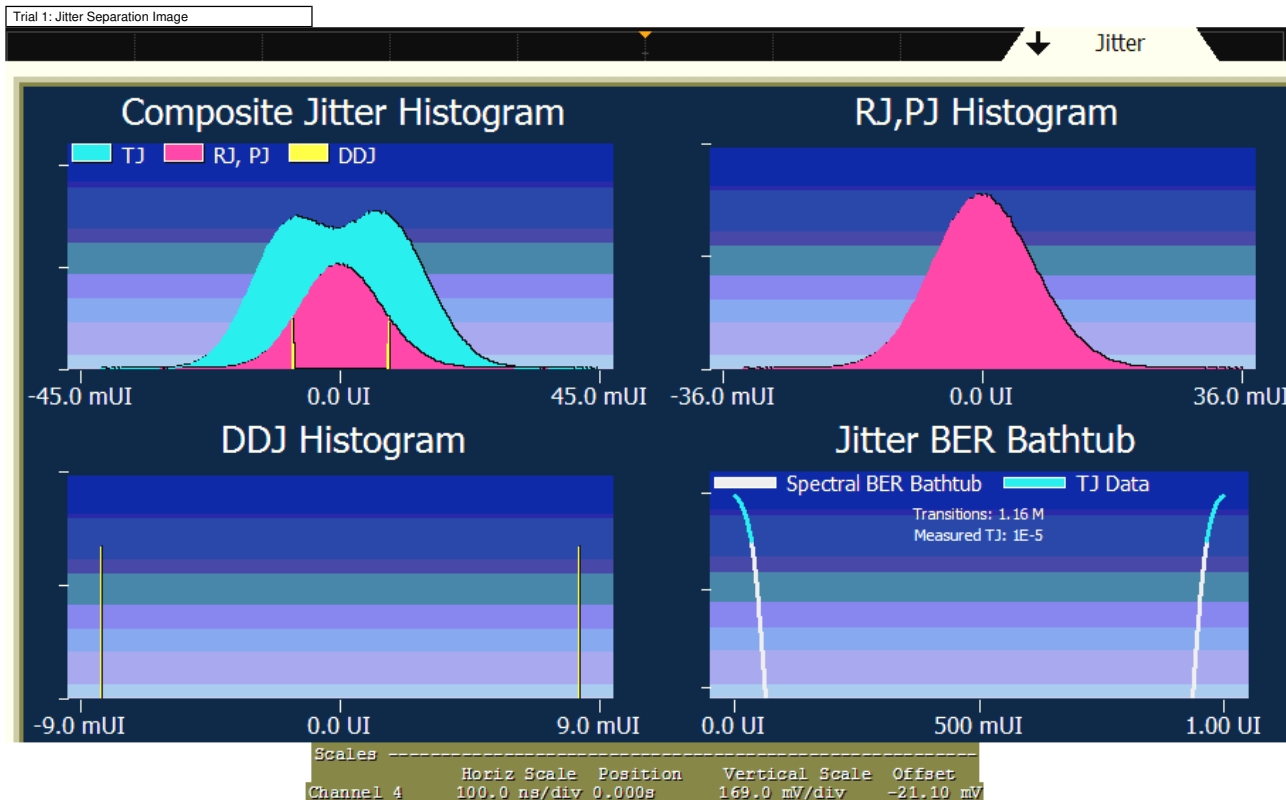
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 250.000 mUI Lane 2 D10.2 Deterministic Jitter (TP3\_EQ No Cable) 28.100 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 96.3 mUI	Total Jitter (TJ) in ps 17.8333 ps	Periodic Jitter (PJ rms) 4.2 mUI	Periodic Jitter (PJ p-p) 13.4 mUI
Deterministic Jitter (DJ) 28.1 mUI	Random Jitter (RJ) 5.6 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 16.6 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1



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✓ Lane 3 - D10.2 Deterministic Jitter with No Cable (TP3\_EQ)

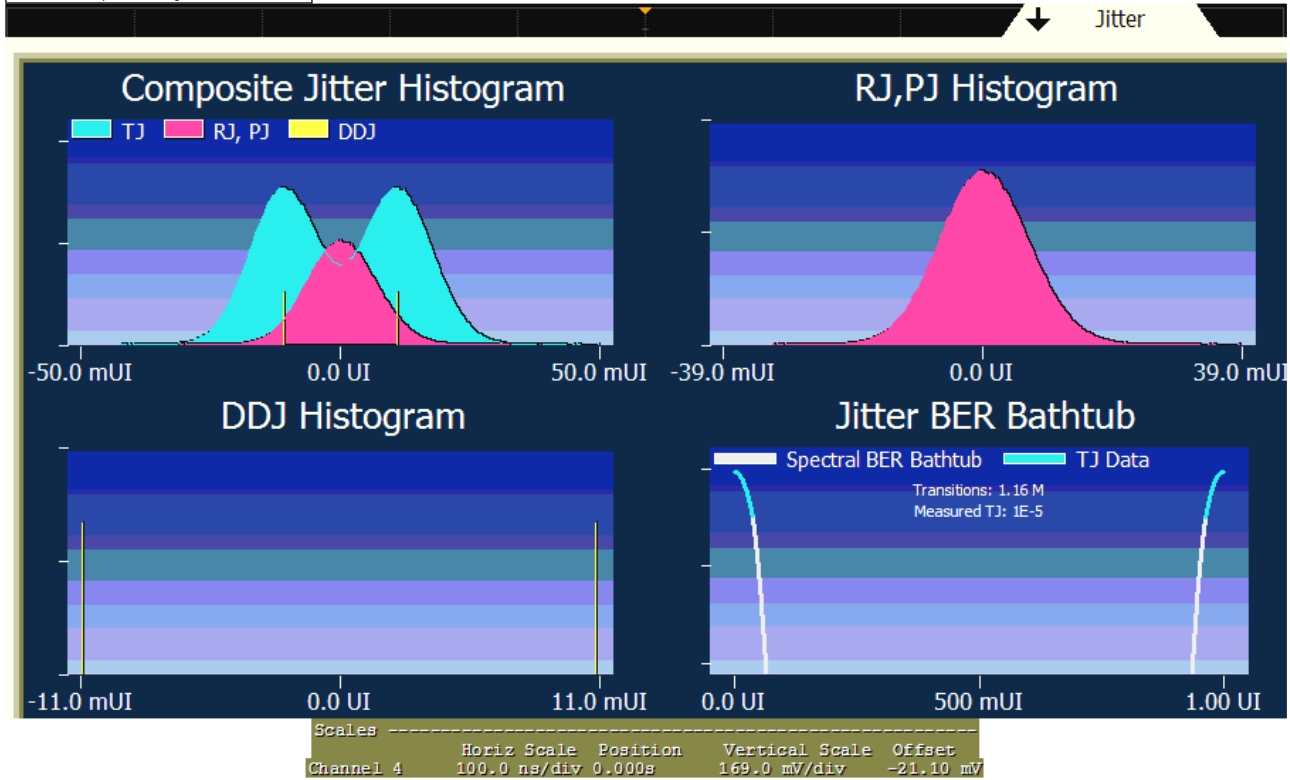
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 250.000 mUI D10.2 Deterministic Jitter (TP3\_EQ No Cable) 33.000 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 100.4 mUI	Total Jitter (TJ) in ps 18.5926 ps	Periodic Jitter (PJ rms) 3.8 mUI	Periodic Jitter (PJ p-p) 13.1 mUI
Deterministic Jitter (DJ) 33.0 mUI	Random Jitter (RJ) 5.5 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 21.9 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 0

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 0 - D10.2 Random Jitter with No Cable (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

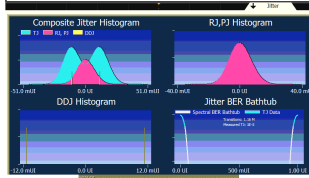
Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 230.000 mUI D10.2 Random Jitter (TP3\_EQ No Cable) 5.800 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 104.6 mUI	Total Jitter (TJ) in ps 19.3704 ps	Periodic Jitter (PJ rms) 4.1 mUI	Periodic Jitter (PJ p-p) 12.9 mUI
Deterministic Jitter (DJ) 33.7 mUI	Random Jitter (RJ) 5.8 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 22.8 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 0

Trial 1

Trial 1: Jitter Separation Image



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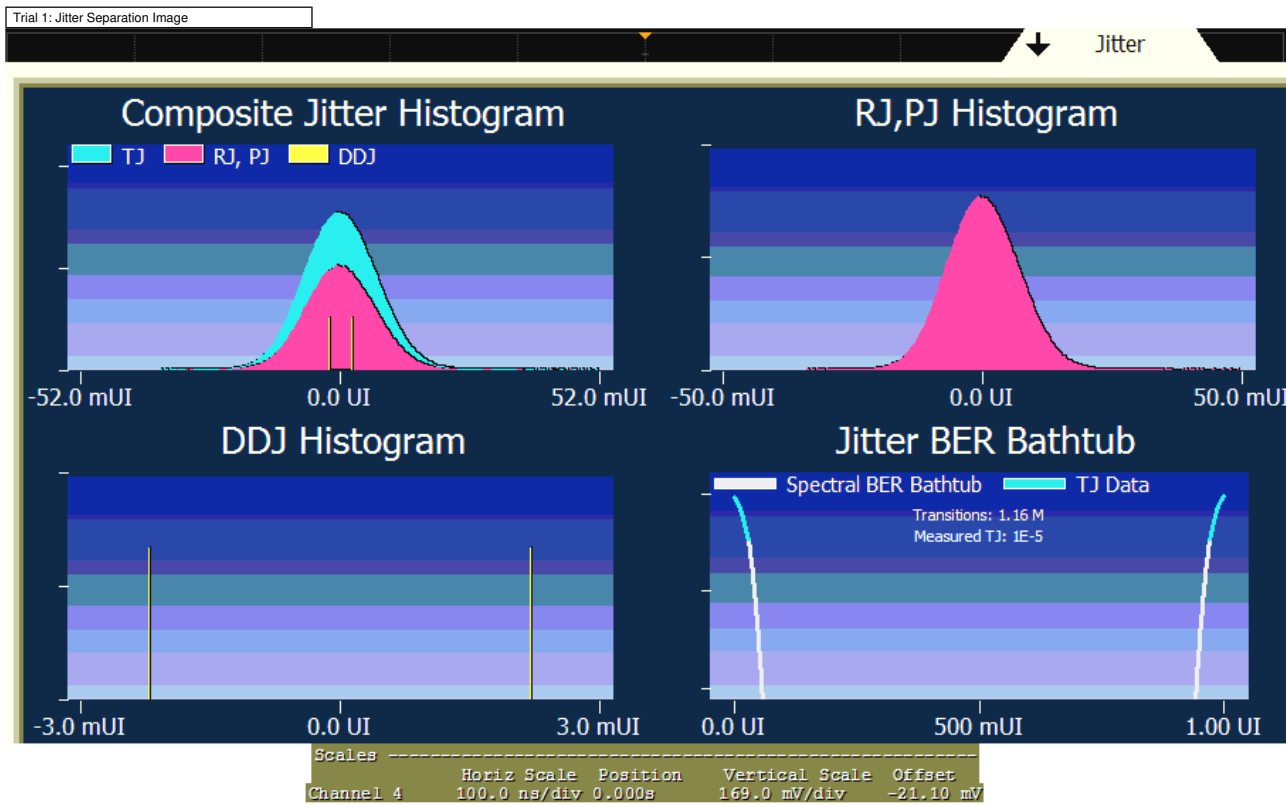
✓ Lane 1 - D10.2 Random Jitter with No Cable (TP3\_EQ) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 230.000 mUI D10.2 Random Jitter (TP3\_EQ No Cable) 5.800 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 85.2 mUI	Total Jitter (TJ) in ps 15.7777 ps	Periodic Jitter (PJ rms) 3.9 mUI	Periodic Jitter (PJ p-p) 15.1 mUI
Deterministic Jitter (DJ) 17.1 mUI	Random Jitter (RJ) 5.6 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 4.4 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			Level Swing 0

Trial 1



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✓ Lane 2 - D10.2 Random Jitter with No Cable (TP3\_EQ) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

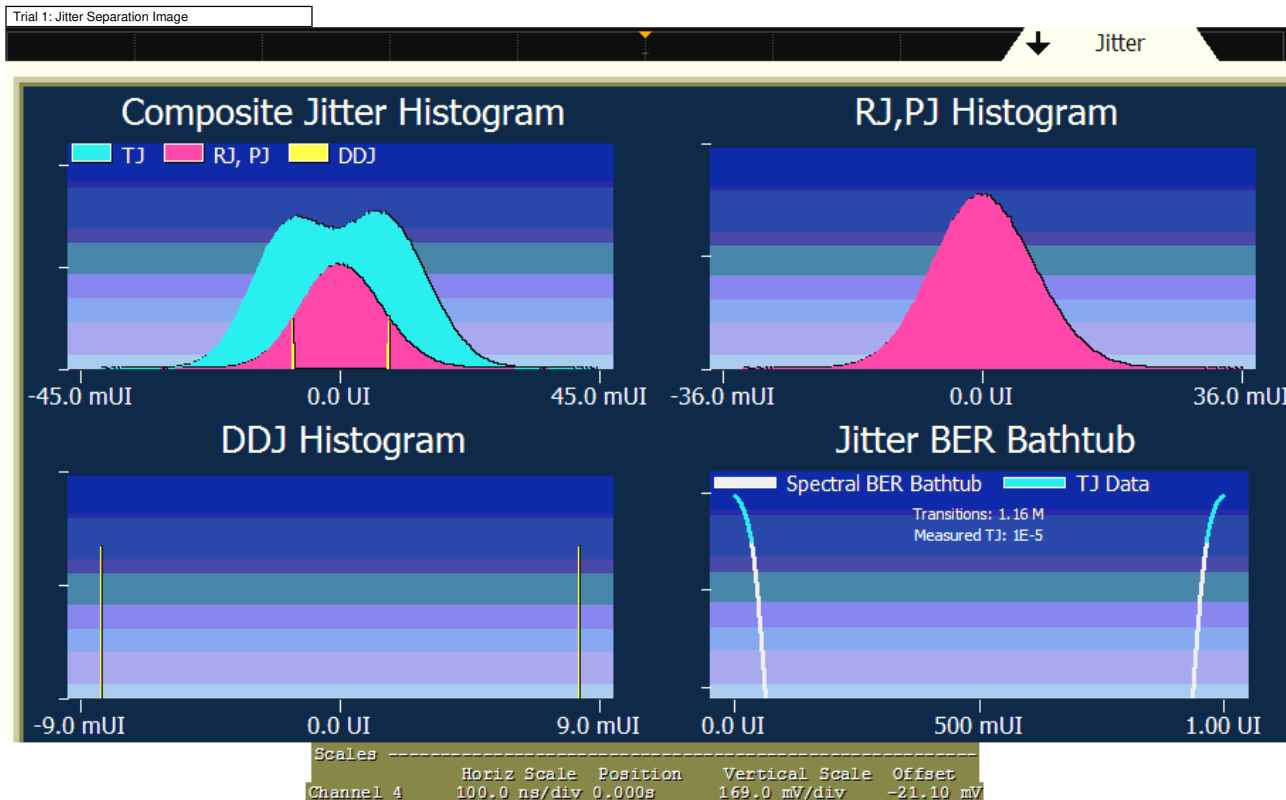
Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 230.000 mUI Lane 2 D10.2 Random Jitter (TP3\_EQ No Cable) 5.600 mUI

**Result Details**

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 96.3 mUI	Total Jitter (TJ) in ps 17.8333 ps	Periodic Jitter (PJ rms) 4.2 mUI	Periodic Jitter (PJ p-p) 13.4 mUI
Deterministic Jitter (DJ) 28.1 mUI	Random Jitter (RJ) 5.6 mUI	ISI Jitter (ISI) 0.0000 UI	Data Dependent Jitter (DDJ) 16.6 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

**Trial 1**



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✓ Lane 3 - D10.2 Random Jitter with No Cable (TP3\_EQ)

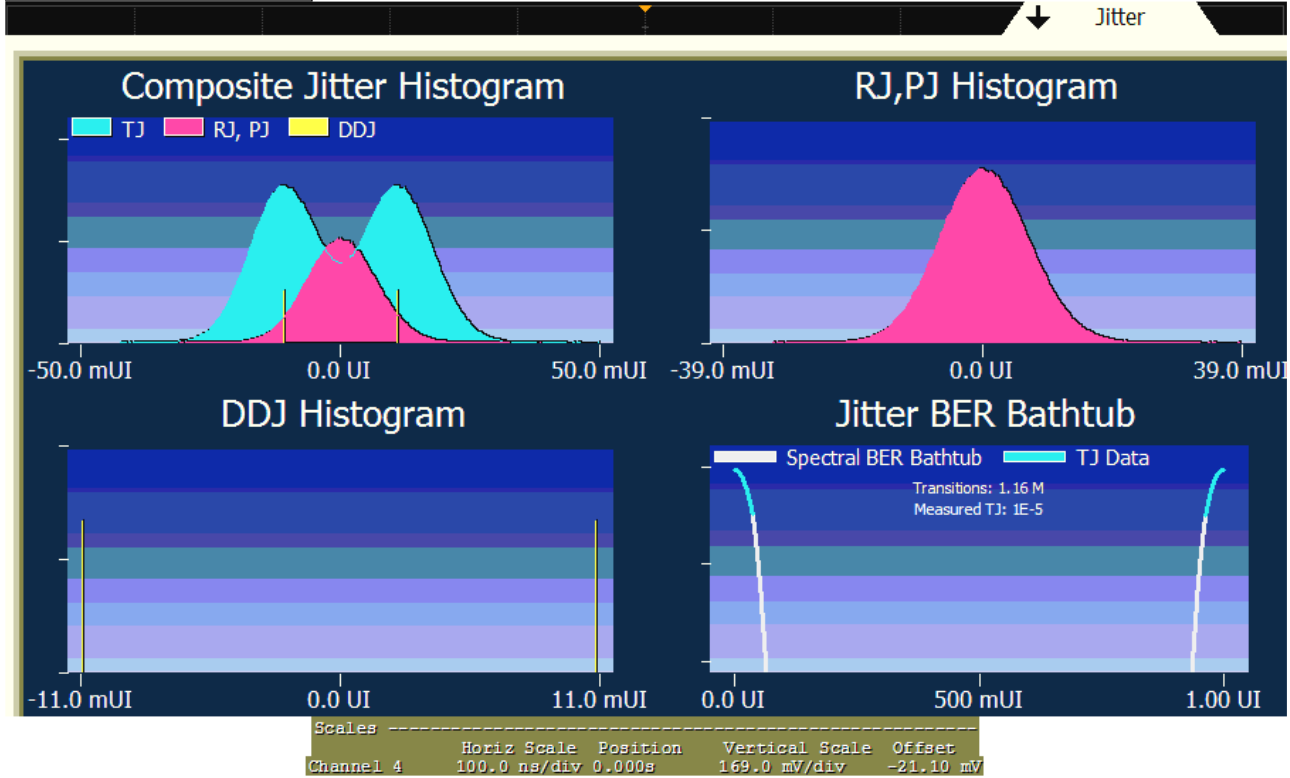
Test Summary: Pass Test Description: To evaluate the Random Jitter (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 230.000 mUI D10.2 Random Jitter (TP3\_EQ No Cable) 5.500 mUI

Result Details

Jitter Separation Image (See image) Edges 1.0000000000 M Total Jitter (TJ) 100.4 mUI Total Jitter (TJ) in ps 18.5926 ps Periodic Jitter (PJ rms) 3.8 mUI Periodic Jitter (PJ p-p) 13.1 mUI  
 Deterministic Jitter (DJ) 33.0 mUI Random Jitter (RJ) 5.5 mUI ISI Jitter (ISI) 0.0000 UI Data Dependent Jitter (DDJ) 21.9 mUI Bit Error Rate (BER) E9 Test Mode Compliance  
 Test Layer Physical Layer Tests Test Condition Compliance Conditions Only DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 0  
 PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 0 - HBR2CPAT Eye Diagram Test with No Cable (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.1

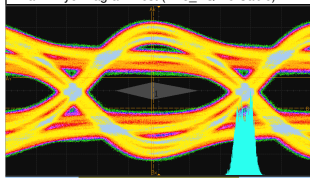
Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ No Cable) 0.000

Result Details

Number of UI 1000000 Statistical Mask Height(VHigh) 65.265 mV Statistical Mask Height(VLow) -70.093 mV Statistical Eye Height 234.641 mV Statistical Mask Width 479.414 mUI  
 Measured RNoise VHigh(Sigma) 10.659 mV Measured RNoise VLow(Sigma) 14.538 mV Measured Eye Height 266.000 mV Measured Eye Width 142.630 ps Max Eye Height Position 470 mUI  
 Measured Rj 7.800 mUI Mask Passing Center Position 0.000 V Vertical Scale 163.335 mV Test Mode Compliance Test Layer Physical Layer Tests Test Condition Compliance Conditions Only  
 DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 0 PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1

Trial 1: Eye Diagram Test (TP3\_EQ No Cable)



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✓ Lane 1 - HBR2CPAT Eye Diagram Test with No Cable (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.1

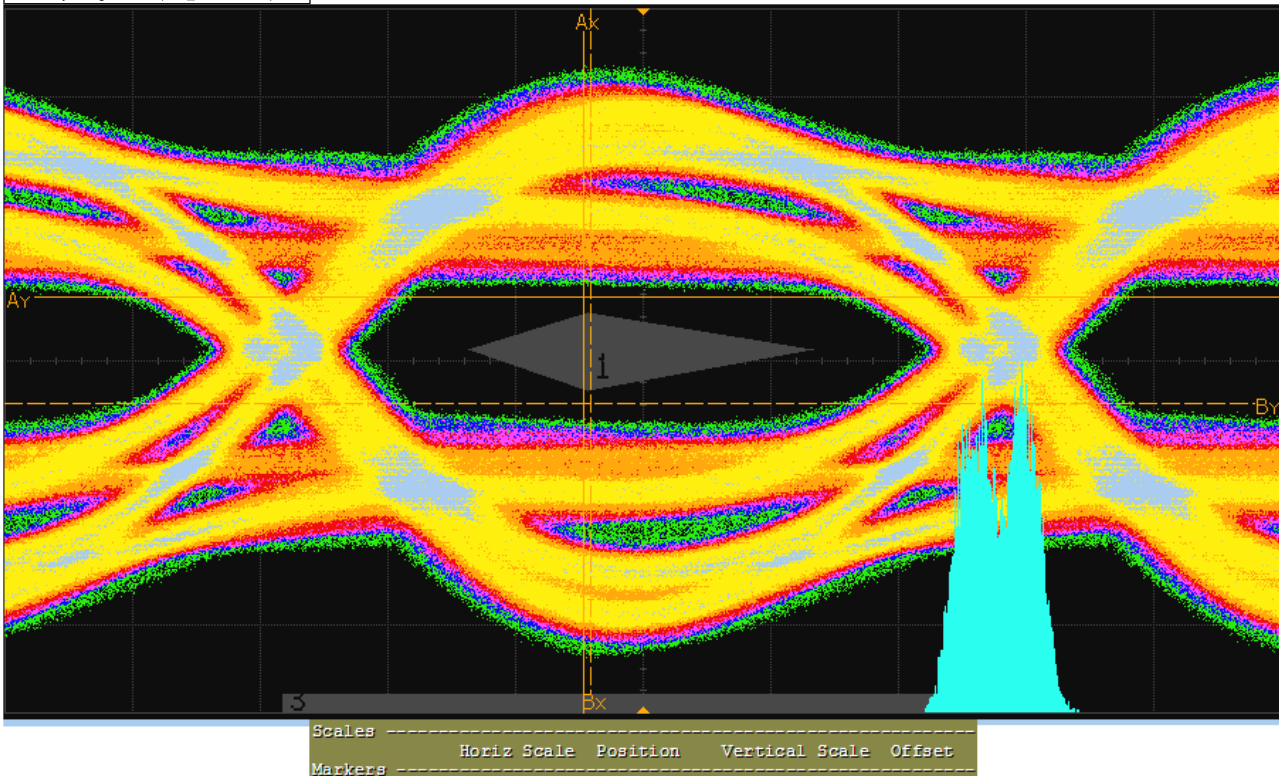
Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ No Cable) 0.000

Result Details

Number of UI 1000000 Statistical Mask Height(VHigh) 74.761 mV Statistical Mask Height(VLow) -82.144 mV Statistical Eye Height 214.295 mV Statistical Mask Width 479.863 mUI  
 Measured RNoise VHigh(Sigma) 18.289 mV Measured RNoise VLow(Sigma) 24.222 mV Measured Eye Height 267.200 mV Measured Eye Width 145.940 ps Max Eye Height Position 420 mUI  
 Measured Rj 7.900 mUI Mask Passing Center Position 0.000 V Vertical Scale 176.235 mV Test Mode Compliance Test Layer Physical Layer Tests Test Condition Compliance Conditions Only  
 DUT Type Source Test Type Differential Tests Connection Type Differential Probe BitRate 5.4 Gbps Level Swing 0 PreEmphasis Pre-emphasis 0 SSC SSC Disabled PostCursor2 Level 0

Trial 1

Trial 1: Eye Diagram Test (TP3\_EQ No Cable)



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✓ Lane 2 - HBR2CPAT Eye Diagram Test with No Cable (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

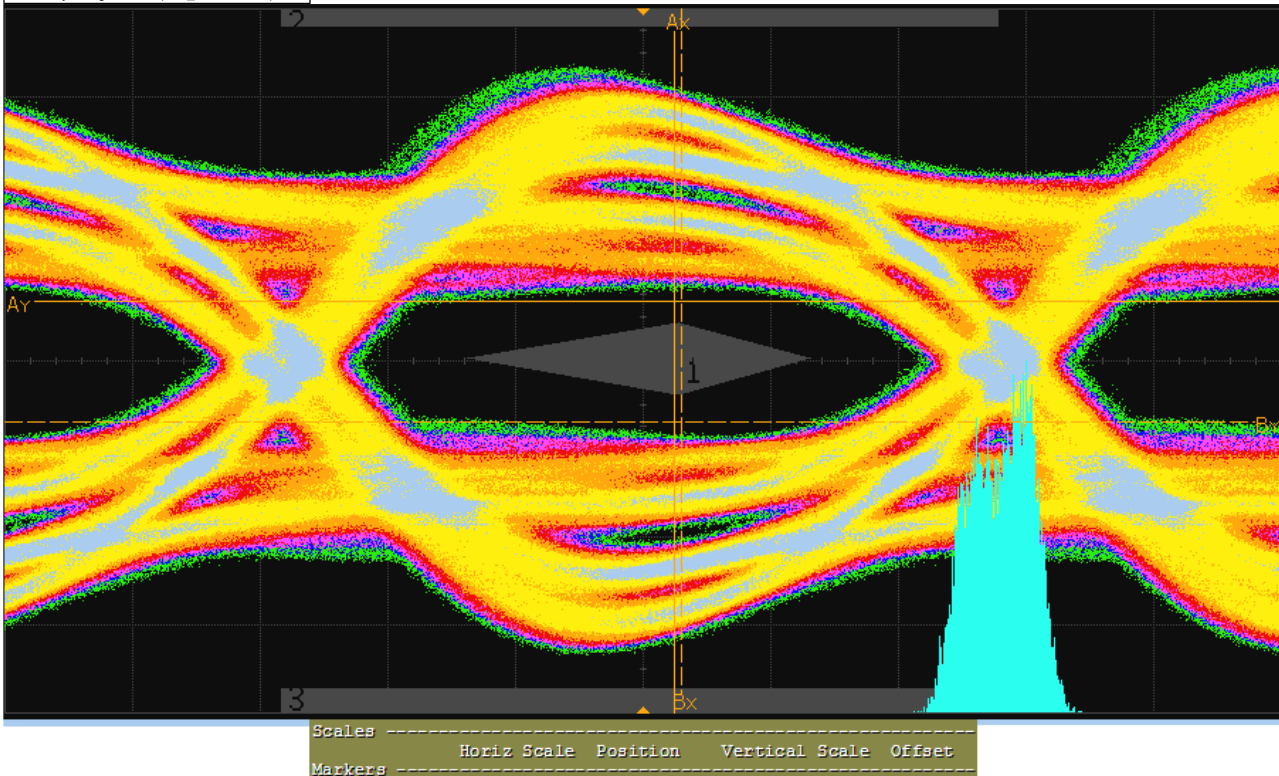
Pass Limits: [-500 m to 500 m] Eye Diagram Test (TP3\_EQ No Cable) 0.000

Result Details

Number of UI	1000000	Statistical Mask Height(VHigh)	73.074 mV	Statistical Mask Height(VLow)	-79.166 mV	Statistical Eye Height	250.060 mV	Statistical Mask Width	479.663 mUI
Measured RNoise VHigh(Sigma)	16.934 mV	Measured RNoise VLow(Sigma)	21.829 mV	Measured Eye Height	298.300 mV	Measured Eye Width	142.260 ps	Max Eye Height Position	550 mUI
Measured Rj	7.900 mUI	Mask Passing Center Position	0.000 V	Vertical Scale	183.135 mV	Test Mode	Compliance	Test Layer	Physical Layer Tests
DUT Type	Source	Test Type	Differential Tests	Connection Type	Differential Probe	BitRate	5.4 Gbps	Level	Swing 0
		PreEmphasis	Pre-emphasis 0	SSC	SSC Disabled	PostCursor2	Level 0		

Trial 1

Trial 1: Eye Diagram Test (TP3\_EQ No Cable)



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✓ Lane 3 - HBR2CPAT Eye Diagram Test with No Cable (TP3\_EQ)



Reference: DisplayPort CTS Sec. 3.1

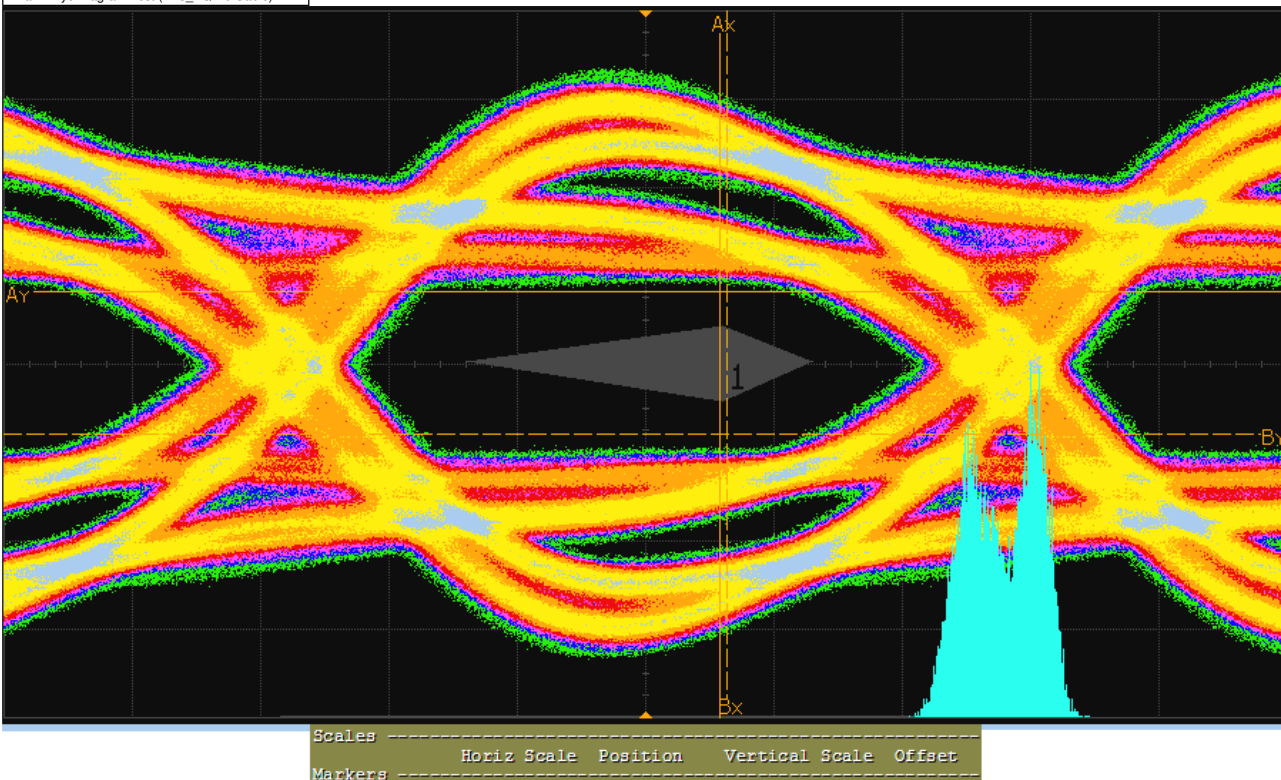
Test Summary: **Pass** Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
**Pass Limits:** [-500 m to 500 m] **Eye Diagram Test (TP3\_EQ No Cable)** 0.000

**Result Details**

**Number of UI** 1000000 **Statistical Mask Height(VHigh)** 68.710 mV **Statistical Mask Height(VLow)** -77.425 mV **Statistical Eye Height** 275.925 mV **Statistical Mask Width** 479.663 mUI  
**Measured RNoise VHigh(Sigma)** 13.427 mV **Measured RNoise VLow(Sigma)** 20.430 mV **Measured Eye Height** 318.060 mV **Measured Eye Width** 139.330 ps **Max Eye Height Position** 610 mUI  
**Measured RJ** 7.900 mUI **Mask Passing Center Position** 0.000 V **Vertical Scale** 171.478 mV **Test Mode** Compliance **Test Layer** Physical Layer Tests **Test Condition** Compliance Conditions Only  
**DUT Type** Source **Test Type** Differential Tests **Connection Type** Differential Probe **BitRate** 5.4 Gbps **Level** Swing 0 **PreEmphasis** Pre-emphasis 0 **SSC** SSC Disabled **PostCursor2** Level 0

**Trial 1**

Trial 1: Eye Diagram Test (TP3\_EQ No Cable)



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**✓ Lane 0 - HBR2CPAT Total Jitter Test with No Cable (TP3\_EQ)** Reference: DisplayPort CTS Sec. 3.12: Table 3.19 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the Total Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

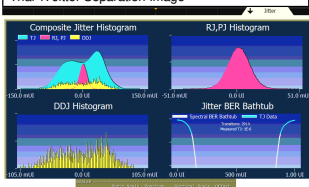
**Pass Limits:** <= 580.000 mUI **HBR2CPAT Total Jitter (TP3\_EQ No Cable)** 275.300 mUI

**Result Details**

**Jitter Separation Image** (See image) **Edges** 1.00000000 M **Total Jitter (TJ)** 275.3 mUI **Total Jitter (TJ) in ps** 50.9823 ps **Periodic Jitter (PJ rms)** 2.5 mUI **Periodic Jitter (PJ p-p)** 9.4 mUI  
**Deterministic Jitter (DJ)** 172.5 mUI **Random Jitter (RJ)** 8.5 mUI **ISI Jitter (ISI)** 180.7 mUI **Data Dependent Jitter (DDJ)** 191.5 mUI **Bit Error Rate (BER)** E9 **Test Mode** Compliance  
**Test Layer** Physical Layer Tests **Test Condition** Compliance Conditions Only **DUT Type** Source **Test Type** Differential Tests **Connection Type** Differential Probe **BitRate** 5.4 Gbps **Level** Swing 0  
**PreEmphasis** Pre-emphasis 0 **SSC** SSC Disabled **PostCursor2** Level 0

**Trial 1**

Trial 1: Jitter Separation Image



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**✓ Lane 1 - HBR2CPAT Total Jitter Test with No Cable (TP3\_EQ)** Reference: DisplayPort CTS Sec. 3.12: Table 3.19 VESA DisplayPort Standard specification

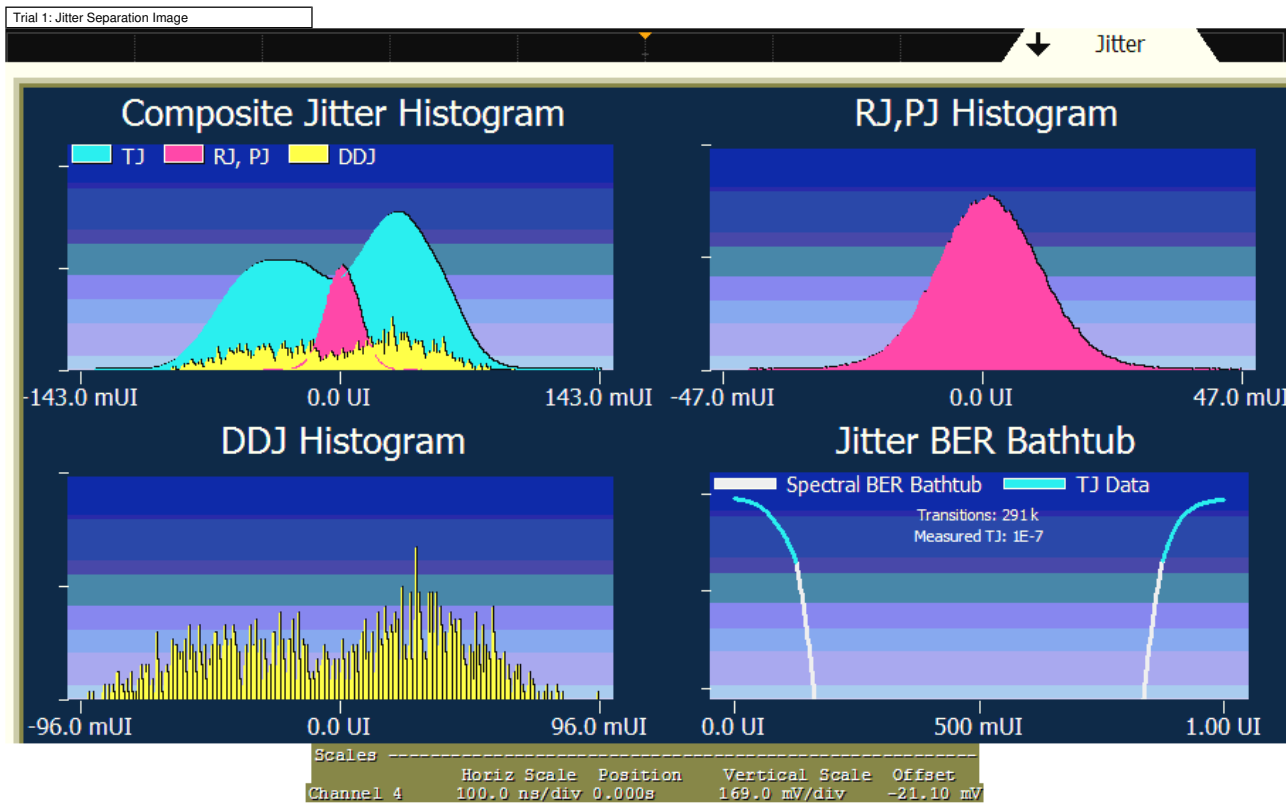
Test Summary: **Pass** Test Description: To evaluate the Total Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

**Pass Limits:** <= 580.000 mUI **HBR2CPAT Total Jitter (TP3\_EQ No Cable)** 277.600 mUI

**Result Details**

**Jitter Separation Image** (See image) **Edges** 1.00000000 M **Total Jitter (TJ)** 277.6 mUI **Total Jitter (TJ) in ps** 51.4079 ps **Periodic Jitter (PJ rms)** 1.7 mUI **Periodic Jitter (PJ p-p)** 7.6 mUI  
**Deterministic Jitter (DJ)** 166.6 mUI **Random Jitter (RJ)** 9.2 mUI **ISI Jitter (ISI)** 183.7 mUI **Data Dependent Jitter (DDJ)** 189.5 mUI **Bit Error Rate (BER)** E9 **Test Mode** Compliance  
**Test Layer** Physical Layer Tests **Test Condition** Compliance Conditions Only **DUT Type** Source **Test Type** Differential Tests **Connection Type** Differential Probe **BitRate** 5.4 Gbps **Level** Swing 0  
**PreEmphasis** Pre-emphasis 0 **SSC** SSC Disabled **PostCursor2** Level 0

**Trial 1**



✓ Lane 2 - HBR2CPAT Total Jitter Test with No Cable (TP3\_EQ) Reference: DisplayPort CTS Sec. 3.12; Table 3.19 VESA DisplayPort Standard specification

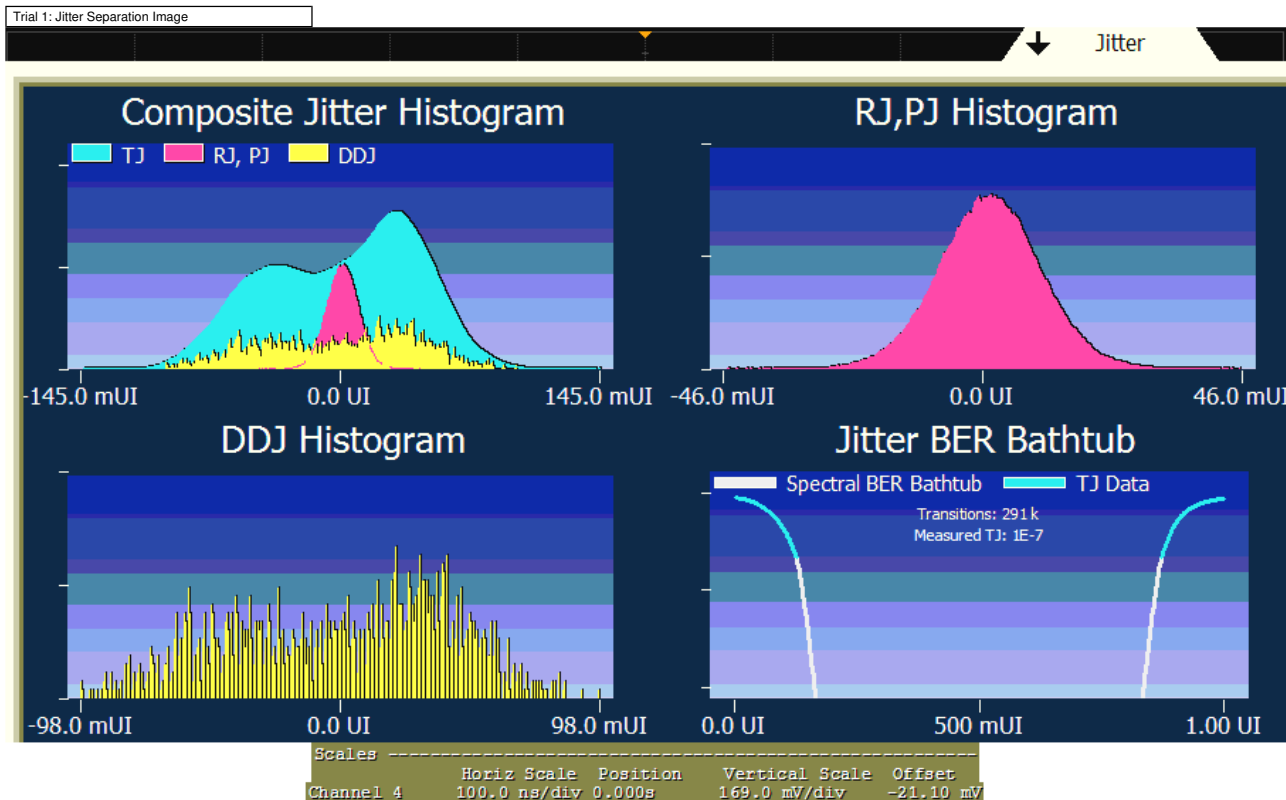
Test Summary: Pass Test Description: To evaluate the Total Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 580.000 mUI Lane 2 HBR2CPAT Total Jitter (TP3\_EQ No Cable) 282.200 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.00000000 M	Total Jitter (TJ) 282.2 mUI	Total Jitter (TJ) in ps 52.2598 ps	Periodic Jitter (PJ rms) 2.5 mUI	Periodic Jitter (PJ p-p) 11.5 mUI
Deterministic Jitter (DJ) 177.4 mUI	Random Jitter (RJ) 8.7 mUI	ISI Jitter (ISI) 196.3 mUI	Data Dependent Jitter (DDJ) 197.0 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1





✓ Lane 3 - HBR2CPAT Total Jitter Test with No Cable (TP3\_EQ)

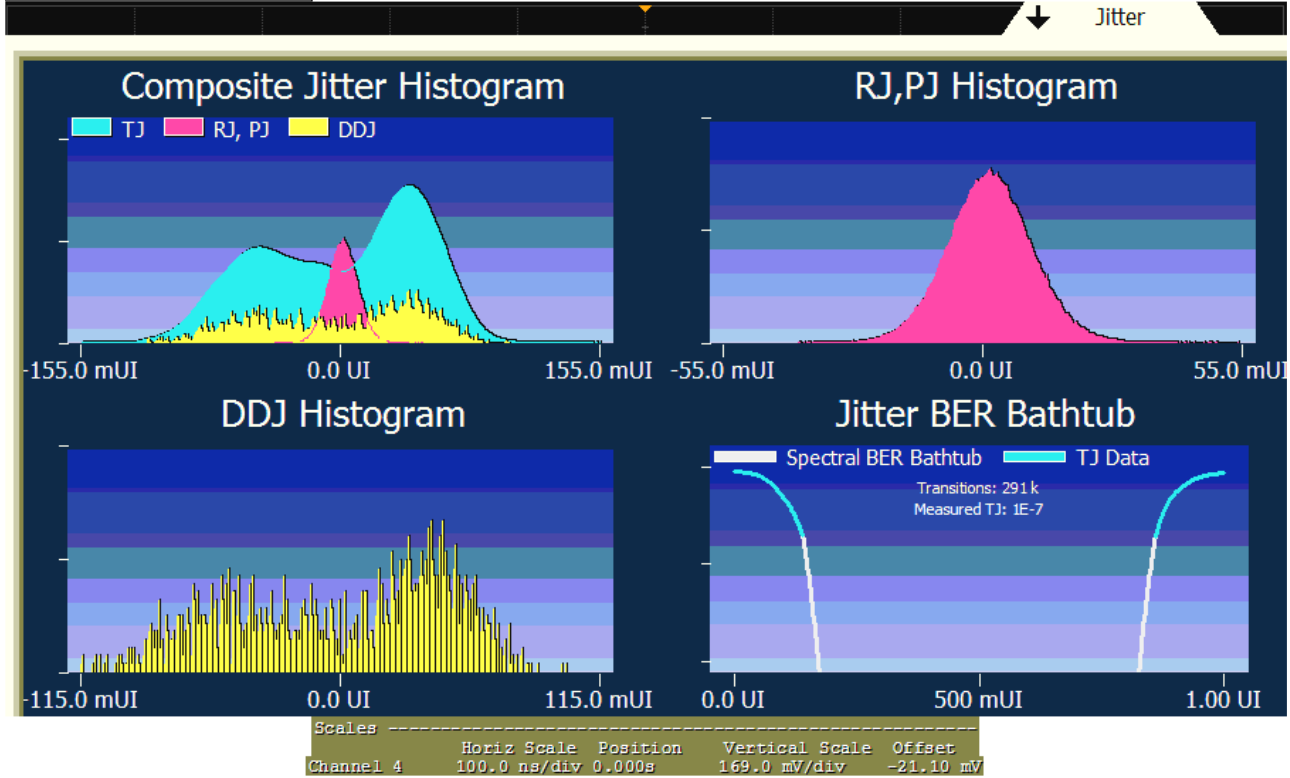
Test Summary: Pass Test Description: To evaluate the Total Jitter with No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 580.000 mUI HBR2CPAT Total Jitter (TP3\_EQ No Cable) 301.300 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.000000000 M	Total Jitter (TJ) 301.3 mUI	Total Jitter (TJ) in ps 55.7972 ps	Periodic Jitter (PJ rms) 3.5 mUI	Periodic Jitter (PJ p-p) 12.7 mUI
Deterministic Jitter (DJ) 202.6 mUI	Random Jitter (RJ) 8.2 mUI	ISI Jitter (ISI) 207.1 mUI	Data Dependent Jitter (DDJ) 216.5 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 0 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3\_EQ)

Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

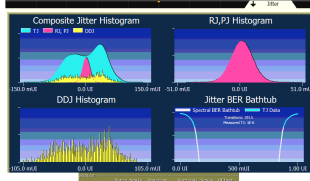
Test Summary: Pass Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 490.000 mUI HBR2CPAT Deterministic Jitter (TP3\_EQ No Cable) 172.500 mUI

Result Details

Jitter Separation Image (See image)	Edges 1.000000000 M	Total Jitter (TJ) 275.3 mUI	Total Jitter (TJ) in ps 50.9823 ps	Periodic Jitter (PJ rms) 2.5 mUI	Periodic Jitter (PJ p-p) 9.4 mUI
Deterministic Jitter (DJ) 172.5 mUI	Random Jitter (RJ) 8.5 mUI	ISI Jitter (ISI) 180.7 mUI	Data Dependent Jitter (DDJ) 191.5 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image



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✓ Lane 1 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3\_EQ)

Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 490.000 mUI HBR2CPAT Deterministic Jitter (TP3\_EQ No Cable) 166.600 mUI

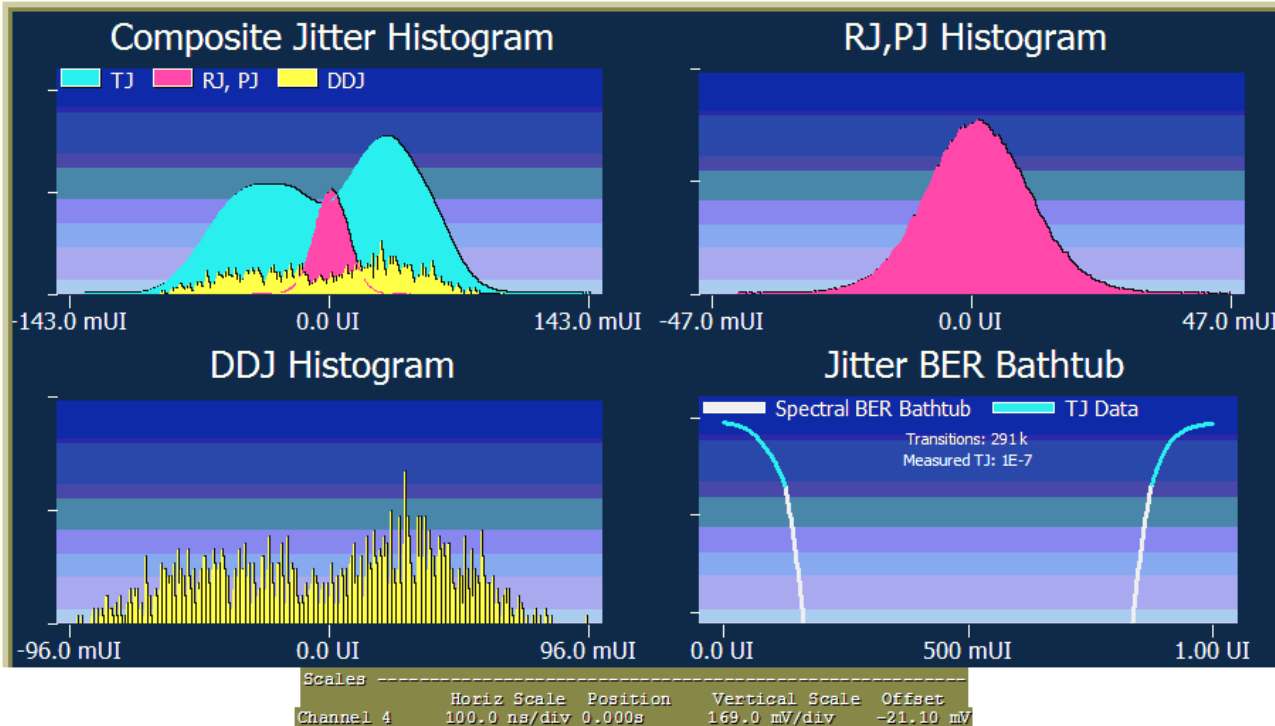
Result Details

Jitter Separation Image (See image)	Edges 1.000000000 M	Total Jitter (TJ) 277.6 mUI	Total Jitter (TJ) in ps 51.4079 ps	Periodic Jitter (PJ rms) 1.7 mUI	Periodic Jitter (PJ p-p) 7.6 mUI
Deterministic Jitter (DJ) 166.6 mUI	Random Jitter (RJ) 9.2 mUI	ISI Jitter (ISI) 183.7 mUI	Data Dependent Jitter (DDJ) 189.5 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image

Jitter



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✓ Lane 2 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3\_EQ)

Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 490.000 mUI Lane 2 HBR2CPAT Deterministic Jitter (TP3\_EQ No Cable) 177.400 mUI

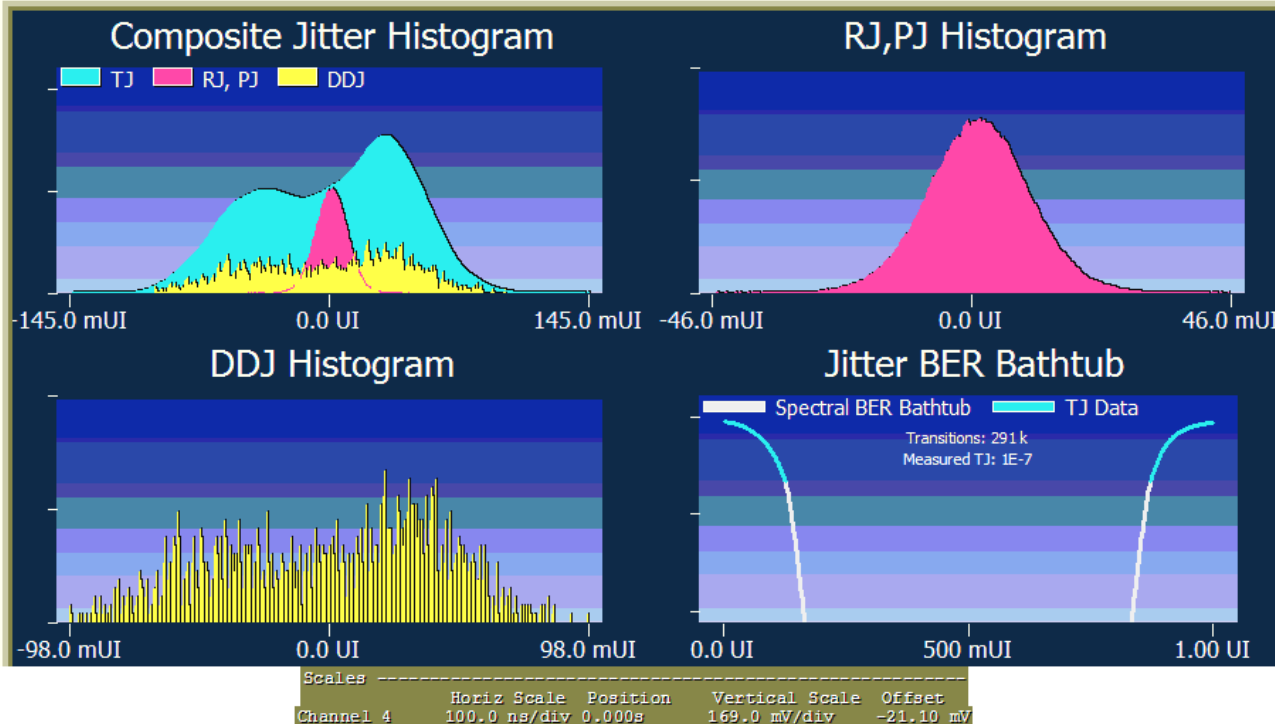
Result Details

Jitter Separation Image (See image)	Edges 1.0000000000 M	Total Jitter (TJ) 282.2 mUI	Total Jitter (TJ) in ps 52.2598 ps	Periodic Jitter (PJ rms) 2.5 mUI	Periodic Jitter (PJ p-p) 11.5 mUI
Deterministic Jitter (DJ) 177.4 mUI	Random Jitter (RJ) 8.7 mUI	ISI Jitter (ISI) 196.3 mUI	Data Dependent Jitter (DDJ) 197.0 mUI	Bit Error Rate (BER) E9	Test Mode Compliance
Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps Level Swing 0
PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0			

Trial 1

Trial 1: Jitter Separation Image

Jitter



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**✓ Lane 3 - HBR2CPAT Deterministic Jitter Test with No Cable (TP3\_EQ)**

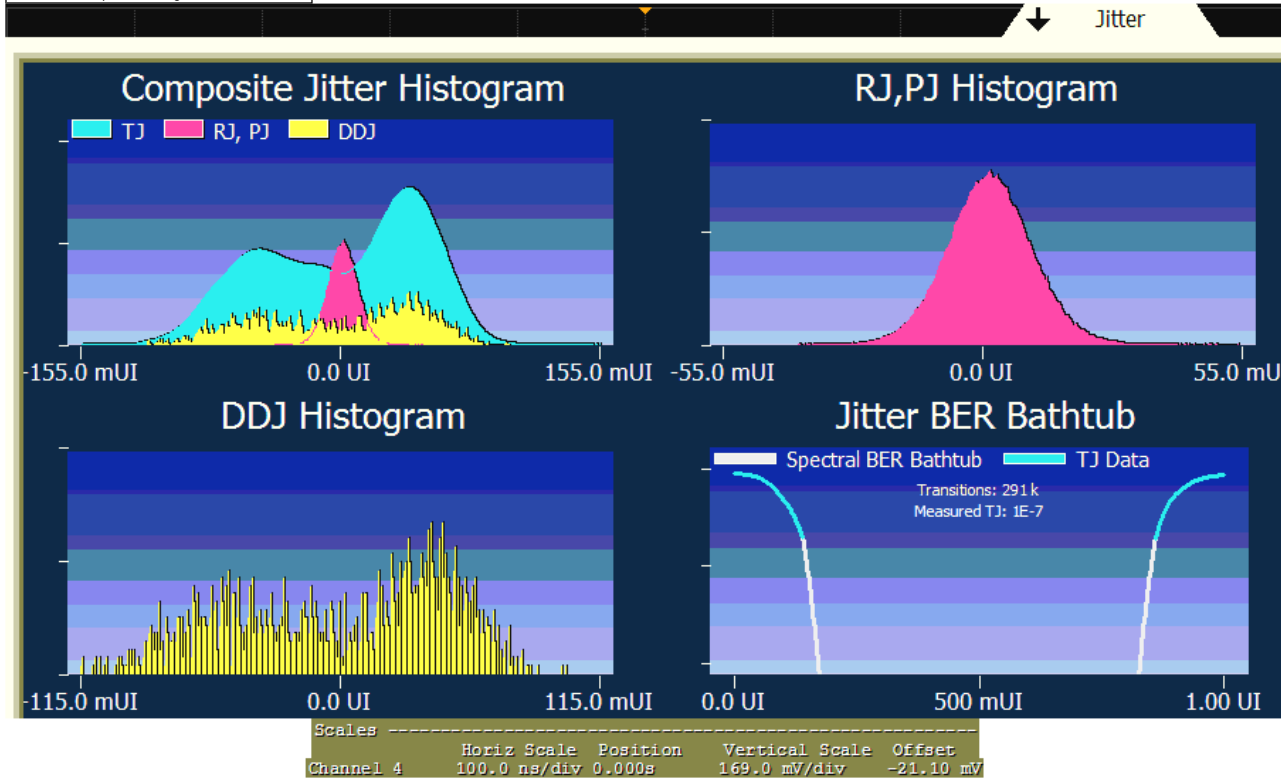
Test Summary: **Pass** Test Description: To evaluate the Deterministic Jitter No Cable (TP3\_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.  
 Pass Limits: <= 490.000 mUI | **HBR2CPAT Deterministic Jitter (TP3\_EQ No Cable)** 202.600 mUI

**Result Details**

Jitter Separation Image (See image) | Edges 1.0000000000 M | Total Jitter (TJ) 301.3 mUI | Total Jitter (TJ) in ps 55.7972 ps | Periodic Jitter (PJ rms) 3.5 mUI | Periodic Jitter (PJ p-p) 12.7 mUI  
 Deterministic Jitter (DJ) 202.6 mUI | Random Jitter (RJ) 8.2 mUI | ISI Jitter (ISI) 207.1 mUI | Data Dependent Jitter (DDJ) 216.5 mUI | Bit Error Rate (BER) E9 | Test Mode Compliance  
 Test Layer Physical Layer Tests | Test Condition Compliance Conditions Only | DUT Type Source | Test Type Differential Tests | Connection Type Differential Probe | BitRate 5.4 Gbps | Level Swing 0  
 PreEmphasis Pre-emphasis 0 | SSC SSC Disabled | PostCursor2 Level 0

**Trial 1**

Trial 1: Jitter Separation Image



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**✗ Lane 0 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)**

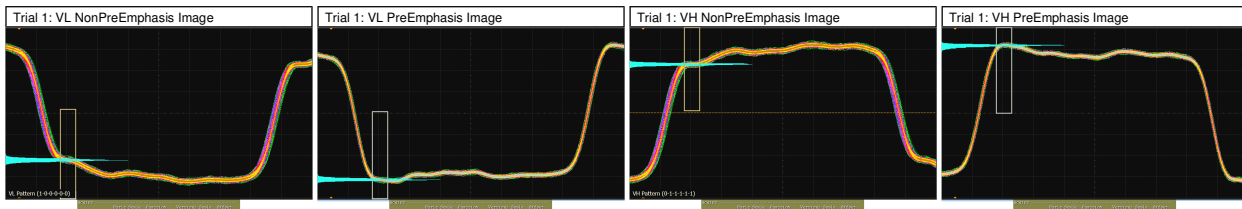
Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 1.600 dB | **PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2)** -87 mdB

**Result Details**

VL NonPreEmphasis Image (See image) | VL PreEmphasis Image (See image) | VH NonPreEmphasis Image (See image) | VH PreEmphasis Image (See image) | Number of UI 1000  
 VSwing PreEmphasis (Transition Bit) 806.433 mV | VSwing PreEmphasis (Non Transition Bit) 720.094 mV | PreEmphasis Result 984 mdB | BitRate 5.4 Gbps | Level Swing 0  
 PreEmphasis Pre-emphasis 3 | SSC SSC Disabled | PostCursor2 Level 0

**Trial 1**



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**✗ Lane 1 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)**

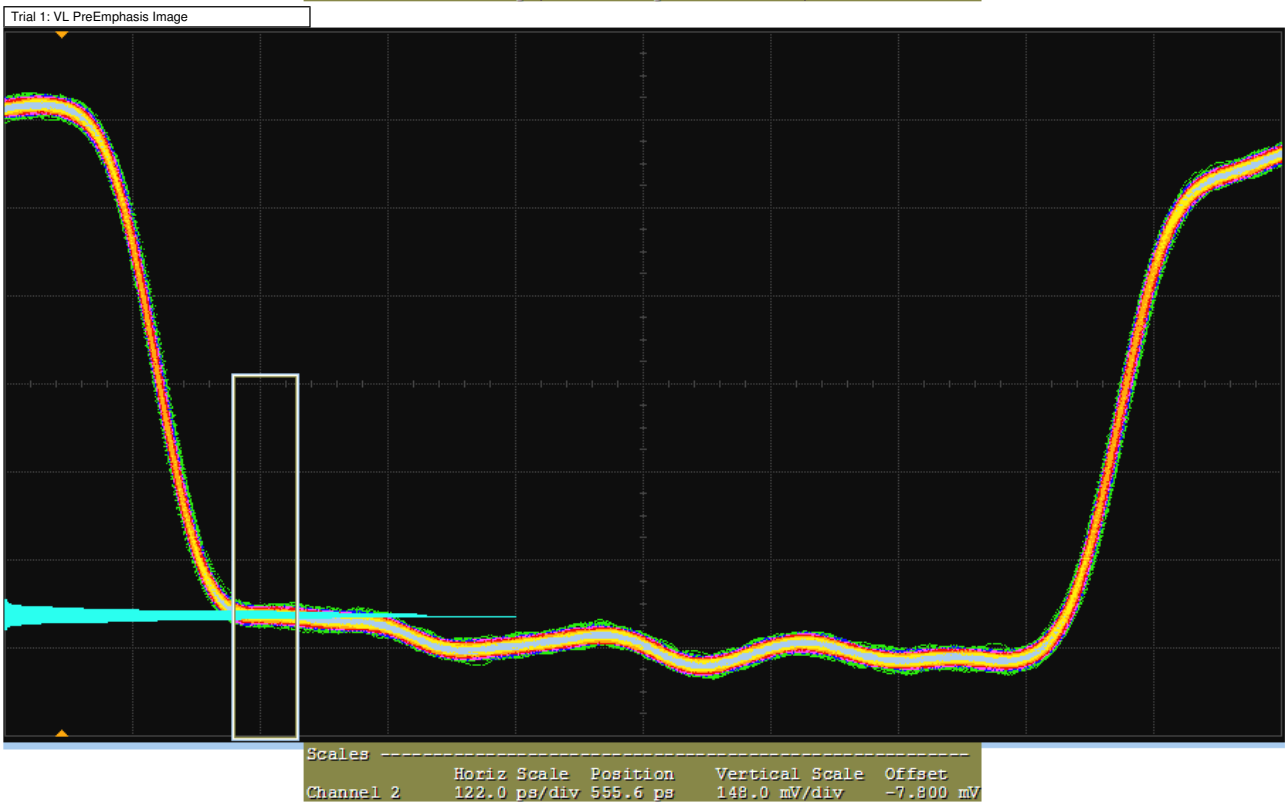
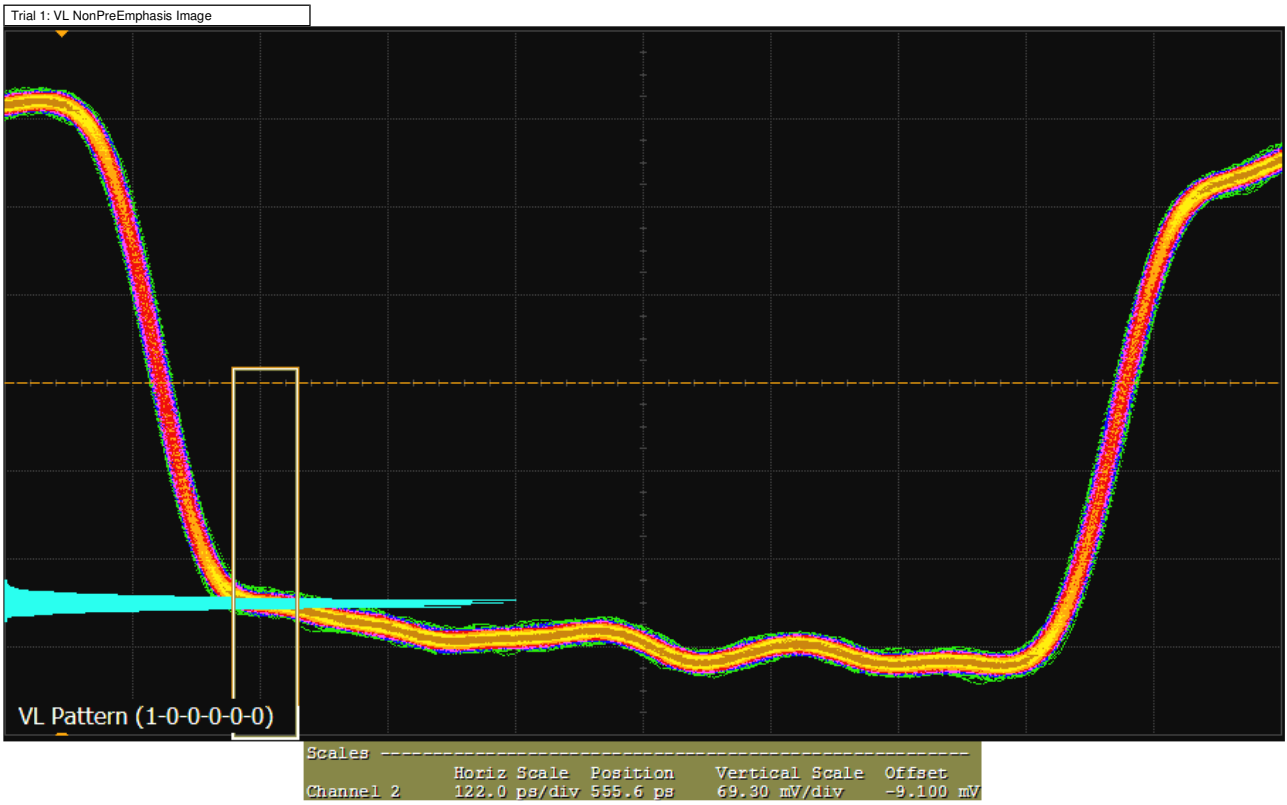
Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

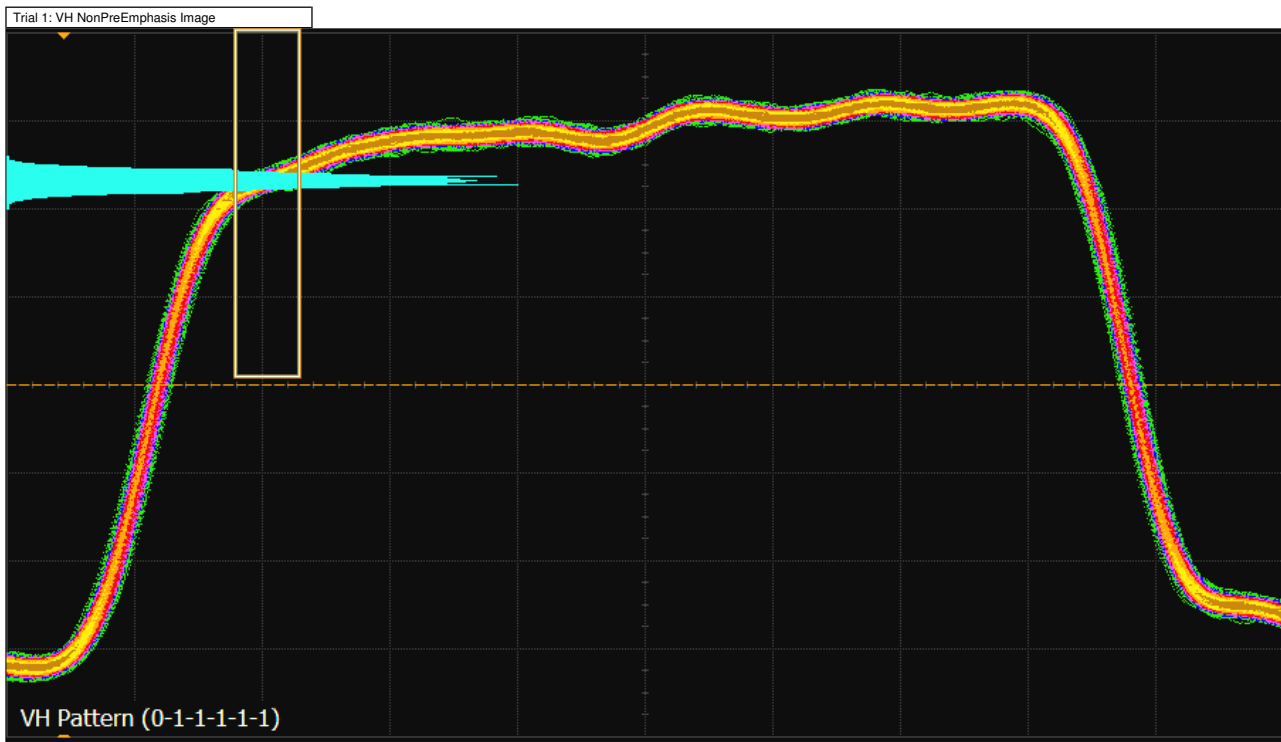
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 1.600 dB | **PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2)** -3.393 dB

**Result Details**

VL NonPreEmphasis Image (See image) | VL PreEmphasis Image (See image) | VH NonPreEmphasis Image (See image) | VH PreEmphasis Image (See image) | Number of UI 1000  
 VSwing PreEmphasis (Transition Bit) 740.882 mV | VSwing PreEmphasis (Non Transition Bit) 891.031 mV | PreEmphasis Result -1.603 dB | BitRate 5.4 Gbps | Level Swing 0  
 PreEmphasis Pre-emphasis 3 | SSC SSC Disabled | PostCursor2 Level 0

**Trial 1**





Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	69.30 mV/div	-9.100 mV

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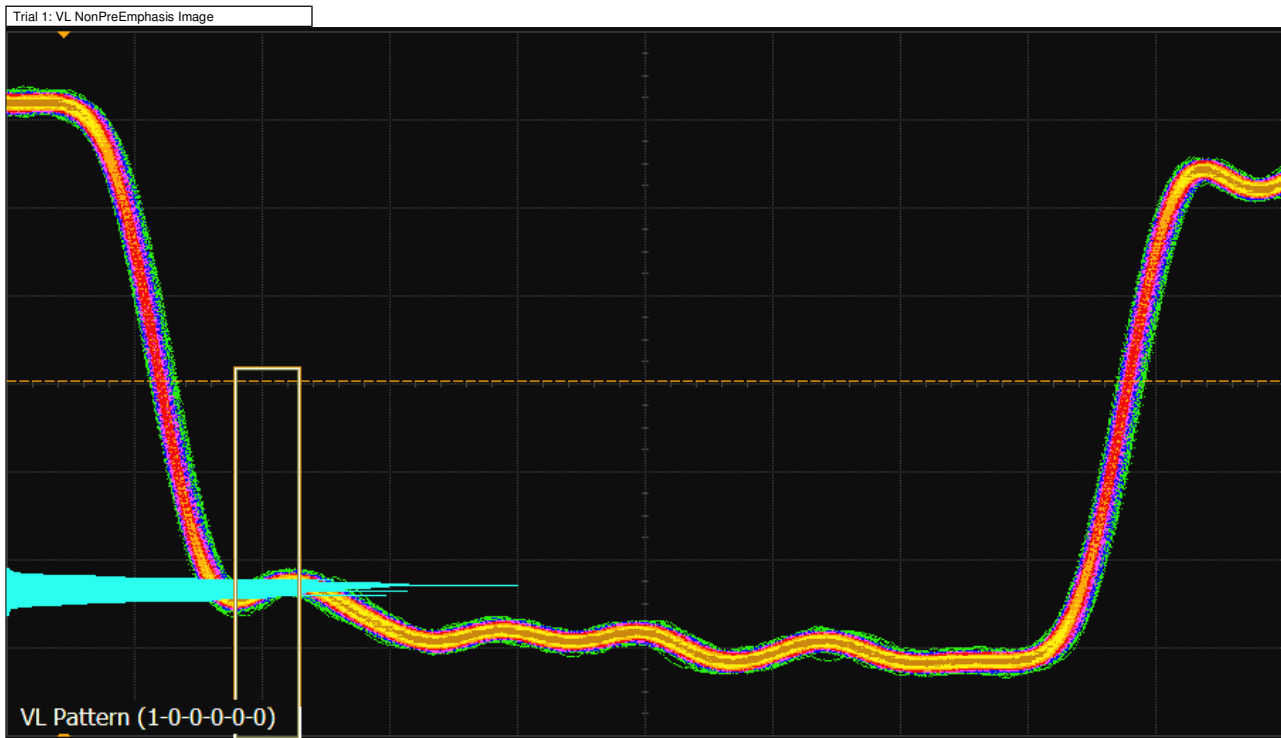
**✖ Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)** Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits:  $\geq 1.600$  dB | PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2)  $-6.295$  dB

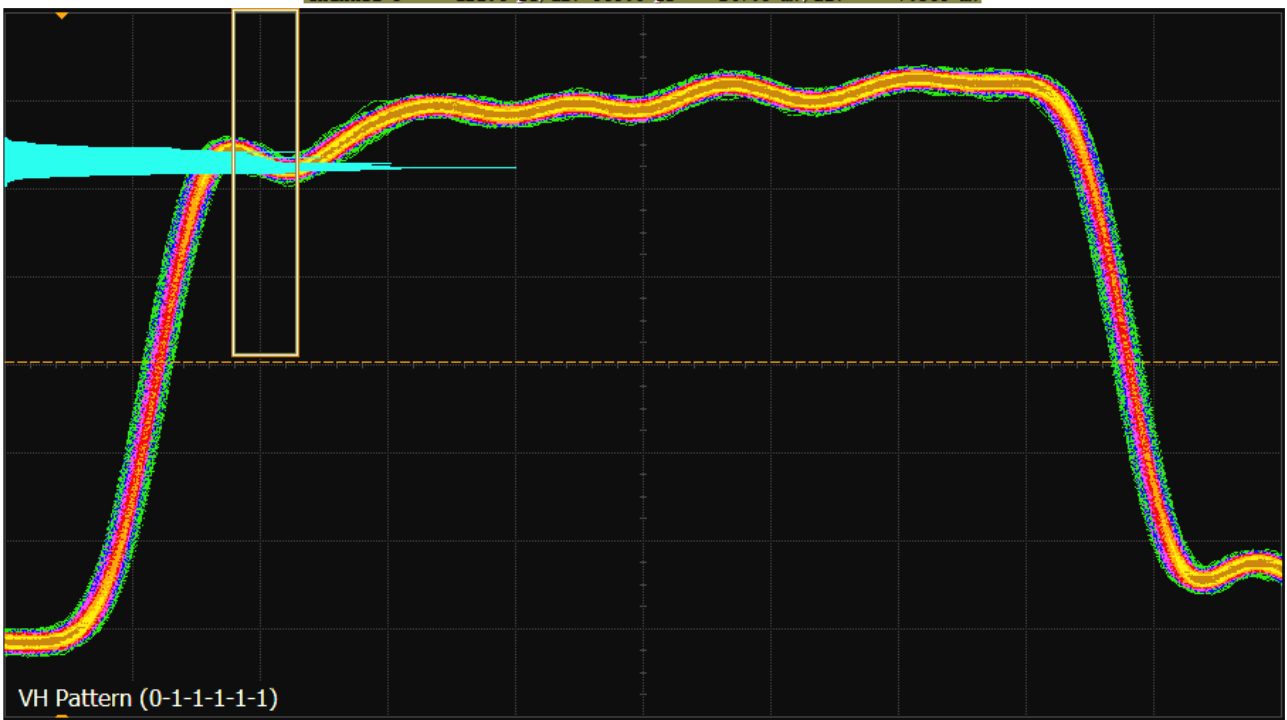
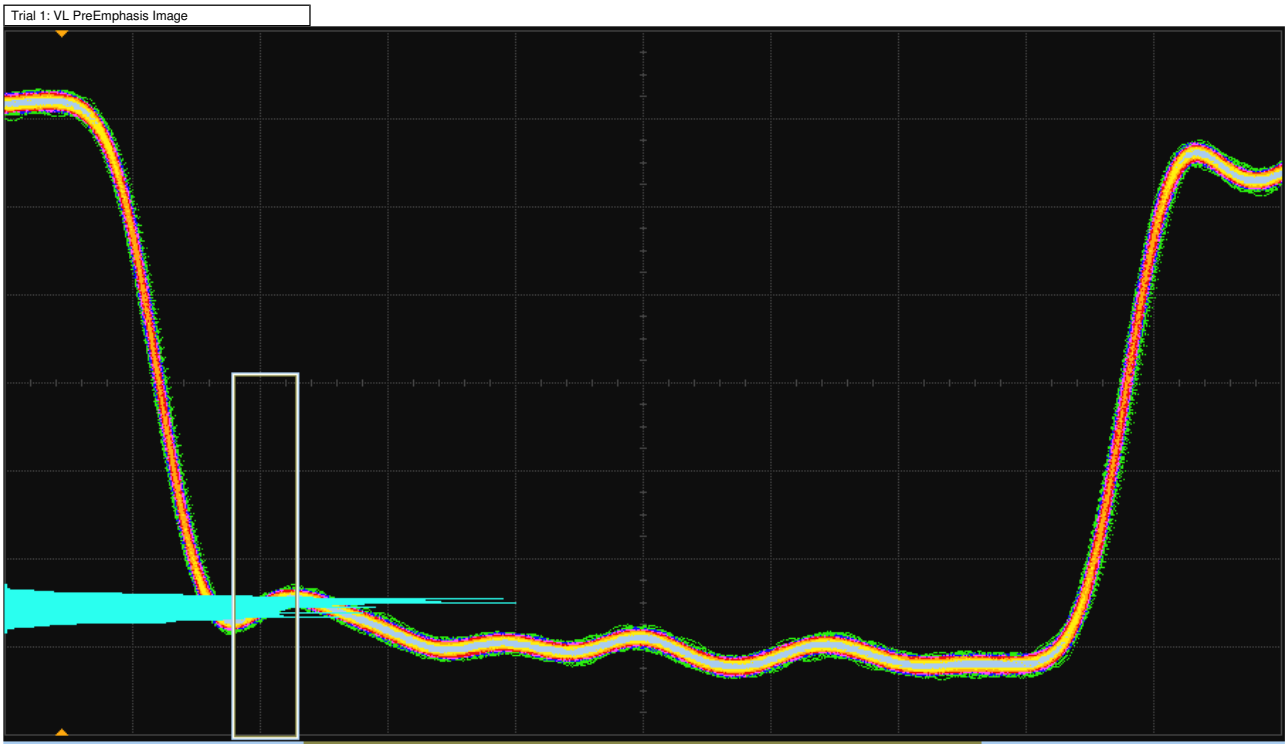
**Result Details**

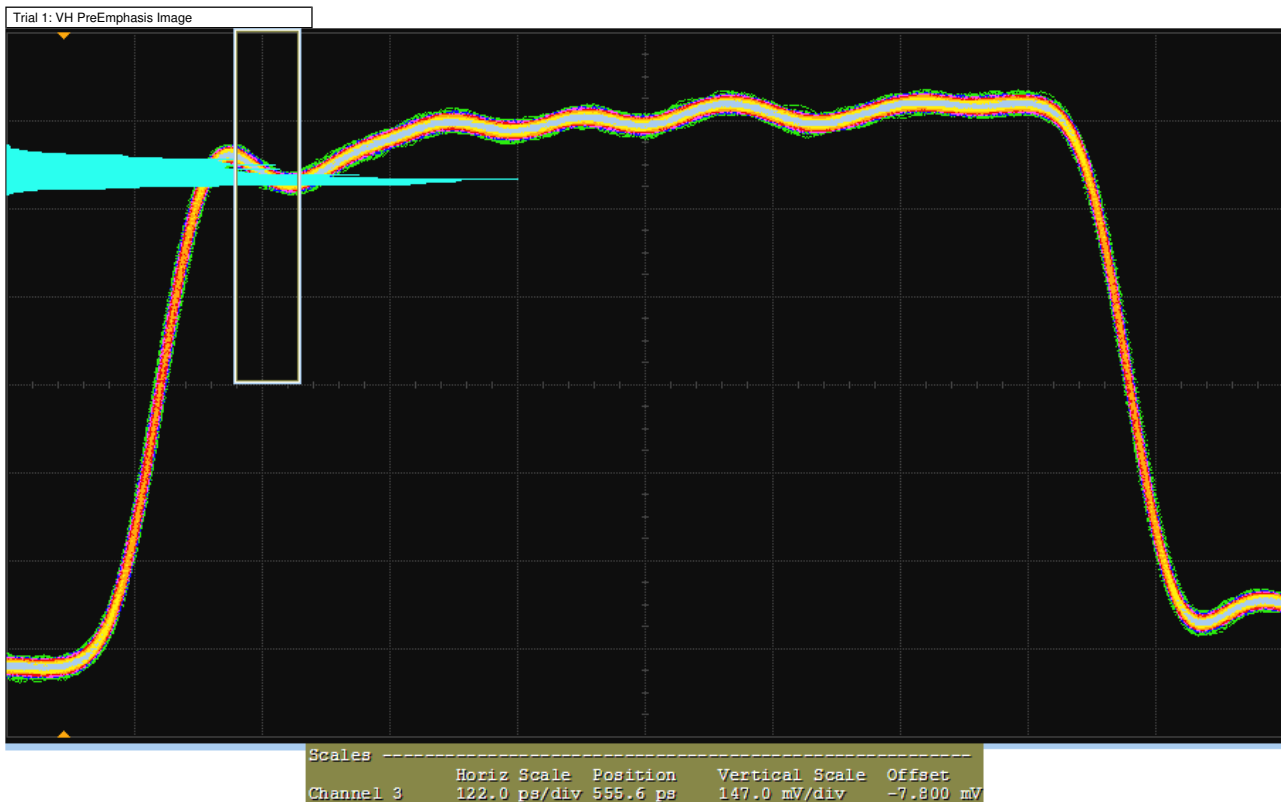
VL NonPreEmphasis Image (See image) | VL PreEmphasis Image (See image) | VH NonPreEmphasis Image (See image) | VH PreEmphasis Image (See image) | Number of UI 1000  
 VSwing PreEmphasis (Transition Bit) 727.709 mV | VSwing PreEmphasis (Non Transition Bit) 902.888 mV | PreEmphasis Result -1.874 dB | BitRate 5.4 Gbps | Level Swing 0  
 PreEmphasis Pre-emphasis 3 | SSC SSC Disabled | PostCursor2 Level 0

Trial 1



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	70.40 mV/div	-7.800 mV





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✓ Lane 3 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

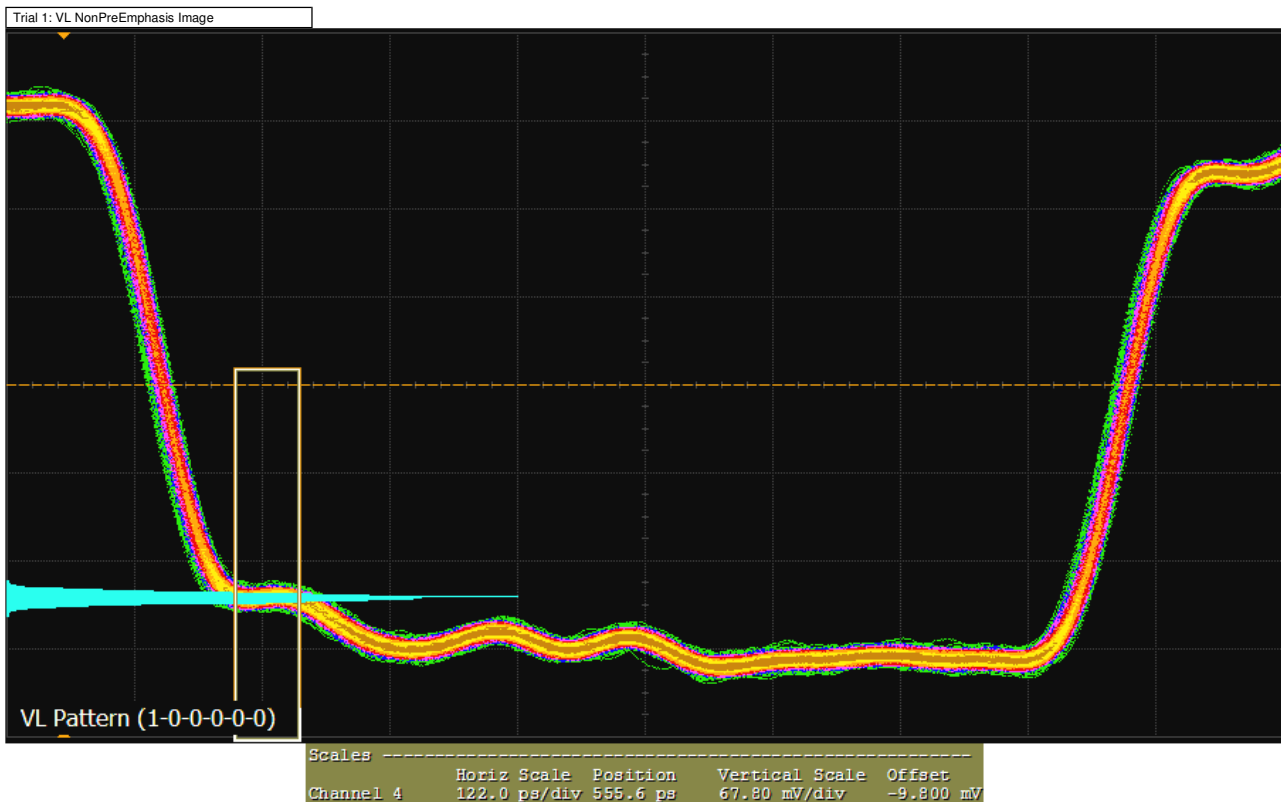
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

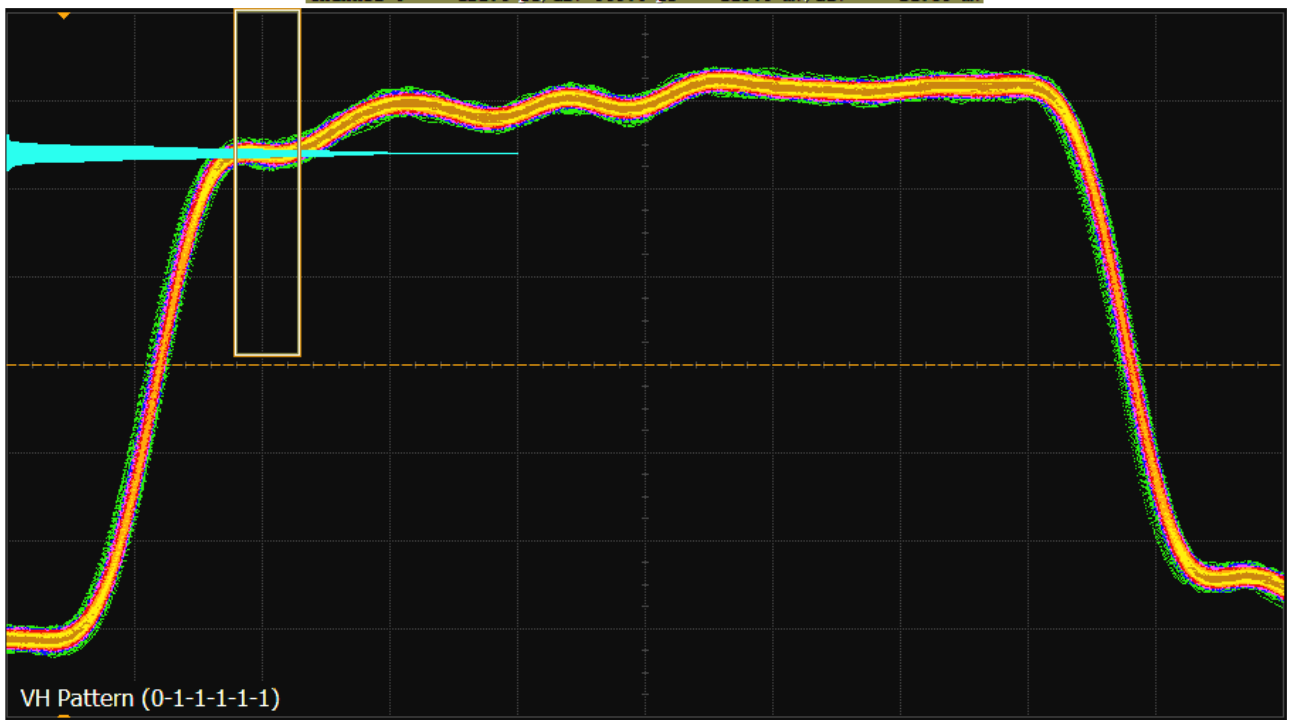
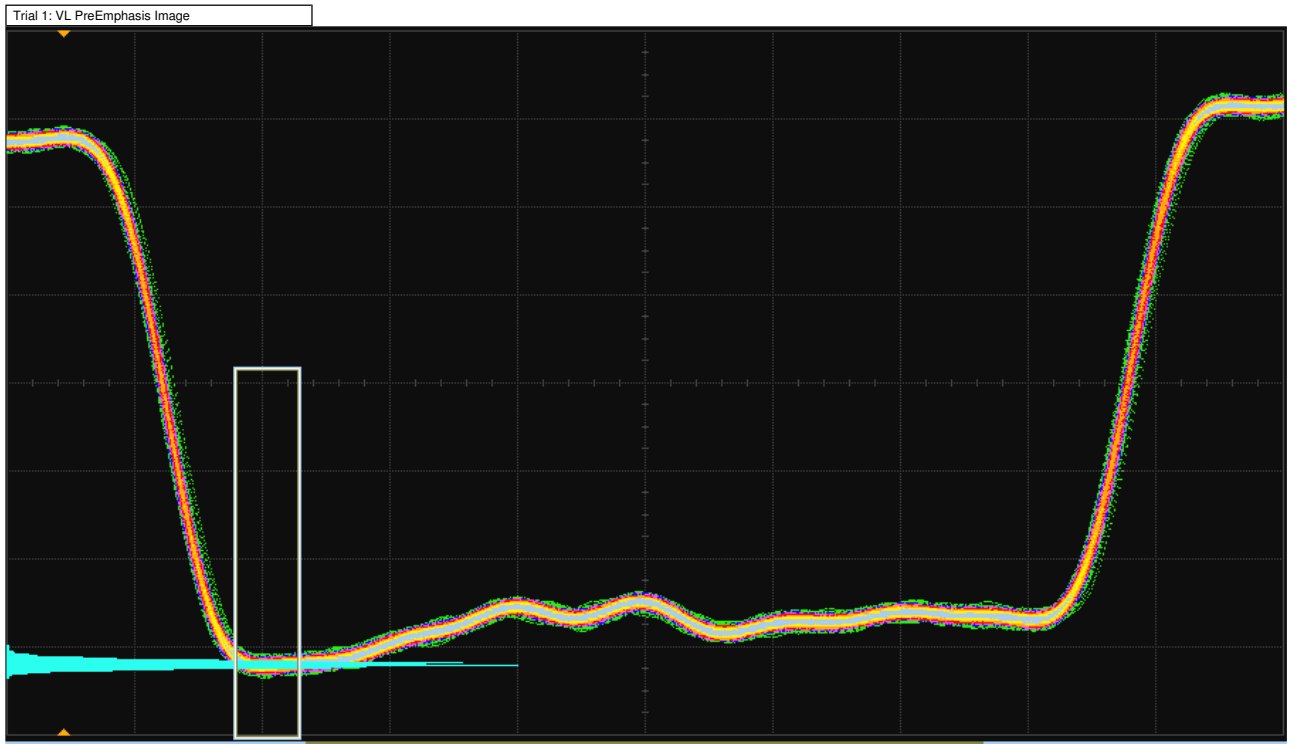
Pass Limits: >= 1.600 dB PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2) 3.230 dB

Result Details

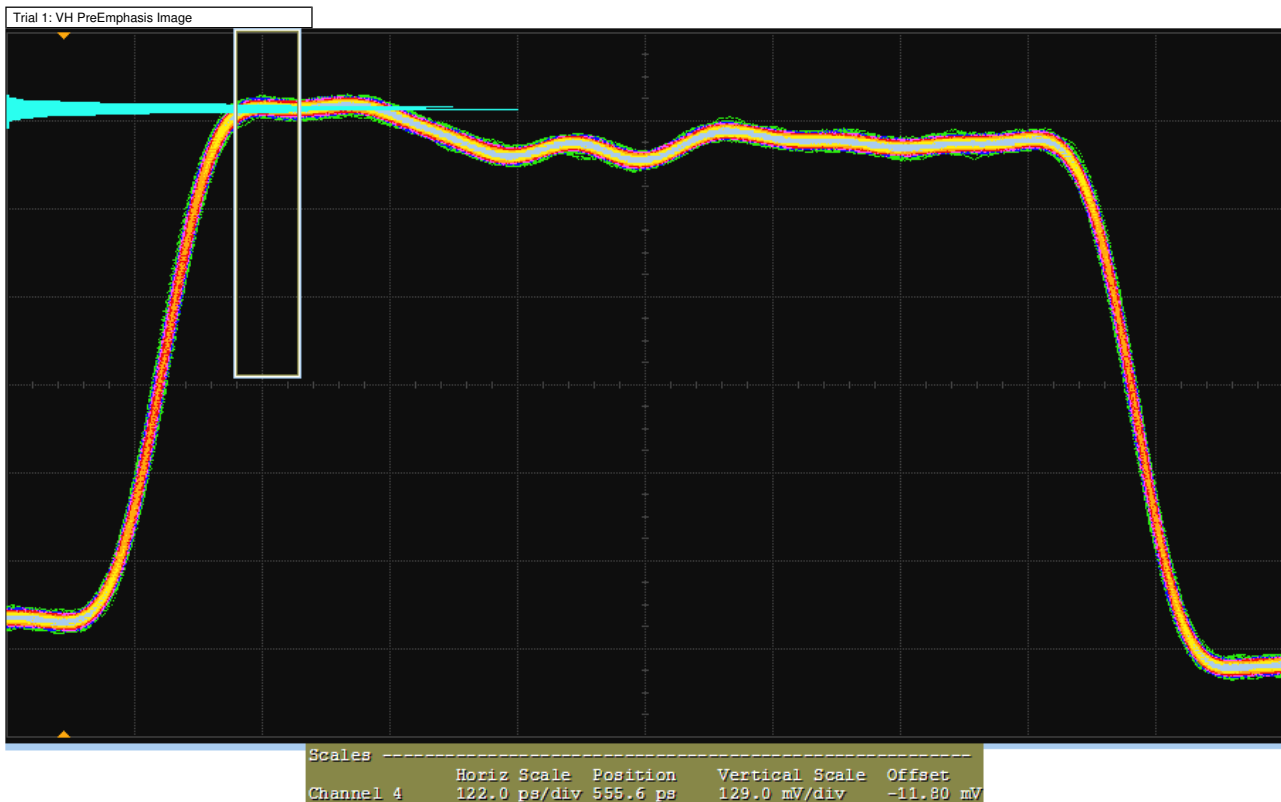
VL NonPreEmphasis Image (See image)
VL PreEmphasis Image (See image)
VH NonPreEmphasis Image (See image)
VH PreEmphasis Image (See image)
Number of UI 1000  
VSwing PreEmphasis (Transition Bit) 855.533 mV
VSwing PreEmphasis (Non Transition Bit) 727.115 mV
PreEmphasis Result 1.413 dB
BitRate 5.4 Gbps
Level Swing 0  
PreEmphasis Pre-emphasis 3
SSC SSC Disabled
PostCursor2 Level 0

Trial 1









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✓ Lane 0 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 850 m Non-Transition Voltage Range 1.164

Result Details

VSwing Non-Transition Bit(Pre-emphasis 0)	407.879 mV	VSwing Non-Transition Bit(Pre-emphasis 1)	341.692 mV	VSwing Non-Transition Bit(Pre-emphasis 2)	474.745 mV
VSwing Non-Transition Bit(Pre-emphasis 3)	720.094 mV	VSwing Non-Transition Bit(Max)	720.094 mV	VSwing Non-Transition Bit(Min)	474.745 mV
BitRate	5.4 Gbps	Level	Swing 0	PreEmphasis	Pre-emphasis 3
SSC	SSC Disabled	PostCursor2	Level 0		

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✓ Lane 1 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 850 m Non-Transition Voltage Range 1.160

Result Details

VSwing Non-Transition Bit(Pre-emphasis 0)	408.211 mV	VSwing Non-Transition Bit(Pre-emphasis 1)	501.513 mV	VSwing Non-Transition Bit(Pre-emphasis 2)	473.588 mV
VSwing Non-Transition Bit(Pre-emphasis 3)	891.031 mV	VSwing Non-Transition Bit(Max)	891.031 mV	VSwing Non-Transition Bit(Min)	473.588 mV
BitRate	5.4 Gbps	Level	Swing 0	PreEmphasis	Pre-emphasis 3
SSC	SSC Disabled	PostCursor2	Level 0		

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✓ Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 850 m Non-Transition Voltage Range 957 m

Result Details

VSwing Non-Transition Bit(Pre-emphasis 0)	425.095 mV	VSwing Non-Transition Bit(Pre-emphasis 1)	414.278 mV	VSwing Non-Transition Bit(Pre-emphasis 2)	406.783 mV
VSwing Non-Transition Bit(Pre-emphasis 3)	902.888 mV	VSwing Non-Transition Bit(Max)	902.888 mV	VSwing Non-Transition Bit(Min)	406.783 mV
BitRate	5.4 Gbps	Level	Swing 0	PreEmphasis	Pre-emphasis 3
SSC	SSC Disabled	PostCursor2	Level 0		

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✓ Lane 3 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 850 m Non-Transition Voltage Range 1.439

Result Details

VSwing Non-Transition Bit(Pre-emphasis 0)	402.157 mV	VSwing Non-Transition Bit(Pre-emphasis 1)	496.921 mV	VSwing Non-Transition Bit(Pre-emphasis 2)	578.852 mV
VSwing Non-Transition Bit(Pre-emphasis 3)	727.115 mV	VSwing Non-Transition Bit(Max)	727.115 mV	VSwing Non-Transition Bit(Min)	578.852 mV
BitRate	5.4 Gbps	Level	Swing 0	PreEmphasis	Pre-emphasis 3
SSC	SSC Disabled	PostCursor2	Level 0		

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✓ Lane 0 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2: Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

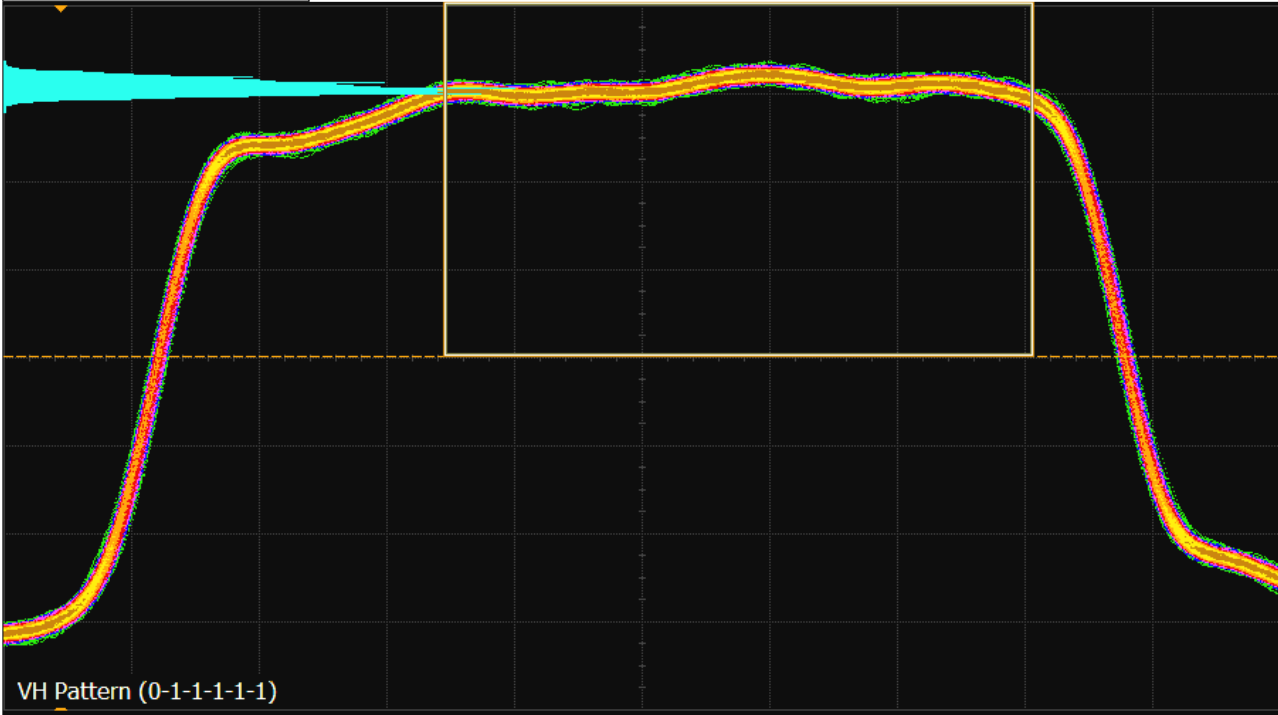
Pass Limits: [1.0000 dB to 4.4000 dB] Lane 0 Non-PreEmphasis Level Test (Swing 3/Swing 2) 1.9634 dB

**Result Details**

Level VH Image (Swing 3) (See image)	Level VL Image (Swing 3) (See image)	Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 3) 481.132 mV	VBase (Swing 3) -508.365 mV	VSwing (Swing 3) 989.497 mV
VBase(Swing 2) -406.953 mV	VSwing(Swing 2) 789.302 mV	Test Mode Compliance	Test Layer Physical Layer Tests	Test Condition Compliance Conditions Only
Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps	Level Swing 3	PreEmphasis Pre-emphasis 0
				SSC SSC Disabled
				PostCursor2 Level 0

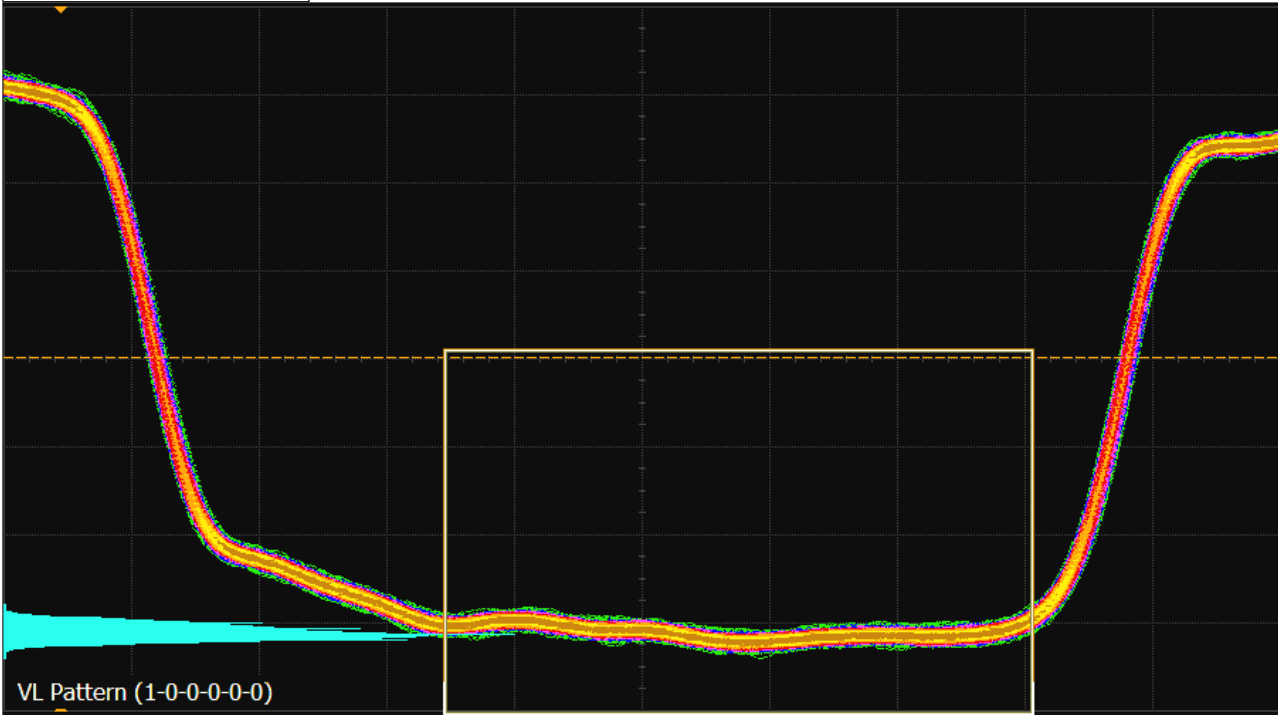
Trial 1

Trial 1: Level VH Image (Swing 3)

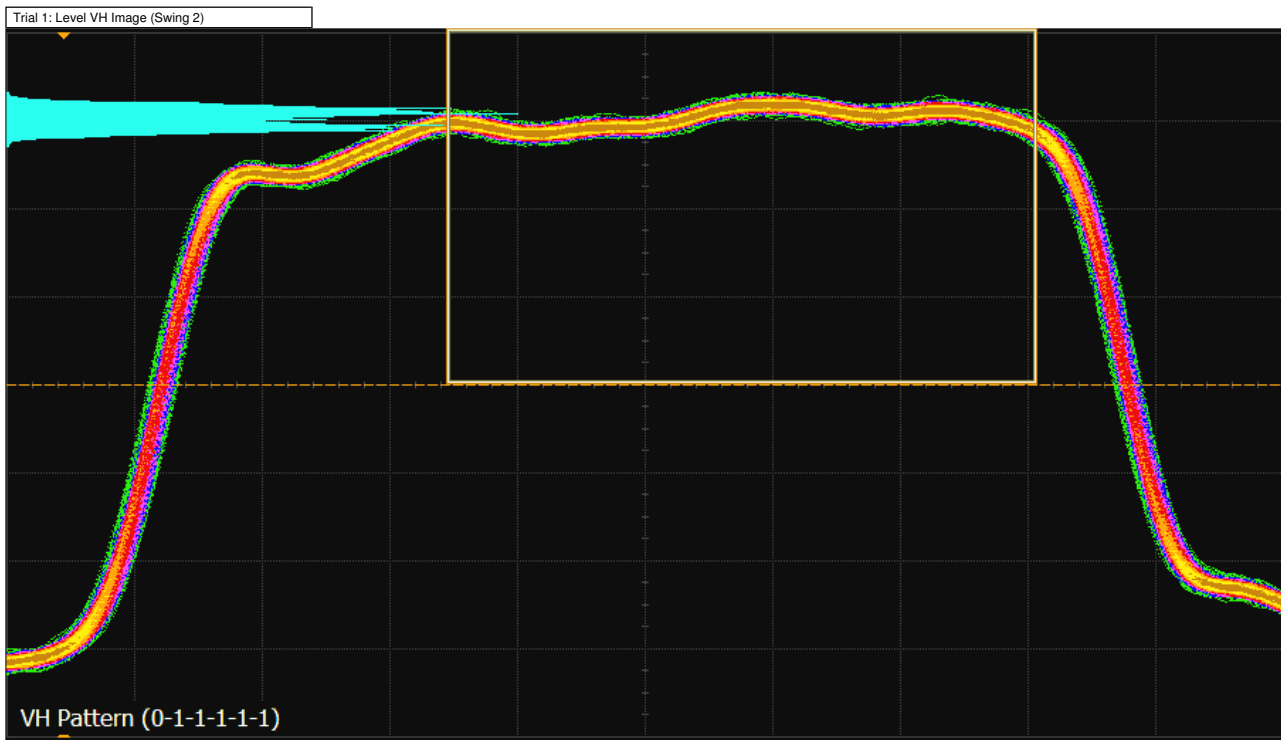


Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	161.0 mV/div	-8.500 mV

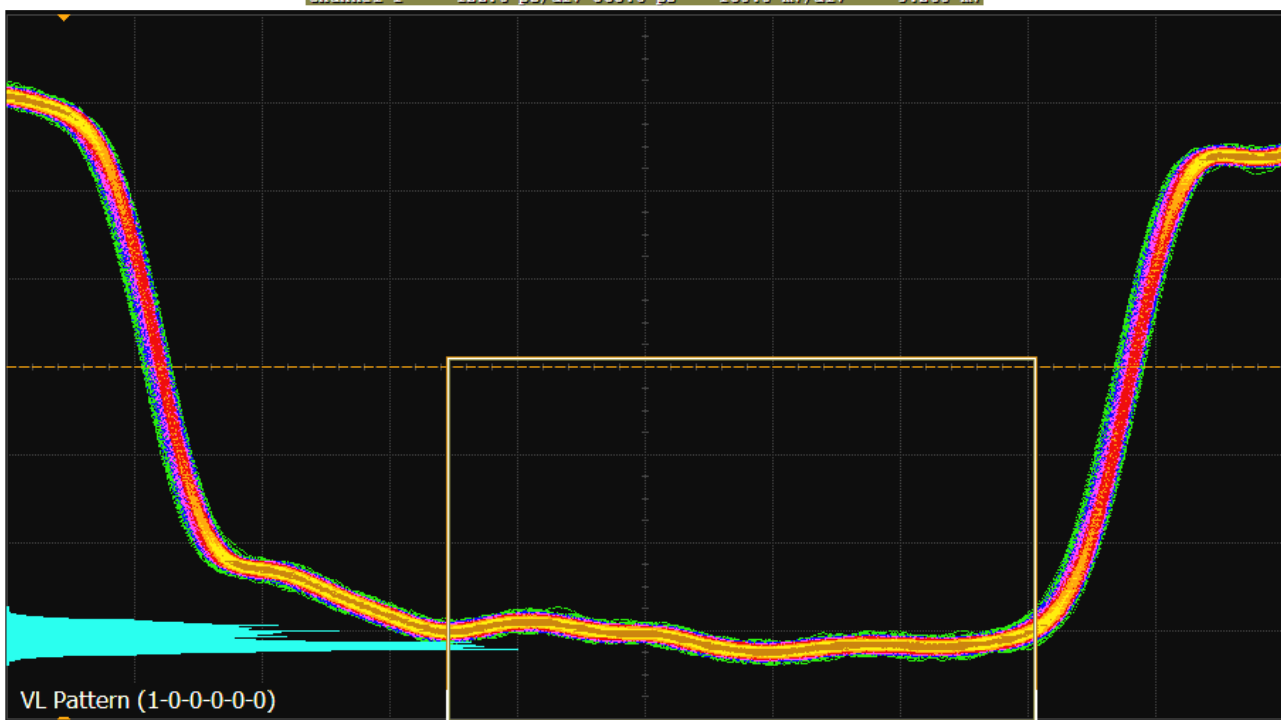
Trial 1: Level VL Image (Swing 3)



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	161.0 mV/div	-8.500 mV



Scales				
Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	130.0 mV/div	-9.200 mV



Scales				
Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	122.0 ps/div	555.6 ps	130.0 mV/div	-9.200 mV

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Lane 1 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

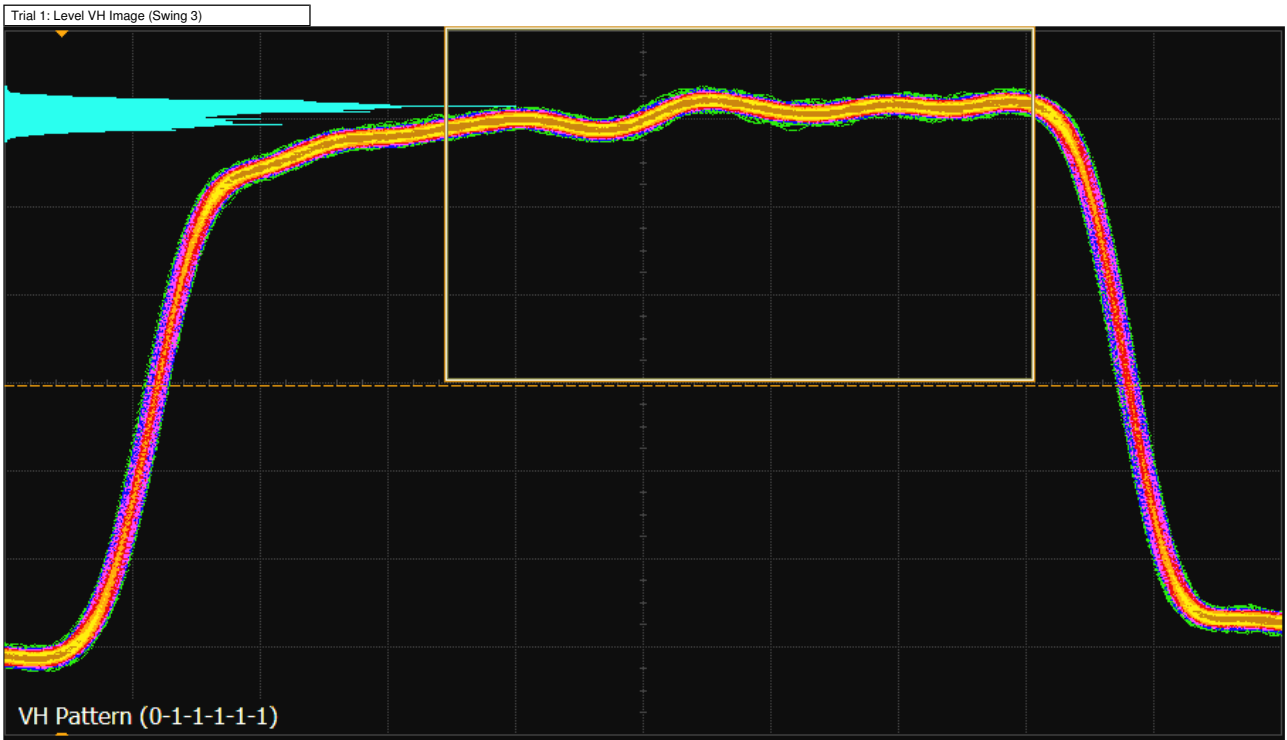
Test Summary:  Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Pass Limits: [1.0000 dB to 4.4000 dB] Lane 1 Non-PreEmphasis Level Test (Swing 3/Swing 2) 1.9420 dB

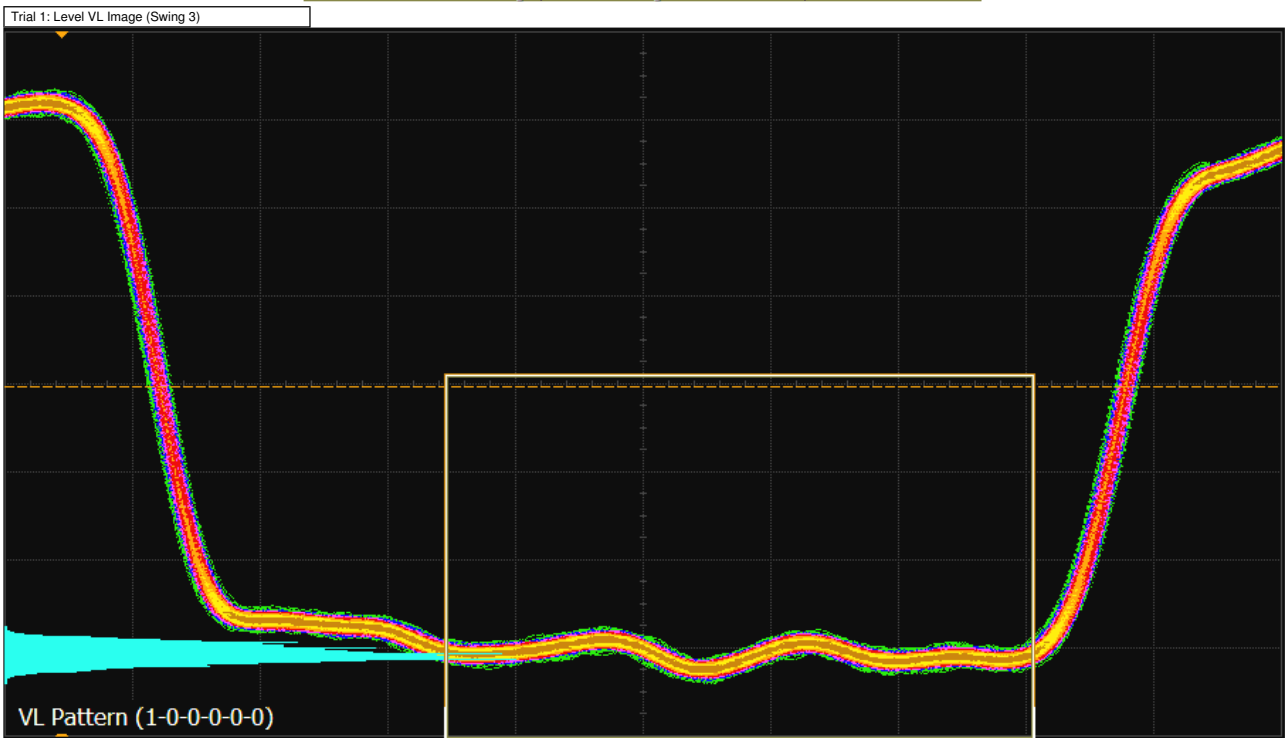
**Result Details**

Level VH Image (Swing 3) (See image)	Level VL Image (Swing 3) (See image)	Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 3) 481.373 mV	VBase (Swing 3) -500.341 mV	VSwing (Swing 3) 981.714 mV
VTop (Swing 2) 381.989 mV	VBase (Swing 2) -403.042 mV	VSwing (Swing 2) 785.031 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 3	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

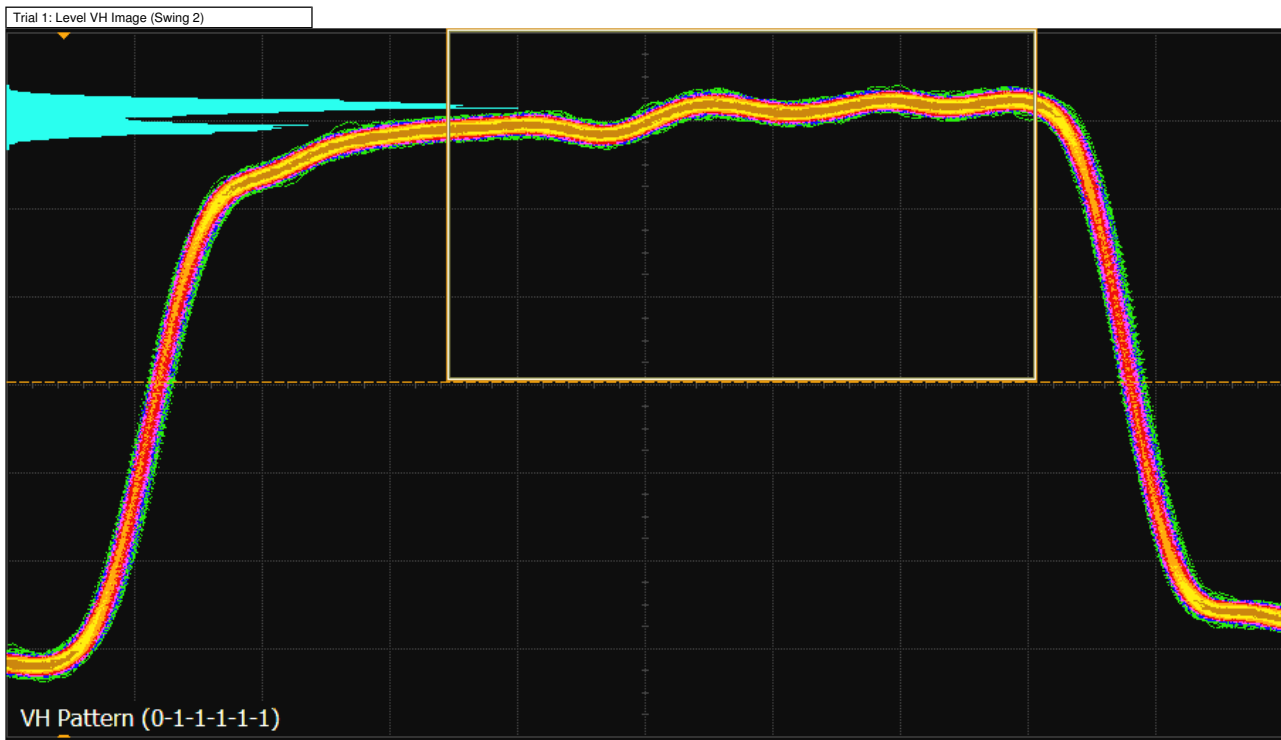
Trial 1



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	162.0 mV/div	-14.30 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	122.0 ps/div	555.6 ps	162.0 mV/div	-14.30 mV



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✓ Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2: Table 3.10 VESA DisplayPort Standard specification

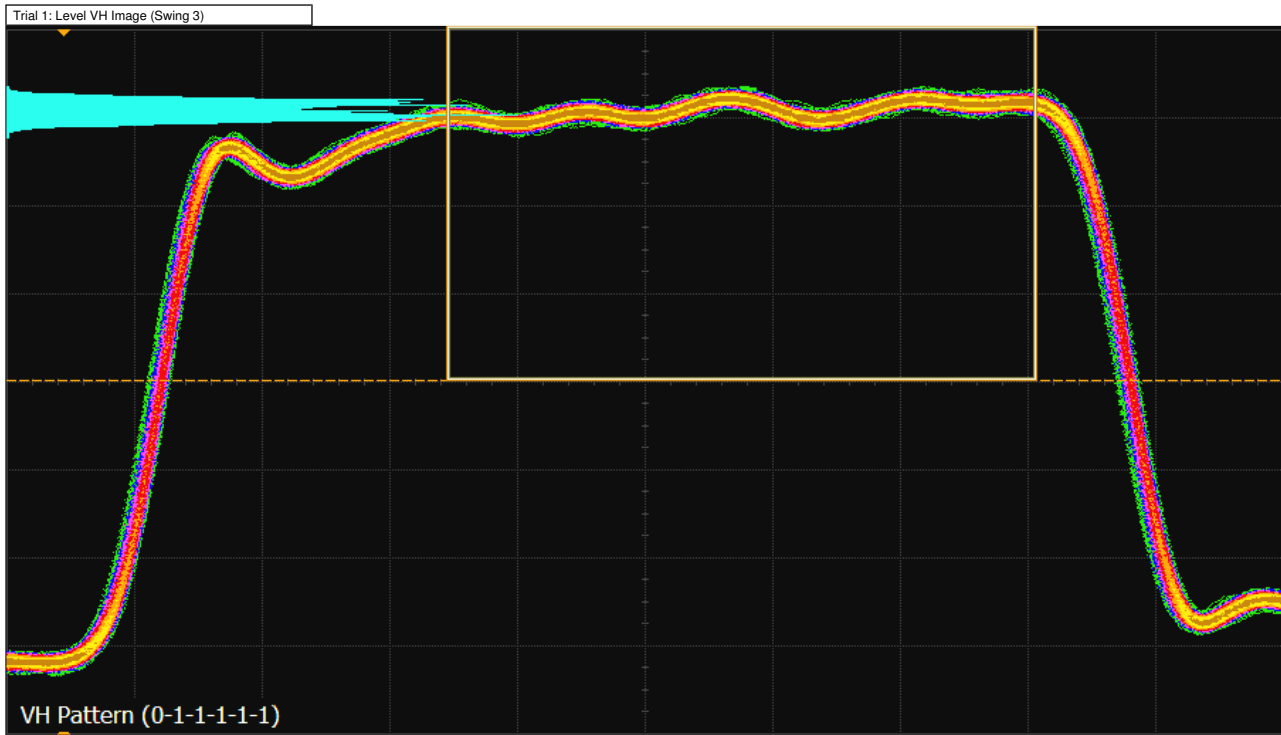
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

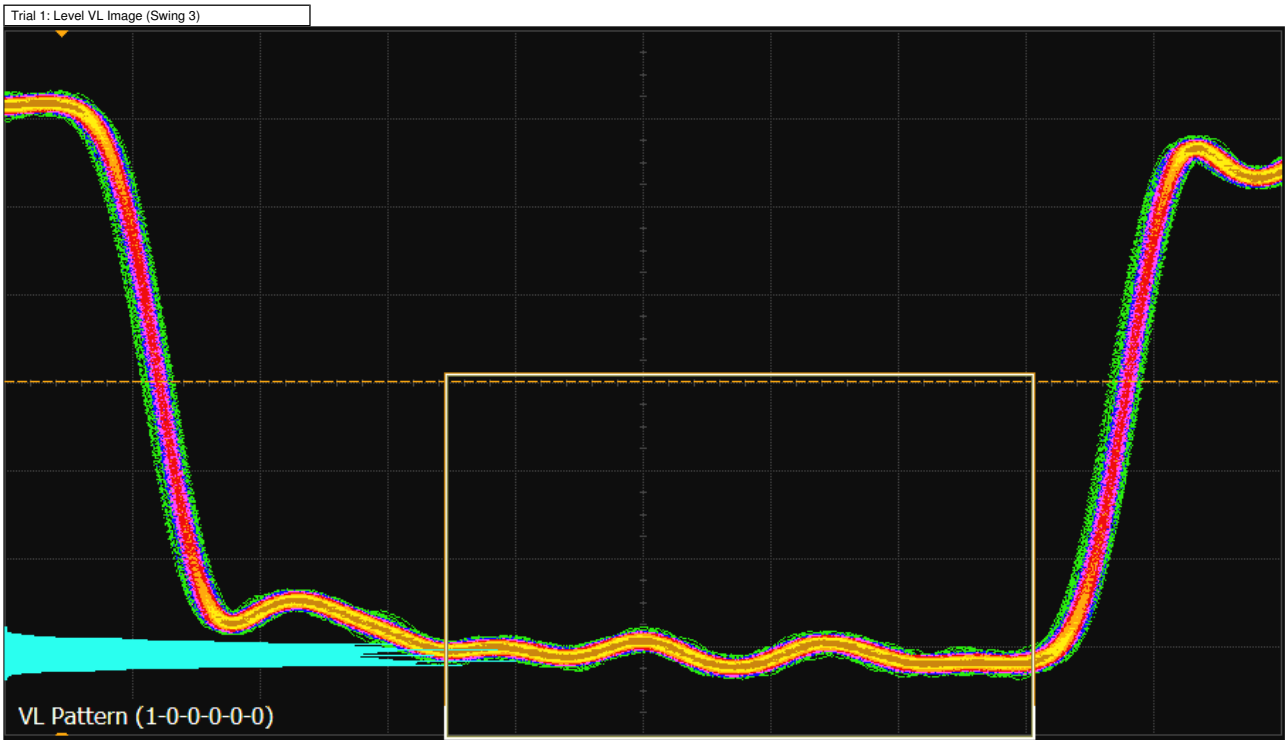
Pass Limits: [1.0000 dB to 4.4000 dB] Lane 2 Non-PreEmphasis Level Test (Swing 3/Swing 2) 1.8821 dB

Result Details

Level VH Image (Swing 3) (See image)	Level VL Image (Swing 3) (See image)	Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 3) 486.366 mV	VBase (Swing 3) -507.311 mV	VSwing (Swing 3) 993.677 mV
VTop (Swing 2) 389.754 mV	VBase (Swing 2) -410.343 mV	VSwing (Swing 2) 800.097 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 3	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

Trial 1

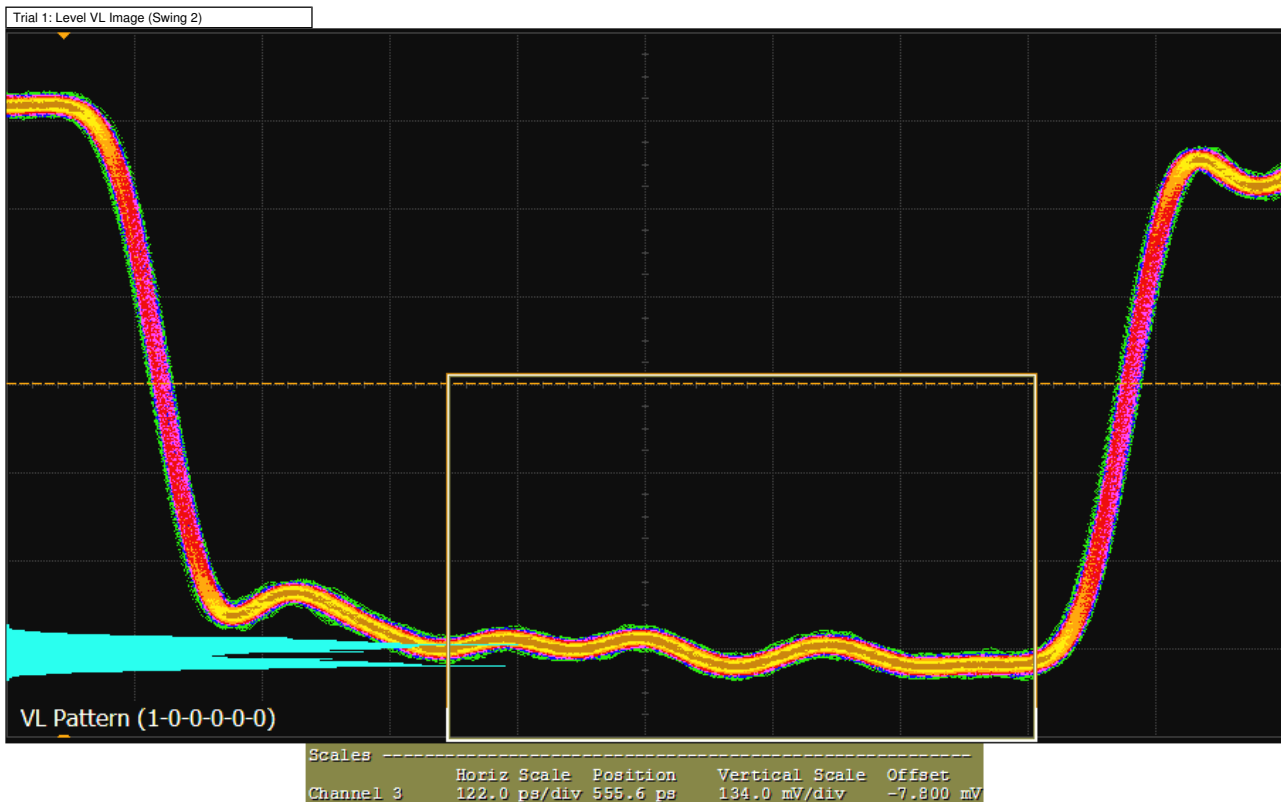




Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	162.0 mV/div	-8.000 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	122.0 ps/div	555.6 ps	134.0 mV/div	-7.800 mV



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✓ Lane 3 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

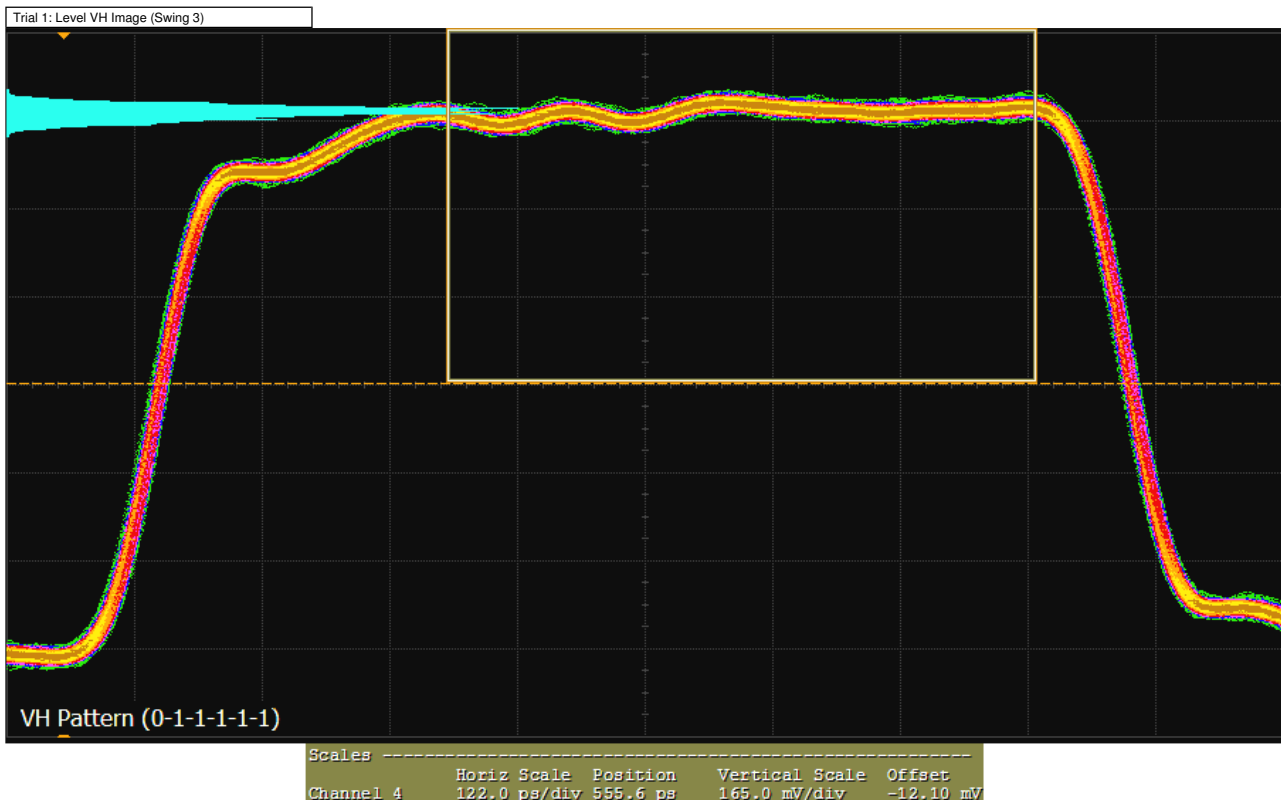
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Pass Limits: [1.0000 dB to 4.4000 dB] Lane 3 Non-PreEmphasis Level Test (Swing 3/Swing 2) 2.0353 dB

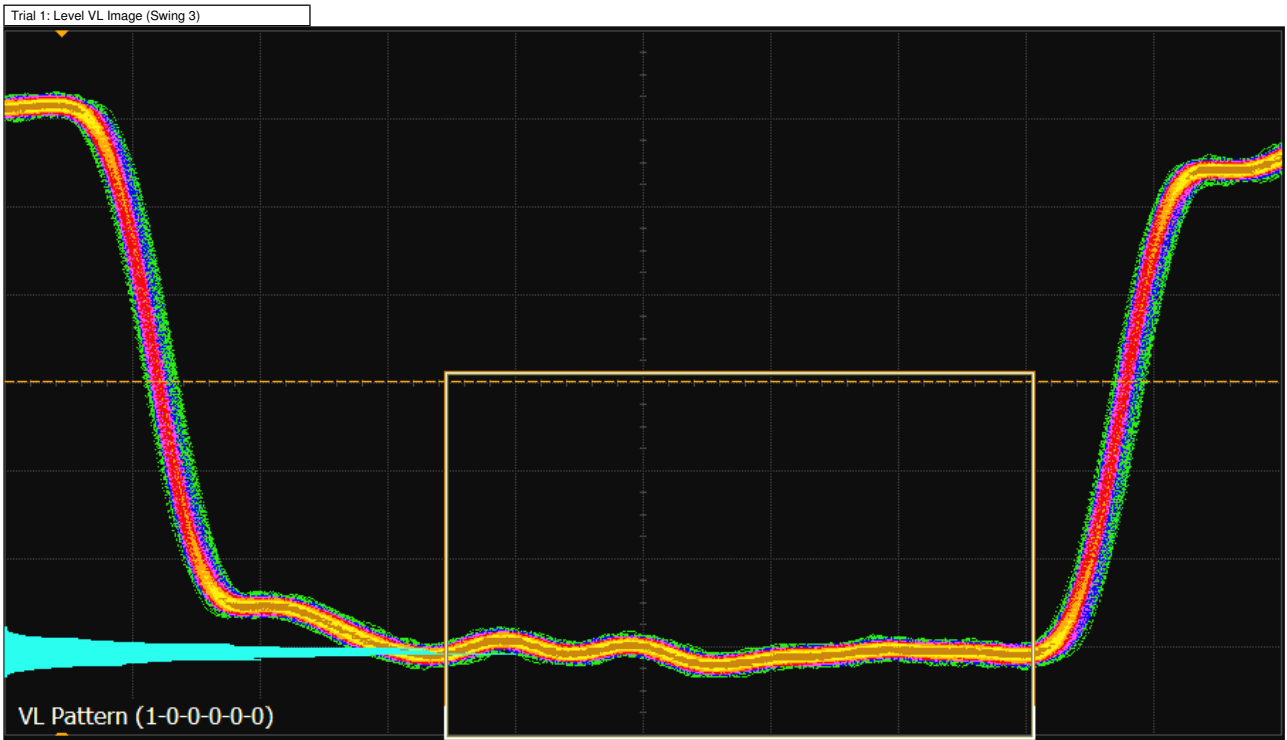
Result Details

Level VH Image (Swing 3) (See image)	Level VL Image (Swing 3) (See image)	Level VH Image (Swing 2) (See image)	Level VL Image (Swing 2) (See image)	Number of UI 1000
VH Trigger Pattern 011111	VL Trigger Pattern 100000	VTop (Swing 3) 490.643 mV	VBase (Swing 3) -513.343 mV	VSwing (Swing 3) 1.003986 V
VTop (Swing 2) 386.243 mV	VBase (Swing 2) -408.020 mV	VSwing (Swing 2) 794.263 mV	Test Mode Compliance	Test Layer Physical Layer Tests
Test Condition Compliance Conditions Only	DUT Type Source	Test Type Differential Tests	Connection Type Differential Probe	BitRate 5.4 Gbps
Level Swing 3	PreEmphasis Pre-emphasis 0	SSC SSC Disabled	PostCursor2 Level 0	

Trial 1





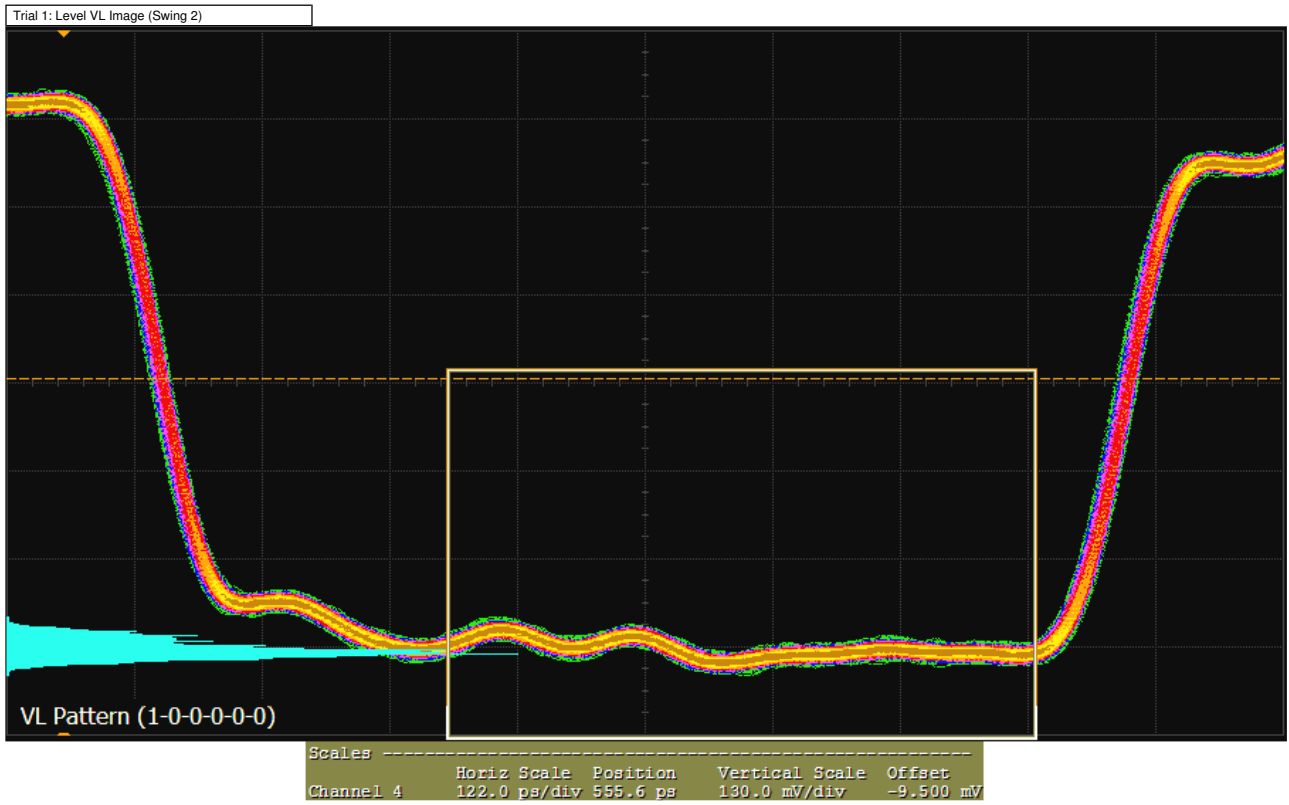


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	122.0 ps/div	555.6 ps	165.0 mV/div	-12.10 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	122.0 ps/div	555.6 ps	130.0 mV/div	-9.500 mV





✓ Lane 0 - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the Peak to Peak Voltage.  
**Pass Limits:** <= 1.380 V | **Peak to Peak Voltage (Worst of 20 Trials)** 1.172 V | **# Trials Run:** 20 | **Worst Trial:** Trial 12

Overall Summary + details of 20 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	905.6 mV	34.38 %													
	<i>StdDev</i>	223.3 mV	16.19 %													
	<i>Range</i>	687.7 mV	49.86 %													
	<i>Min</i>	484.3 mV	15.07 %													
	<i>Max</i>	1.172 V	64.93 %													
	<i>Sum</i>	18.11 V	687.6 %													
✓	Trial 1	924 mV	33.0%	447.100 mV	-476.540 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	1.130 V	18.1%	553.540 mV	-576.340 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	686 mV	50.3%	330.000 mV	-356.030 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	969 mV	29.8%	471.950 mV	-496.750 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	1.018 V	26.2%	494.150 mV	-523.890 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 6	484 mV	64.9%	231.460 mV	-252.790 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 7	694 mV	49.7%	332.310 mV	-362.110 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	738 mV	46.5%	355.690 mV	-382.690 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	1.081 V	21.7%	527.650 mV	-553.640 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10	1.146 V	17.0%	559.840 mV	-586.290 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 11	960 mV	30.4%	464.670 mV	-494.980 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 12 (Worst)	1.172 V	15.1%	575.660 mV	-596.280 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 13	708 mV	48.7%	342.340 mV	-365.540 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 14	1.020 V	26.1%	499.320 mV	-521.150 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 15	1.077 V	22.0%	527.510 mV	-549.580 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 16	492 mV	64.3%	231.960 mV	-259.660 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 17	726 mV	47.4%	352.080 mV	-374.310 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 18	786 mV	43.0%	384.470 mV	-401.980 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 19	1.133 V	17.9%	554.440 mV	-578.110 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 20	1.167 V	15.4%	567.140 mV	-600.340 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 1 - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: **Pass**    Test Description: To evaluate the peak to peak voltage.  
**Pass Limits:** <= 1.380 V    **Peak to Peak Voltage (Worst of 20 Trials)** 1.180 V    **# Trials Run:** 20    **Worst Trial:** Trial 20

Overall Summary + details of 20 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	<i>870.9 mV</i>	<i>36.89 %</i>													
	<i>StdDev</i>	<i>217.7 mV</i>	<i>15.77 %</i>													
	<i>Range</i>	<i>685.9 mV</i>	<i>49.71 %</i>													
	<i>Min</i>	<i>494.0 mV</i>	<i>14.49 %</i>													
	<i>Max</i>	<i>1.180 V</i>	<i>64.20 %</i>													
	<i>Sum</i>	<i>17.42 V</i>	<i>737.8 %</i>													
✓	Trial 1	944 mV	31.6%	462.820 mV	-480.920 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	1.045 V	24.3%	517.500 mV	-527.500 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	704 mV	49.0%	347.450 mV	-356.670 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	849 mV	38.5%	418.070 mV	-431.410 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	1.021 V	26.0%	493.950 mV	-527.020 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 6	499 mV	63.8%	241.660 mV	-257.220 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 7	601 mV	56.4%	292.780 mV	-308.010 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	744 mV	46.1%	355.510 mV	-388.150 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	1.048 V	24.1%	522.400 mV	-525.800 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10	1.150 V	16.7%	571.540 mV	-578.580 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 11	951 mV	31.1%	474.530 mV	-476.080 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 12	1.070 V	22.5%	539.710 mV	-530.610 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 13	708 mV	48.7%	348.080 mV	-359.790 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 14	862 mV	37.5%	430.510 mV	-431.860 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 15	1.085 V	21.4%	537.810 mV	-546.980 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 16	494 mV	64.2%	241.560 mV	-252.390 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 17	604 mV	56.2%	300.000 mV	-303.740 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 18	784 mV	43.2%	383.750 mV	-400.190 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 19	1.075 V	22.1%	539.560 mV	-535.860 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 20 (Worst)	1.180 V	14.5%	589.270 mV	-590.560 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 2 - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the peak to peak voltage.  
**Pass Limits:** <= 1.380 V | **Peak to Peak Voltage (Worst of 20 Trials)** 1.176 V | **# Trials Run:** 20 | **Worst Trial:** Trial 20

Overall Summary + details of 20 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	900.4 mV	34.75 %													
	<i>StdDev</i>	211.5 mV	15.33 %													
	<i>Range</i>	667.3 mV	48.33 %													
	<i>Min</i>	508.6 mV	14.78 %													
	<i>Max</i>	1.176 V	63.12 %													
	<i>Sum</i>	18.01 V	695.0 %													
✓	Trial 1	964 mV	30.1%	474.670 mV	-489.560 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	1.086 V	21.3%	529.040 mV	-557.420 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	716 mV	48.1%	349.340 mV	-366.870 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	915 mV	33.7%	446.060 mV	-468.460 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	1.100 V	20.3%	534.710 mV	-565.320 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 6	509 mV	63.1%	245.960 mV	-262.630 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 7	653 mV	52.7%	314.950 mV	-337.670 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	833 mV	39.6%	404.010 mV	-429.210 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	1.069 V	22.5%	530.540 mV	-538.070 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10	1.146 V	17.0%	567.520 mV	-578.610 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 11	964 mV	30.1%	476.730 mV	-487.530 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 12	1.093 V	20.8%	537.420 mV	-555.820 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 13	720 mV	47.8%	354.330 mV	-365.440 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 14	908 mV	34.2%	442.910 mV	-464.830 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 15	1.084 V	21.4%	531.150 mV	-552.720 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 16	509 mV	63.1%	244.080 mV	-265.060 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 17	657 mV	52.4%	319.510 mV	-337.580 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 18	835 mV	39.5%	408.600 mV	-426.610 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 19	1.072 V	22.3%	532.120 mV	-539.750 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 20 (Worst)	1.176 V	14.8%	588.450 mV	-587.450 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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✓ Lane 3 - Peak to Peak Voltage Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the peak to peak voltage.  
 Pass Limits: <= 1.380 V Peak to Peak Voltage (Worst of 20 Trials) 1.154 V # Trials Run: 20 Worst Trial: Trial 10

Overall Summary + details of 20 worst trials

Pass	Trial	Actual Value	Margin	VMax	VMin	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	843.1 mV	38.91 %													
	<i>StdDev</i>	224.3 mV	16.24 %													
	<i>Range</i>	685.1 mV	49.64 %													
	<i>Min</i>	469.2 mV	16.38 %													
	<i>Max</i>	1.154 V	66.01 %													
	<i>Sum</i>	16.86 V	778.3 %													
✓	Trial 1	921 mV	33.3%	441.600 mV	-479.830 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	1.033 V	25.1%	500.460 mV	-532.830 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 3	683 mV	50.5%	324.940 mV	-357.800 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	836 mV	39.4%	399.600 mV	-436.400 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 5	962 mV	30.3%	463.450 mV	-498.530 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 6	480 mV	65.2%	224.750 mV	-255.080 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 7	591 mV	57.2%	280.300 mV	-310.500 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 8	683 mV	50.5%	324.530 mV	-358.040 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 9	1.096 V	20.6%	532.570 mV	-563.740 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 10 (Worst)	1.154 V	16.4%	565.190 mV	-589.160 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 11	917 mV	33.6%	447.860 mV	-468.840 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 12	1.042 V	24.5%	514.690 mV	-527.240 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 13	673 mV	51.2%	327.020 mV	-345.820 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 14	826 mV	40.1%	403.330 mV	-423.130 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 15	964 mV	30.1%	472.660 mV	-491.570 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 16	469 mV	66.0%	224.500 mV	-244.740 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 17	585 mV	57.6%	283.550 mV	-301.150 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 1	SSC Disabled	Level 0
✓	Trial 18	679 mV	50.8%	331.670 mV	-347.640 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 19	1.119 V	18.9%	555.820 mV	-563.080 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
✓	Trial 20	1.147 V	16.9%	566.130 mV	-581.330 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

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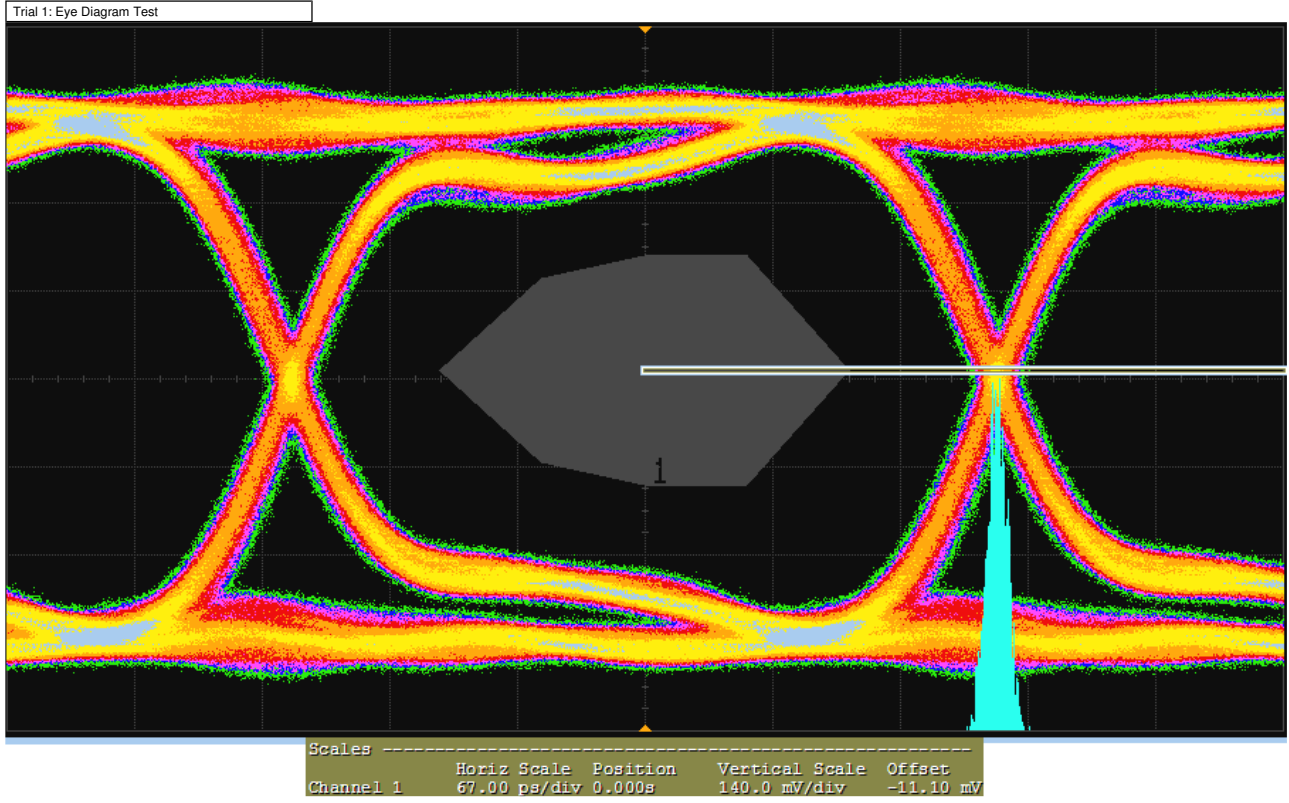
✓ Lane 0 - Eye Diagram Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (Worst of 2 Trials) 0.000 # Trials Run: 2 Worst Trial: Trial 1

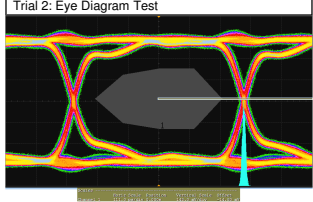
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Number of UI	Left Jitter	Right Jitter	VTop	VBase	VSwing	Mask Scalling Type	Mask Scalling Option	Mask Movement Option	Mask Movement Margin (Horizontal)	Mask Movement Margin (Vertical)	Measured Eye Height	Measured Eye Width	Vertical Scale	Test Mode	Test Layer	Test Condition	DUT Type
	Avg	0.000	50.00 %																		
	StdDev	0.000	0.000 %																		
	Range	0.000	0.000 %																		
	Min	0.000	50.00 %																		
	Max	0.000	50.00 %																		
	Sum	0.000	100.0 %																		
✓	Trial 1 (Worst)	0.000	50.0%	256000	32.7600 ps	33.5000 ps	397.440 mV	422.410 mV	819.850 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	590.040 mV	337.601 ps	140.000 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source
✓	Trial 2	0.000	50.0%	256000	40.7000 ps	39.4700 ps	396.092 mV	418.110 mV	814.202 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	702.730 mV	576.574 ps	142.500 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source

Trial 1



Trial 2



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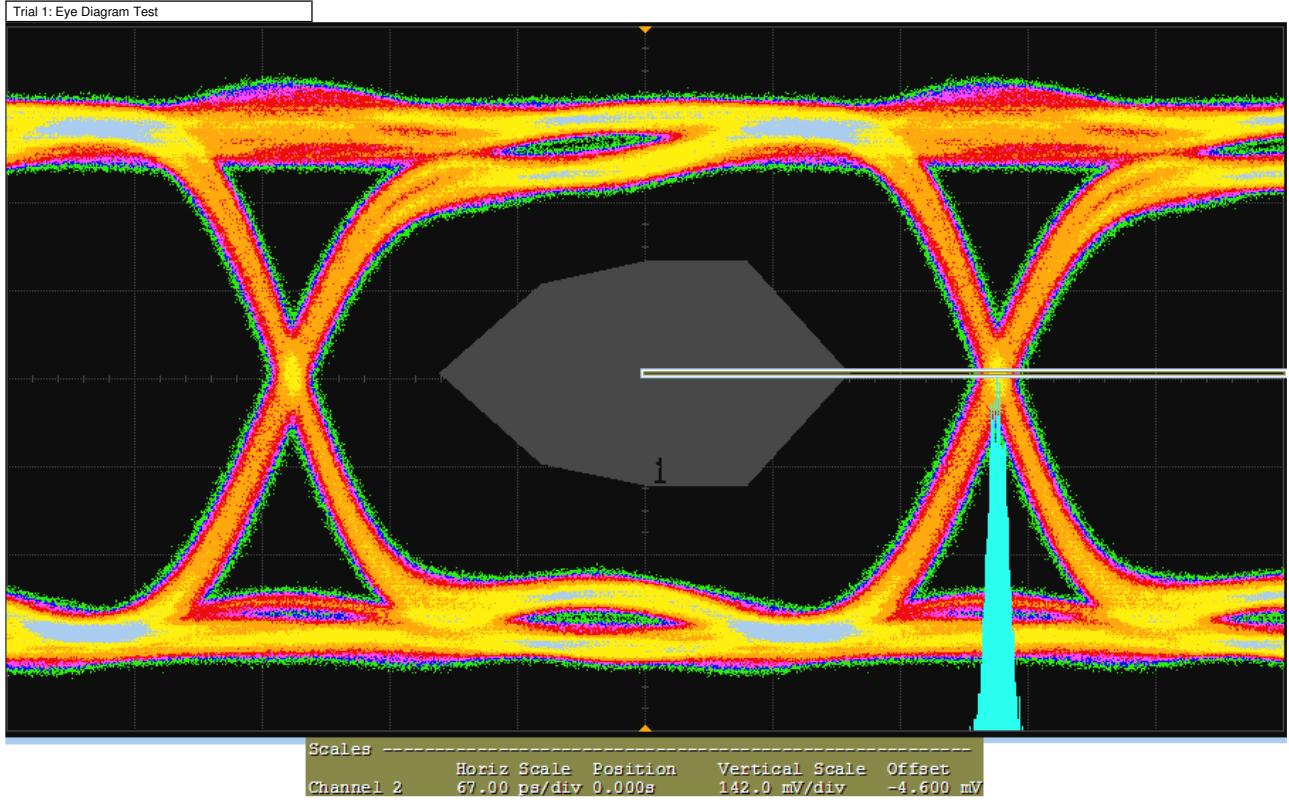
✓ Lane 1 - Eye Diagram Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (Worst of 2 Trials) 0.000 # Trials Run: 2 Worst Trial: Trial 1

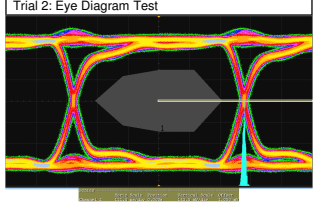
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Number of UI	Left Jitter	Right Jitter	VTop	VBase	VSwing	Mask Scalling Type	Mask Scalling Option	Mask Movement Option	Mask Movement Margin (Horizontal)	Mask Movement Margin (Vertical)	Measured Eye Height	Measured Eye Width	Vertical Scale	Test Mode	Test Layer	Test Condition	DUT Type
	Avg	0.000	50.00 %																		
	StdDev	0.000	0.000 %																		
	Range	0.000	0.000 %																		
	Min	0.000	50.00 %																		
	Max	0.000	50.00 %																		
	Sum	0.000	100.0 %																		
✓	Trial 1 (Worst)	0.000	50.0%	256000	27.5400 ps	26.8000 ps	401.220 mV	418.548 mV	819.768 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	618.710 mV	342.821 ps	142.500 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source
✓	Trial 2	0.000	50.0%	256000	39.4700 ps	39.4700 ps	398.058 mV	416.513 mV	814.571 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	678.870 mV	577.806 ps	142.500 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source

Trial 1



Trial 2



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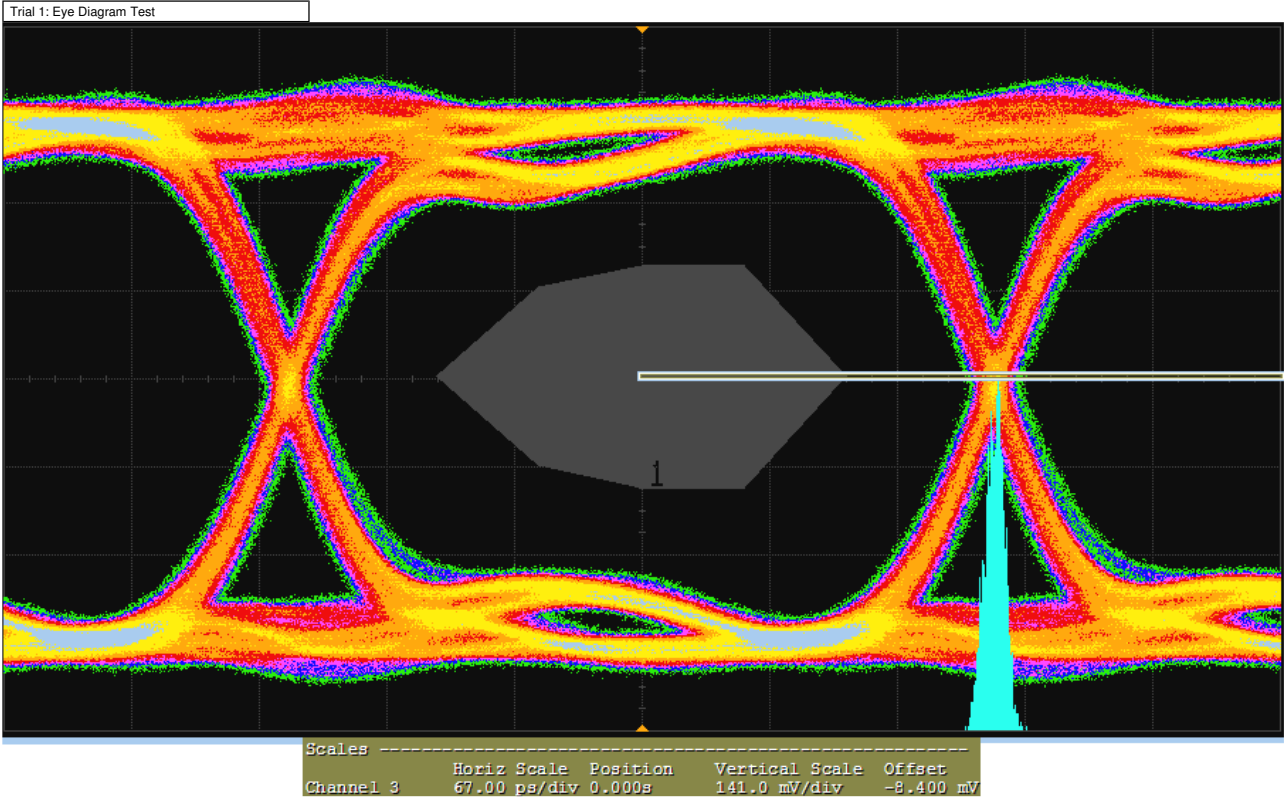
✓ Lane 2 - Eye Diagram Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (Worst of 2 Trials) 0.000 # Trials Run: 2 Worst Trial: Trial 1

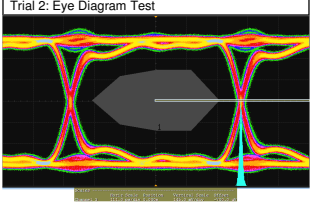
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Number of UI	Left Jitter	Right Jitter	VTop	VBase	VSwing	Mask Scalling Type	Mask Scalling Option	Mask Movement Option	Mask Movement Margin (Horizontal)	Mask Movement Margin (Vertical)	Measured Eye Height	Measured Eye Width	Vertical Scale	Test Mode	Test Layer	Test Condition	DUT Type
	Avg	0.000	50.00 %																		
	StdDev	0.000	0.000 %																		
	Range	0.000	0.000 %																		
	Min	0.000	50.00 %																		
	Max	0.000	50.00 %																		
	Sum	0.000	100.0 %																		
✓	Trial 1 (Worst)	0.000	50.0%	256000	32.0100 ps	32.0100 ps	401.228 mV	427.992 mV	829.219 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	632.130 mV	338.350 ps	141.250 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source
✓	Trial 2	0.000	50.0%	256000	40.7000 ps	40.7000 ps	398.274 mV	416.661 mV	814.935 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	686.450 mV	576.572 ps	145.000 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source

Trial 1



Trial 2



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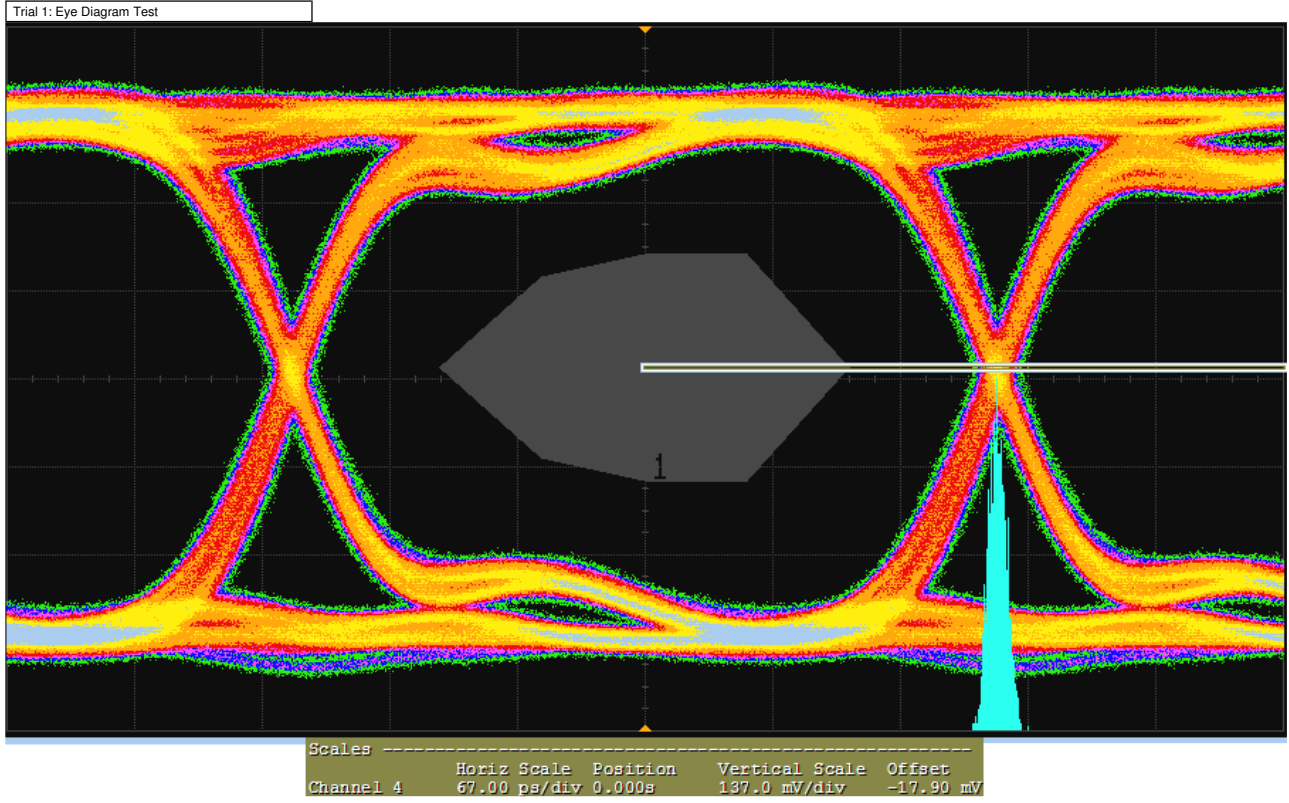
✓ Lane 3 - Eye Diagram Test Reference: DisplayPort CTS Sec. 3.1

Test Summary: Pass Test Description: To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.  
 Pass Limits: [-500 m to 500 m] Eye Diagram Test (Worst of 2 Trials) 0.000 # Trials Run: 2 Worst Trial: Trial 1

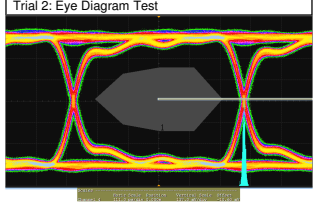
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Number of UI	Left Jitter	Right Jitter	VTop	VBase	VSwing	Mask Scalling Type	Mask Scalling Option	Mask Movement Option	Mask Movement Margin (Horizontal)	Mask Movement Margin (Vertical)	Measured Eye Height	Measured Eye Width	Vertical Scale	Test Mode	Test Layer	Test Condition	DUT Type
	Avg	0.000	50.00 %																		
	StdDev	0.000	0.000 %																		
	Range	0.000	0.000 %																		
	Min	0.000	50.00 %																		
	Max	0.000	50.00 %																		
	Sum	0.000	100.0 %																		
✓	Trial 1 (Worst)	0.000	50.0%	256000	29.0300 ps	28.2900 ps	395.694 mV	419.681 mV	815.375 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	673.420 mV	341.333 ps	137.500 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source
✓	Trial 2	0.000	50.0%	256000	33.3000 ps	33.3000 ps	395.436 mV	418.812 mV	814.248 mV	TP2	Absolute	Fixed	0.0000000000000000 s	0.000 V	672.160 mV	583.974 ps	137.500 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source

Trial 1



Trial 2



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✓ Lane 0 - Total Jitter Test (High BitRate) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

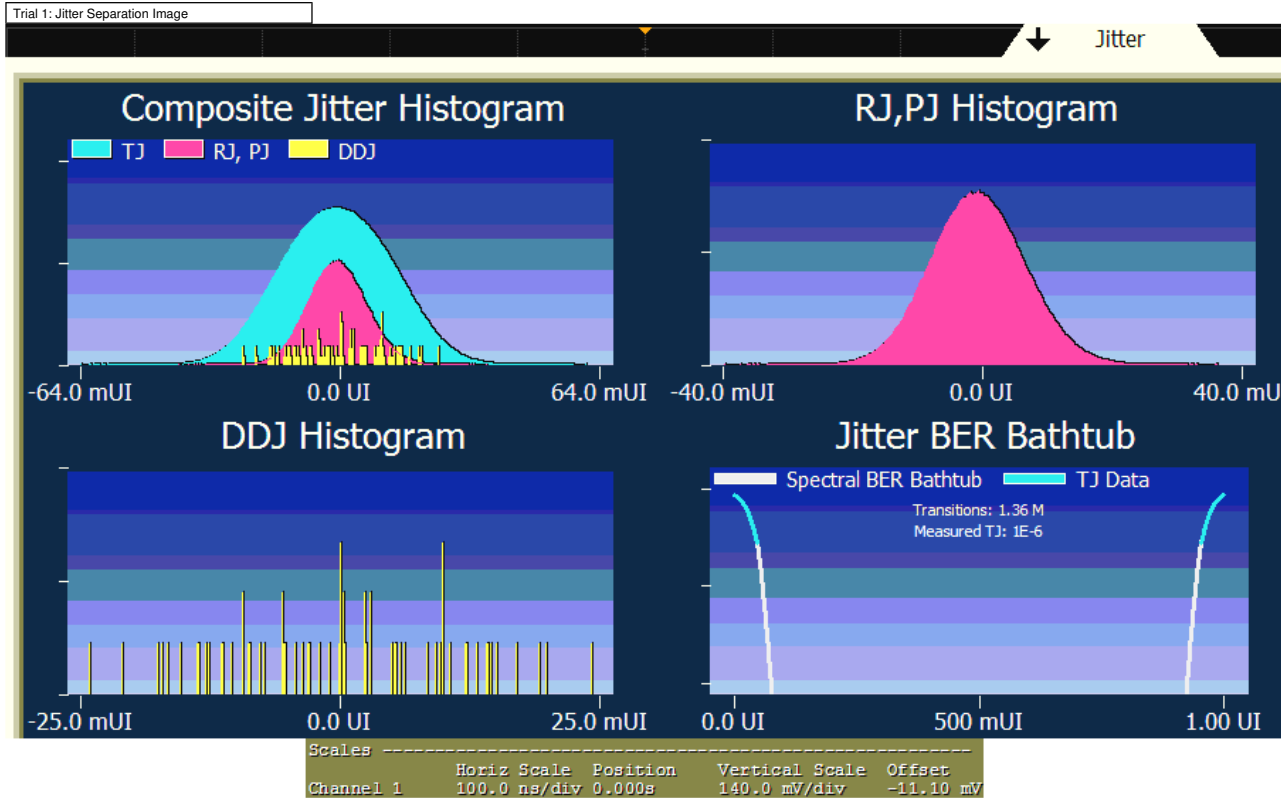
Test Summary: Pass Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

Pass Limits: <= 420.000 mUI Lane 0 Total Jitter Test (High BitRate) (Worst of 4 Trials) 118.700 mUI # Trials Run: 4 Worst Trial: Trial 2

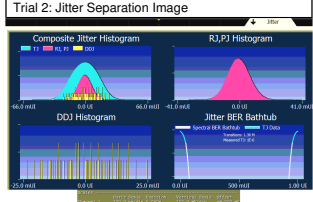
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	117.4 mUI	72.06 %																		
	StdDev	1.439 mUI	342.6 m%																		
	Range	3.000 mUI	714.3 m%																		
	Min	115.7 mUI	71.74 %																		
	Max	118.7 mUI	72.45 %																		
	Sum	469.4 mUI	288.2 %																		
✓	Trial 1	118.400 mUI	71.8%	(See image)	M	118.4	43.8508	3.7 mUI	10.0 mUI	45.4 mUI	6.1 mUI	43.5 mUI	48.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 2 (Worst)	118.700 mUI	71.7%	(See image)	M	118.7	43.9630	3.8 mUI	10.7 mUI	45.4 mUI	6.1 mUI	40.5 mUI	48.3 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 3	116.600 mUI	72.2%	(See image)	M	116.6	43.1852	3.8 mUI	10.3 mUI	43.2 mUI	6.1 mUI	39.6 mUI	45.4 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 4	115.700 mUI	72.5%	(See image)	M	115.7	42.8519	3.8 mUI	11.0 mUI	44.5 mUI	5.9 mUI	44.7 mUI	45.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps

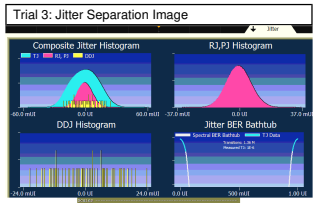
Trial 1



Trial 2



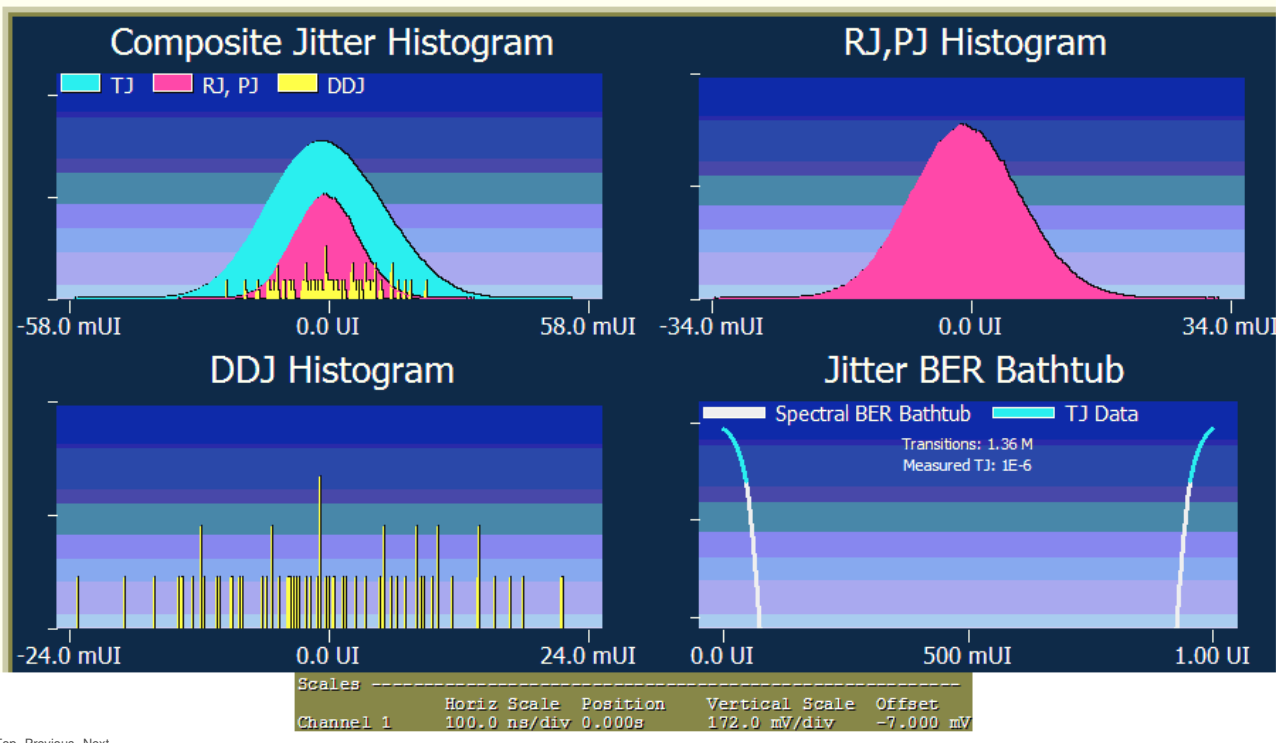
Trial 3



Trial 4

Trial 4: Jitter Separation Image

Jitter



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✓ Lane 1 - Total Jitter Test (High BitRate) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

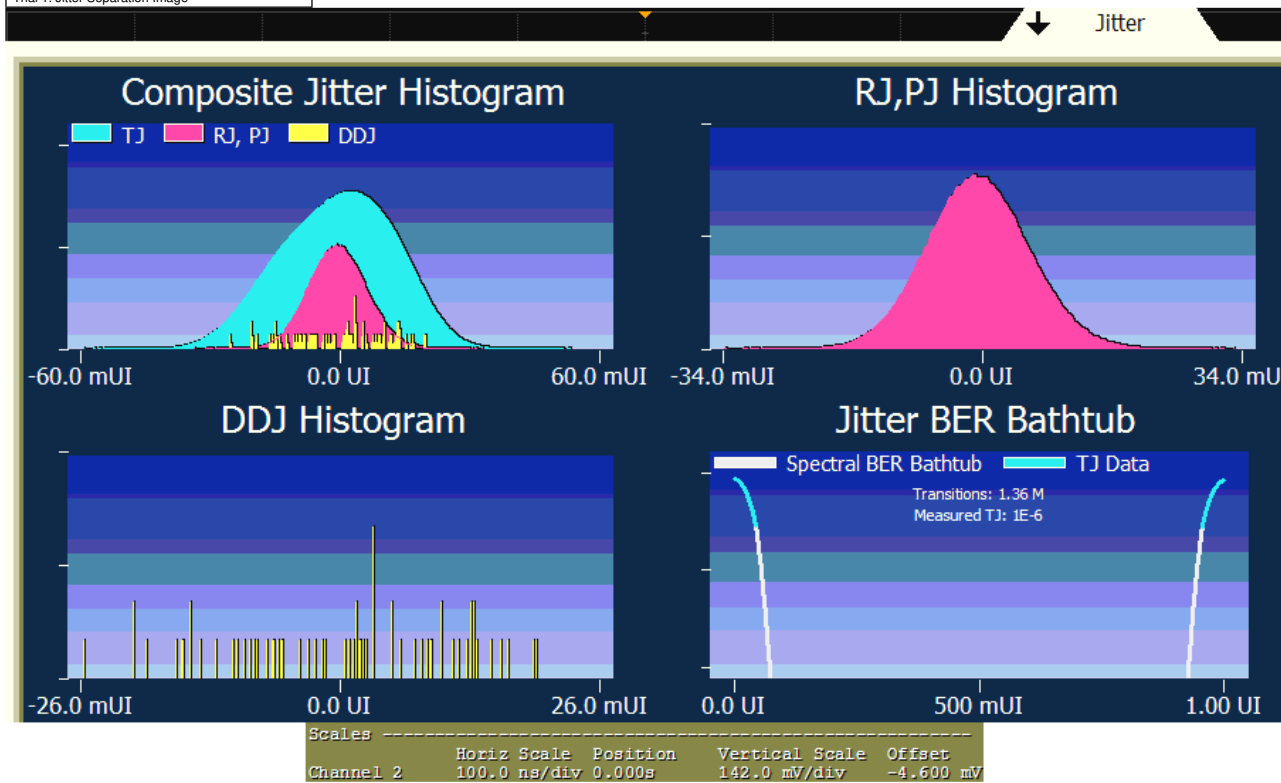
Pass Limits: <= 420.000 mUI Lane 1 Total Jitter Test (High BitRate) (Worst of 4 Trials) 114.100 mUI # Trials Run: 4 Worst Trial: Trial 3

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	113.7 mUI	72.93 %																		
	StdDev	287.2 μUI	68.39 m%																		
	Range	600.0 μUI	142.9 m%																		
	Min	113.5 mUI	72.83 %																		
	Max	114.1 mUI	72.98 %																		
	Sum	454.7 mUI	291.7 %																		
✓	Trial 1	113.500 mUI	73.0%	(See image)	1.00000000 M	113.5 mUI	42.0360 ps	2.7 mUI	7.1 mUI	40.9 mUI	6.0 mUI	45.0 mUI	45.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 2	113.600 mUI	73.0%	(See image)	1.00000000 M	113.6 mUI	42.0732 ps	3.0 mUI	8.5 mUI	41.1 mUI	6.0 mUI	43.8 mUI	45.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 3 (Worst)	114.100 mUI	72.8%	(See image)	1.00000000 M	114.1 mUI	42.2583 ps	2.7 mUI	6.9 mUI	39.0 mUI	6.3 mUI	43.9 mUI	43.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 4	113.500 mUI	73.0%	(See image)	1.00000000 M	113.5 mUI	42.0361 ps	2.8 mUI	8.2 mUI	41.9 mUI	6.0 mUI	45.5 mUI	45.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps

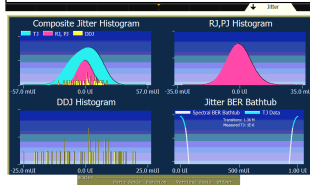
Trial 1

Trial 1: Jitter Separation Image



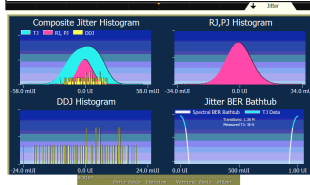
Trial 2

Trial 2: Jitter Separation Image



Trial 3

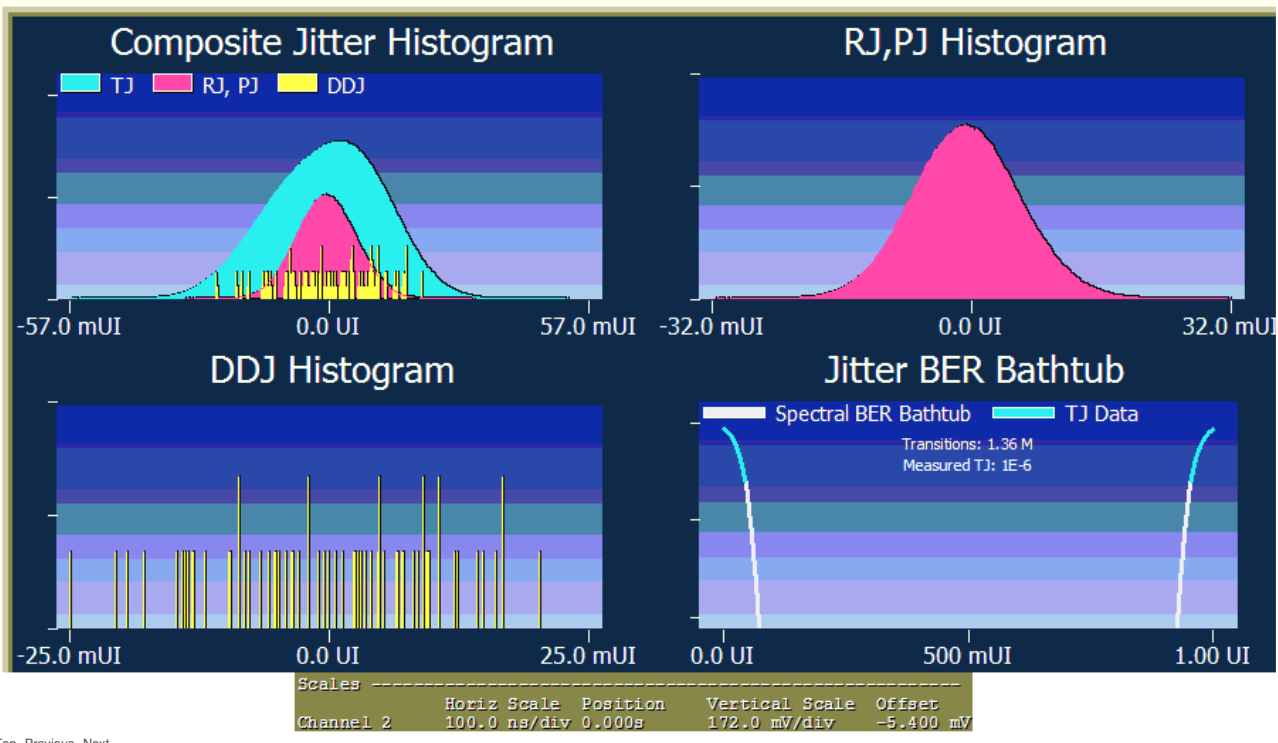
Trial 3: Jitter Separation Image



Trial 4

Trial 4: Jitter Separation Image

Jitter



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**✓ Lane 2 - Total Jitter Test (High BitRate)** Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

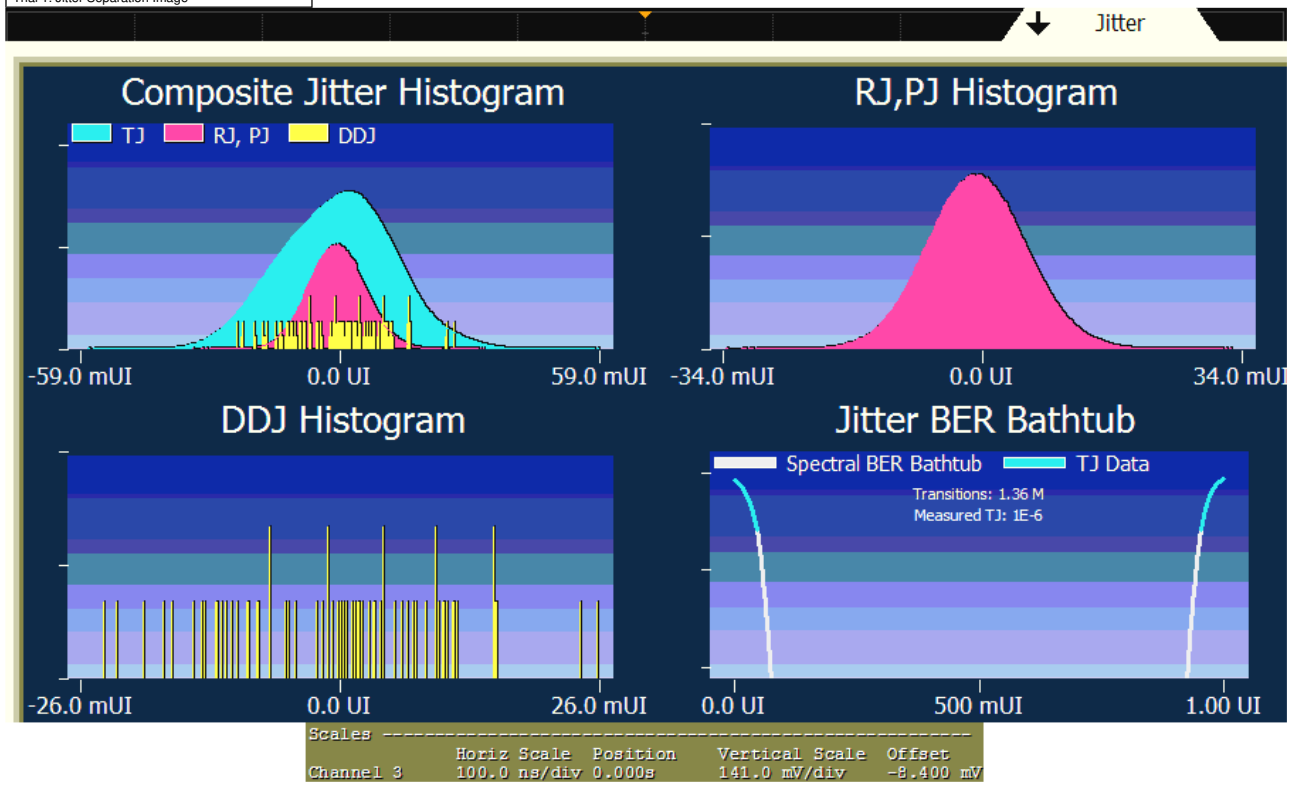
**Pass Limits:** <= 420.000 mUI | **Lane 2 Total Jitter Test (High BitRate) (Worst of 4 Trials)** 122.700 mUI | **# Trials Run:** 4 | **Worst Trial:** Trial 3

**Overall Summary + details of 4 worst trials**

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	<b>Avg</b>	117.6 mUI	72.01 %			117.0	43.3321	2.4 mUI	7.8 mUI	45.2 mUI	6.0 mUI	47.9 mUI	49.8 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
	<b>StdDev</b>	4.019 mUI	956.8 m%			117.6	43.5547	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
	<b>Range</b>	9.800 mUI	2.333 %			117.6	43.5547	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
	<b>Min</b>	112.9 mUI	70.79 %			112.9	43.5547	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
	<b>Max</b>	122.7 mUI	73.12 %			122.7	43.5547	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
	<b>Sum</b>	470.2 mUI	288.0 %			470.2	43.5547	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 1	117.000 mUI	72.1%	(See image)	1.00000000 M	117.0	43.3321	2.4 mUI	7.8 mUI	45.2 mUI	6.0 mUI	47.9 mUI	49.8 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 2	117.600 mUI	72.0%	(See image)	1.00000000 M	117.6	43.5547	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 3 (Worst)	122.700 mUI	70.8%	(See image)	1.00000000 M	122.7	45.4436	2.3 mUI	6.8 mUI	49.0 mUI	6.1 mUI	53.2 mUI	54.2 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 4	112.900 mUI	73.1%	(See image)	1.00000000 M	112.9	41.8140	2.5 mUI	7.4 mUI	42.2 mUI	5.9 mUI	44.5 mUI	45.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps

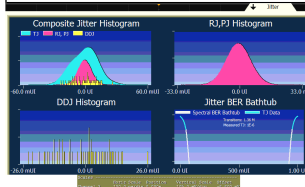
**Trial 1**

Trial 1: Jitter Separation Image



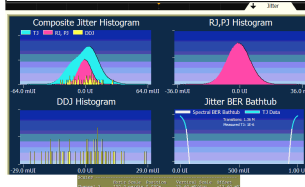
**Trial 2**

Trial 2: Jitter Separation Image



**Trial 3**

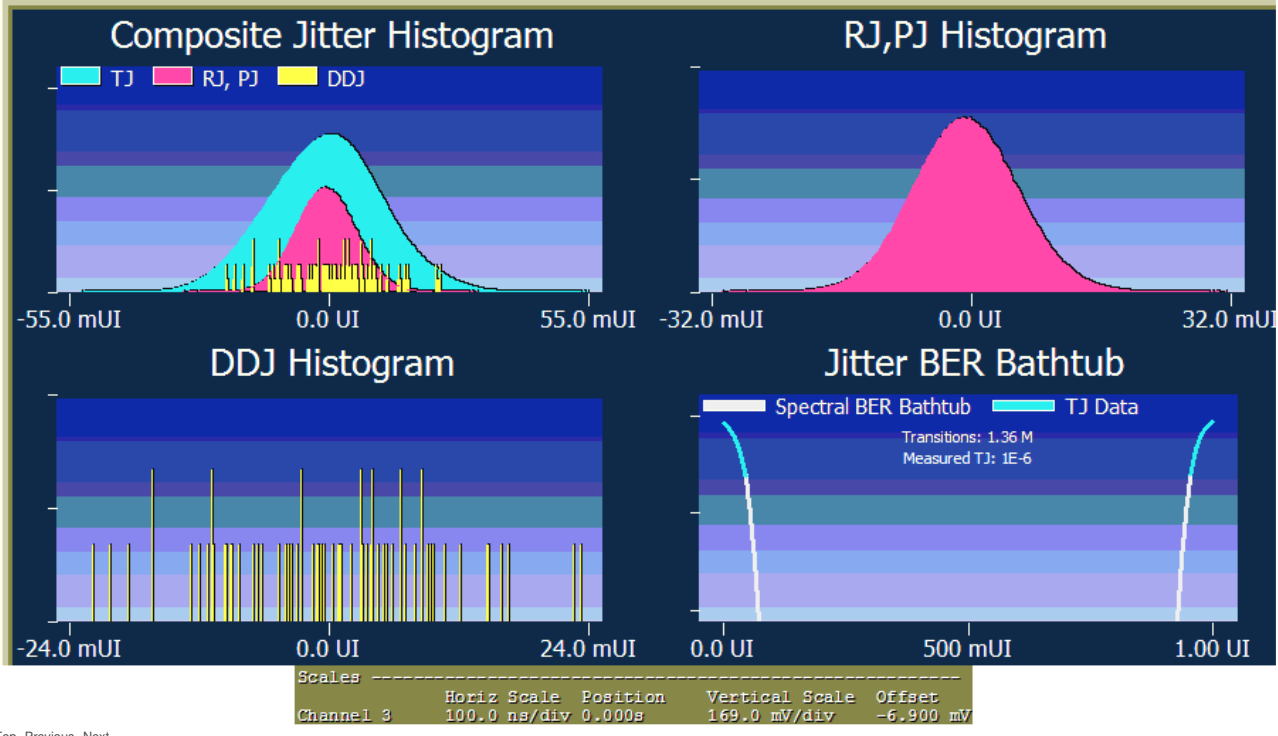
Trial 3: Jitter Separation Image



**Trial 4**

Trial 4: Jitter Separation Image

Jitter



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**✓ Lane 3 - Total Jitter Test (High BitRate)** Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

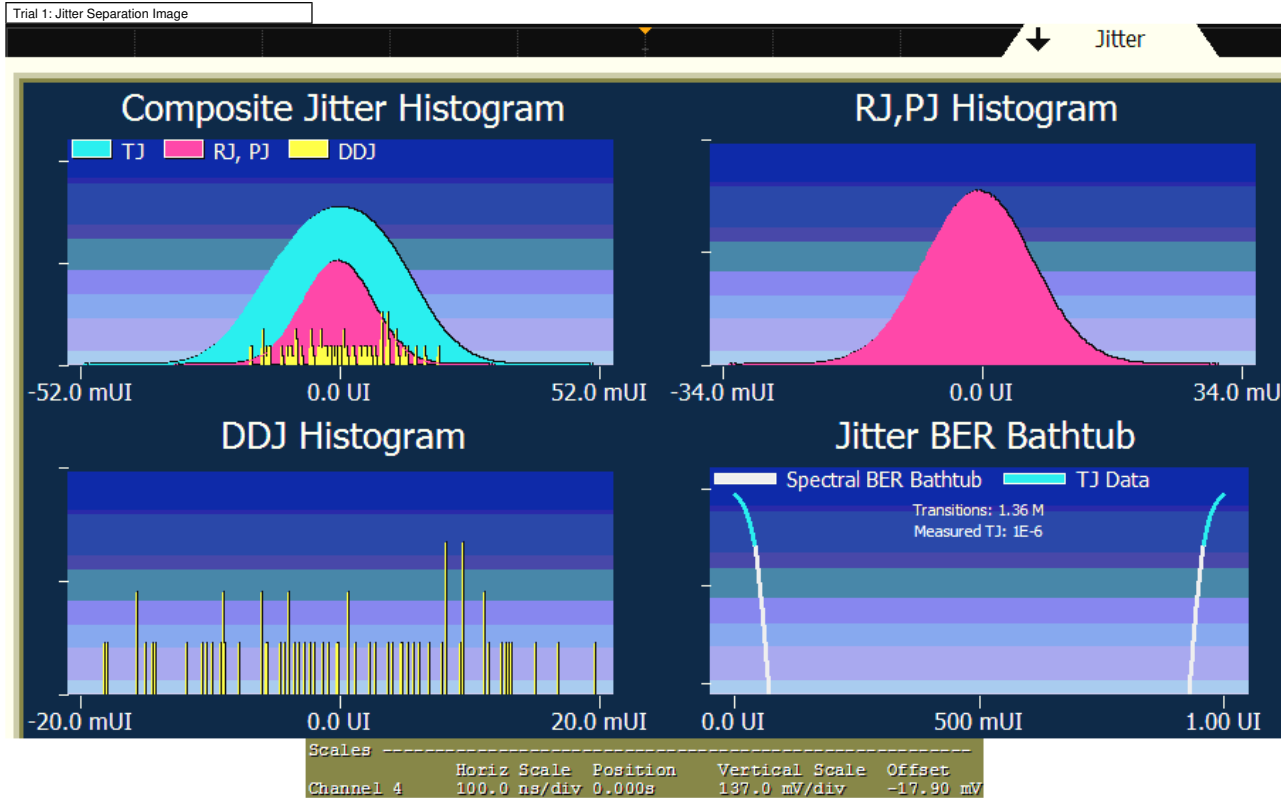
Test Summary: **Pass** Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

**Pass Limits:** <= 420.000 mUI | **Lane 3 Total Jitter Test (High BitRate) (Worst of 4 Trials)** 111.800 mUI | **# Trials Run:** 4 | **Worst Trial:** Trial 3

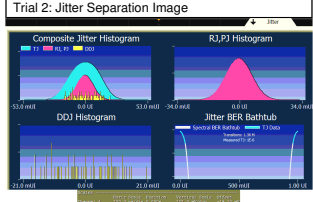
**Overall Summary + details of 4 worst trials**

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	<b>Avg</b>	109.4 mUI	73.95 %																		
	<b>StdDev</b>	1.782 mUI	424.3 m%																		
	<b>Range</b>	4.200 mUI	1.000 %																		
	<b>Min</b>	107.6 mUI	73.38 %																		
	<b>Max</b>	111.8 mUI	74.38 %																		
	<b>Sum</b>	437.7 mUI	295.8 %																		
✓	Trial 1	107.600 mUI	74.4%	(See image)	1.00000000 M	107.6 mUI	39.8510 ps	3.4 mUI	8.5 mUI	35.5 mUI	6.0 mUI	35.4 mUI	38.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 2	108.700 mUI	74.1%	(See image)	1.00000000 M	108.7 mUI	40.2582 ps	3.4 mUI	9.1 mUI	36.0 mUI	6.1 mUI	37.6 mUI	38.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 3 (Worst)	111.800 mUI	73.4%	(See image)	1.00000000 M	111.8 mUI	41.4063 ps	3.4 mUI	8.8 mUI	37.9 mUI	6.2 mUI	40.5 mUI	40.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps
✓	Trial 4	109.600 mUI	73.9%	(See image)	1.00000000 M	109.6 mUI	40.5915 ps	3.7 mUI	10.4 mUI	38.1 mUI	6.0 mUI	36.3 mUI	39.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps

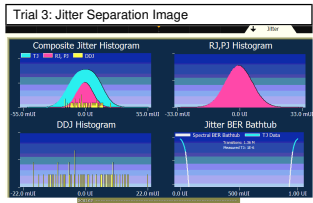
**Trial 1**



**Trial 2**



**Trial 3**

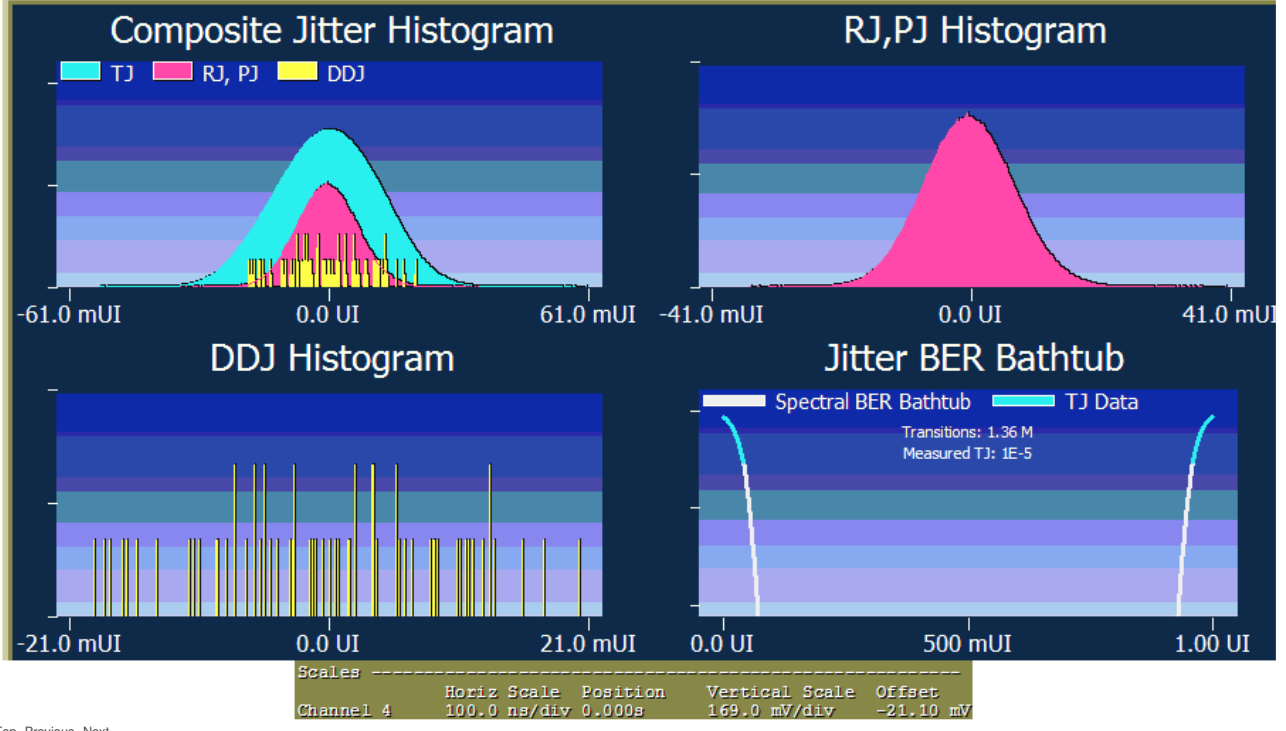


**Trial 4**



Trial 4: Jitter Separation Image

Jitter



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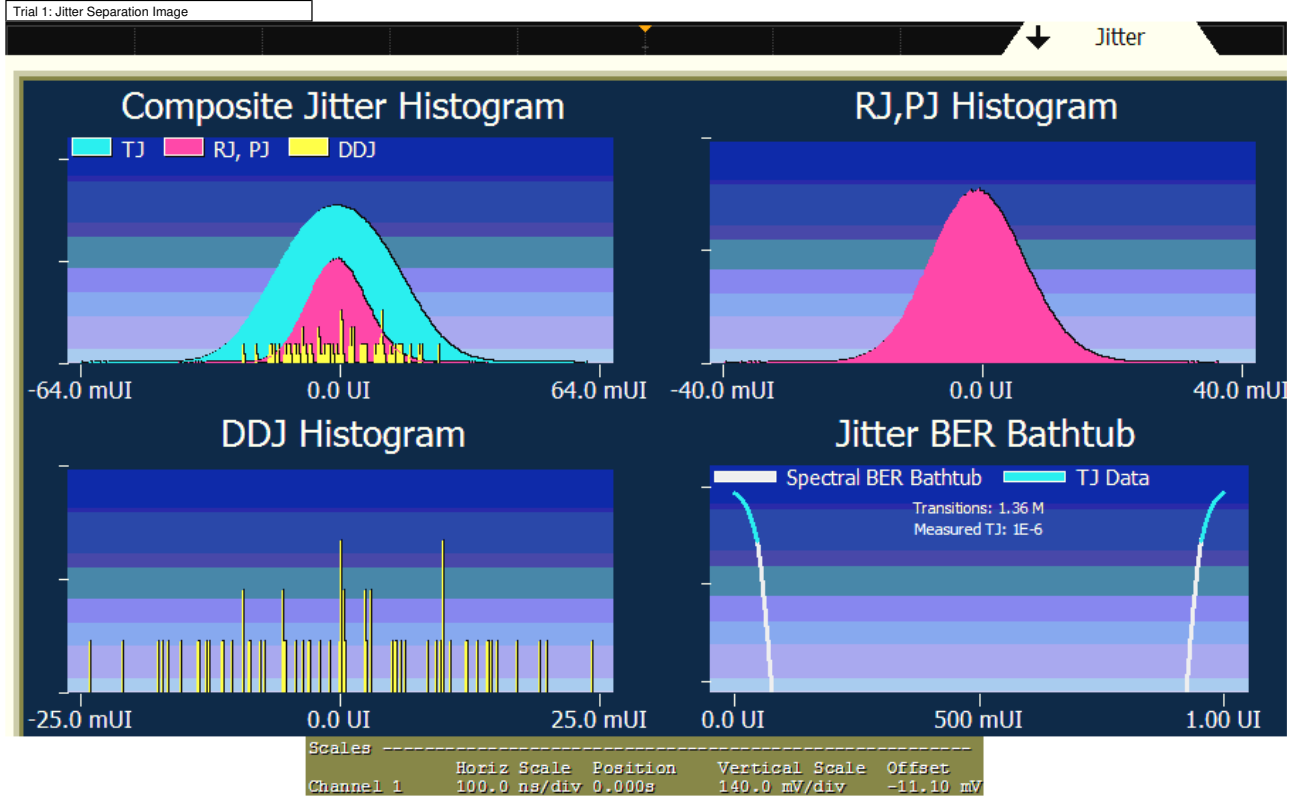
✓ Lane 0 - Non-ISI Jitter Test (High BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 276.0000 mUI Lane 0 Non ISI Jitter Test (High BitRate) (Worst of 4 Trials) 78.2000 mUI # Trials Run: 4 Worst Trial: Trial 2

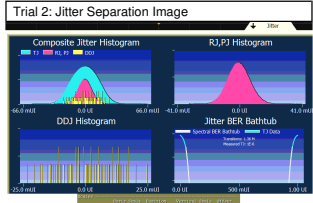
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ) mUI	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	75.28 mUI	72.73 %																			
	StdDev	3.160 mUI	1.145 %																			
	Range	7.200 mUI	2.609 %																			
	Min	71.00 mUI	71.67 %																			
	Max	78.20 mUI	74.28 %																			
	Sum	301.1 mUI	290.9 %																			
✓	Trial 1	74.9000 mUI	72.9%	(See image)	1.00000000 M	27.7401 ps	118.4 mUI	3.7 mUI	10.0 mUI	45.4 mUI	6.1 mUI	43.5 mUI	48.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 2 (Worst)	78.2000 mUI	71.7%	(See image)	1.00000000 M	28.9630 ps	118.7 mUI	3.8 mUI	10.7 mUI	45.4 mUI	6.1 mUI	40.5 mUI	48.3 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 3	77.0000 mUI	72.1%	(See image)	1.00000000 M	28.5185 ps	116.6 mUI	3.8 mUI	10.3 mUI	43.2 mUI	6.1 mUI	39.6 mUI	45.4 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 4	71.0000 mUI	74.3%	(See image)	1.00000000 M	26.2963 ps	115.7 mUI	3.8 mUI	11.0 mUI	44.5 mUI	5.9 mUI	44.7 mUI	45.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	

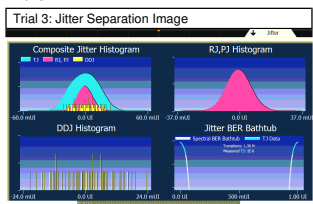
Trial 1



Trial 2



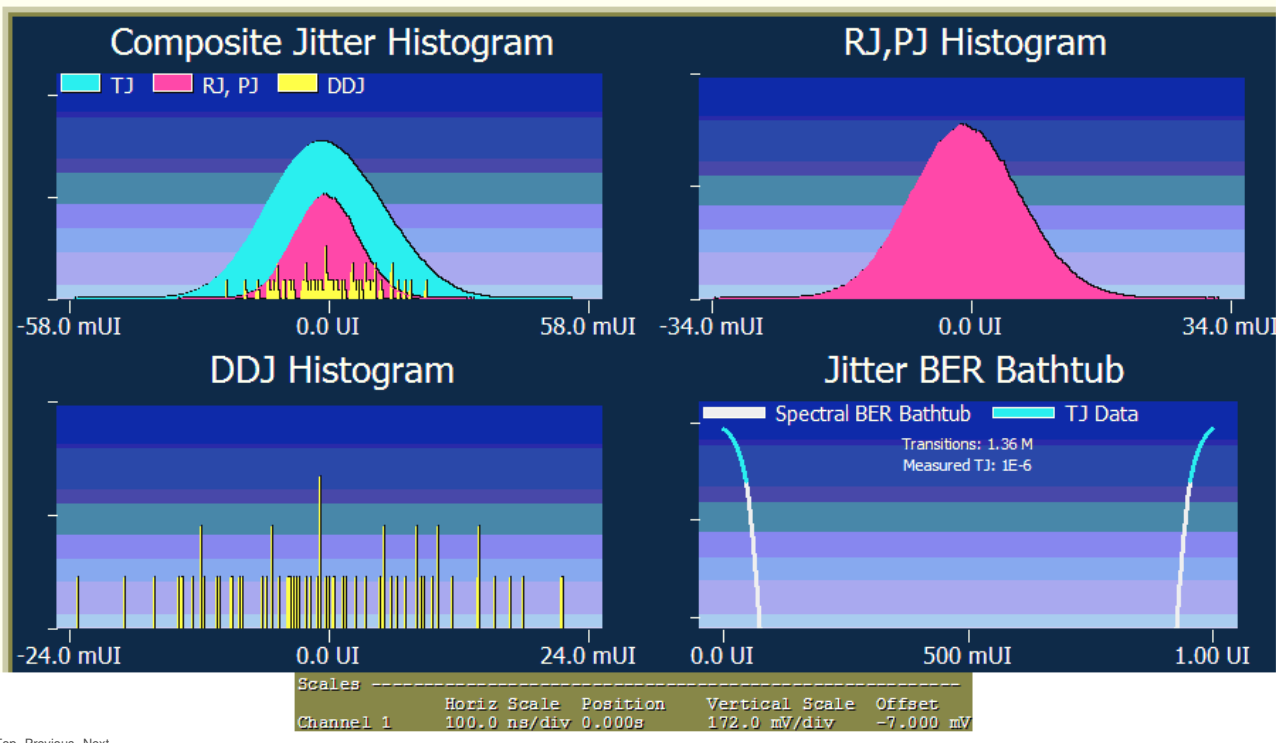
Trial 3



Trial 4

Trial 4: Jitter Separation Image

Jitter



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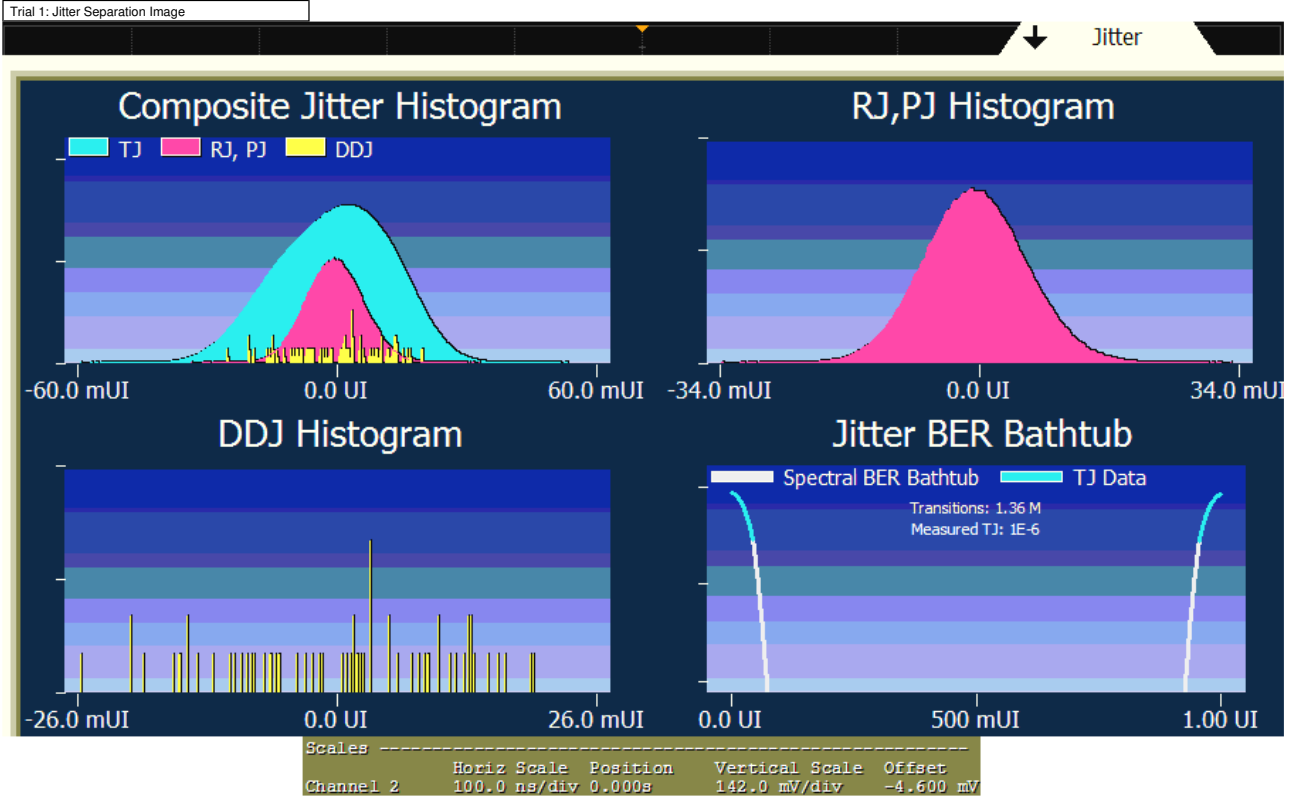
✓ Lane 1 - Non-ISI Jitter Test (High BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 276.0000 mUI | Lane 1 Non ISI Jitter Test (High BitRate) (Worst of 4 Trials) 70.2000 mUI | # Trials Run: 4 | Worst Trial: Trial 3

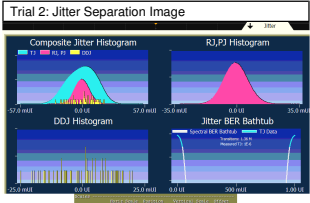
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ) mUI	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	69.13 mUI	74.95 %																			
	StdDev	1.044 mUI	378.1 m%																			
	Range	2.200 mUI	797.1 m%																			
	Min	68.00 mUI	74.57 %																			
	Max	70.20 mUI	75.36 %																			
	Sum	276.5 mUI	299.8 %																			
✓	Trial 1	68.5000 mUI	75.2%	(See image)	1.00000000 M	25.3698 ps	113.5 mUI	2.7 mUI	7.1 mUI	40.9 mUI	6.0 mUI	45.0 mUI	45.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 2	69.8000 mUI	74.7%	(See image)	1.00000000 M	25.8513 ps	113.6 mUI	3.0 mUI	8.5 mUI	41.1 mUI	6.0 mUI	43.8 mUI	45.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 3 (Worst)	70.2000 mUI	74.6%	(See image)	1.00000000 M	25.9994 ps	114.1 mUI	2.7 mUI	6.9 mUI	39.0 mUI	6.3 mUI	43.9 mUI	43.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 4	68.0000 mUI	75.4%	(See image)	1.00000000 M	25.1846 ps	113.5 mUI	2.8 mUI	8.2 mUI	41.9 mUI	6.0 mUI	45.5 mUI	45.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	

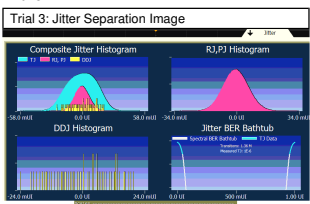
Trial 1



Trial 2



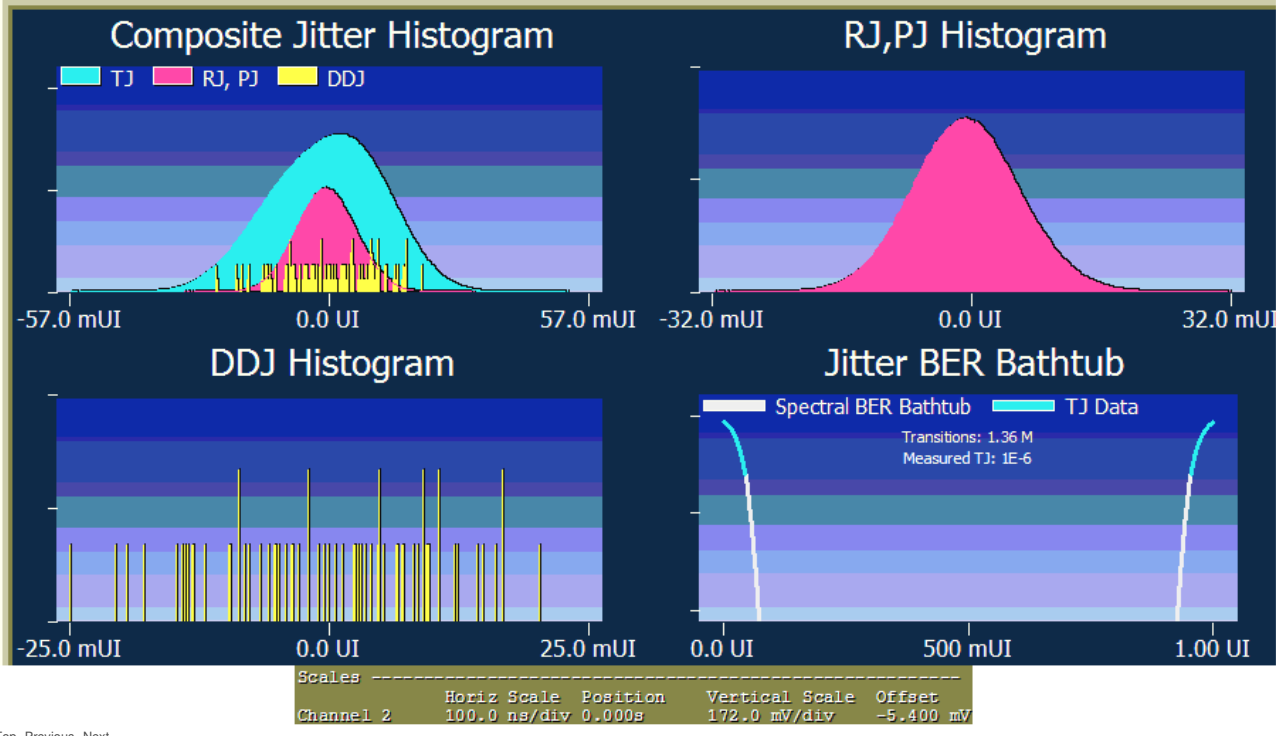
Trial 3



Trial 4

Trial 4: Jitter Separation Image

Jitter



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✓ Lane 2 - Non-ISI Jitter Test (High BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

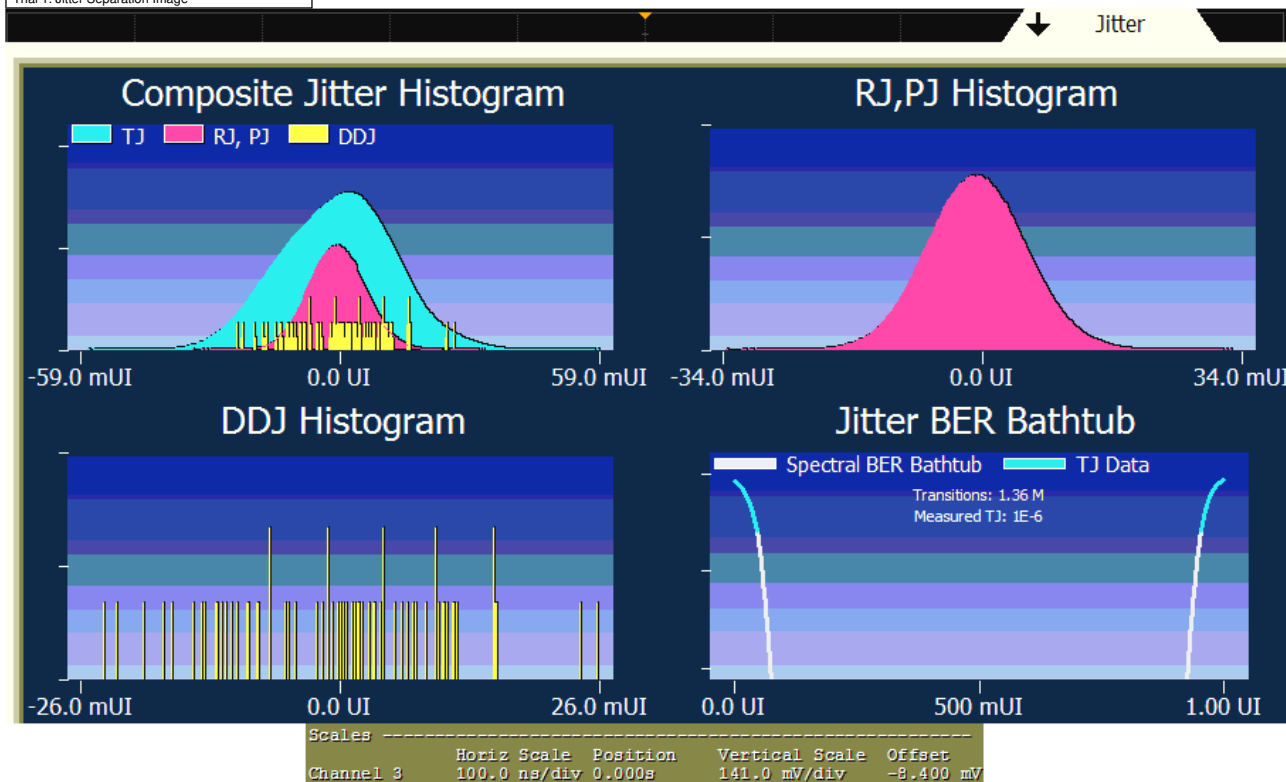
Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 276.0000 mUI Lane 2 Non ISI Jitter Test (High BitRate) (Worst of 4 Trials) 69.5000 mUI # Trials Run: 4 Worst Trial: Trial 3

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ) mUI	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	68.75 mUI	75.09 %																			
	StdDev	675.8 μUI	244.8 m%																			
	Range	1.500 mUI	543.5 m%																			
	Min	68.00 mUI	74.82 %																			
	Max	69.50 mUI	75.36 %																			
	Sum	275.0 mUI	300.4 %																			
✓	Trial 1	69.1000 mUI	75.0%	(See image)	1.00000000 M	25.5919 ps	117.0 mUI	2.4 mUI	7.8 mUI	45.2 mUI	6.0 mUI	47.9 mUI	49.8 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 2	68.0000 mUI	75.4%	(See image)	1.00000000 M	25.1847 ps	117.6 mUI	2.5 mUI	6.4 mUI	45.8 mUI	6.0 mUI	49.6 mUI	50.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 3 (Worst)	69.5000 mUI	74.8%	(See image)	1.00000000 M	25.7403 ps	122.7 mUI	2.3 mUI	6.8 mUI	49.0 mUI	6.1 mUI	53.2 mUI	54.2 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 4	68.4000 mUI	75.2%	(See image)	1.00000000 M	25.3329 ps	112.9 mUI	2.5 mUI	7.4 mUI	42.2 mUI	5.9 mUI	44.5 mUI	45.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	

Trial 1

Trial 1: Jitter Separation Image



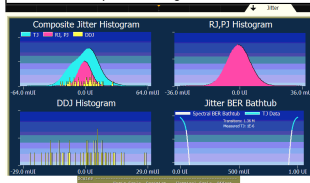
Trial 2

Trial 2: Jitter Separation Image



Trial 3

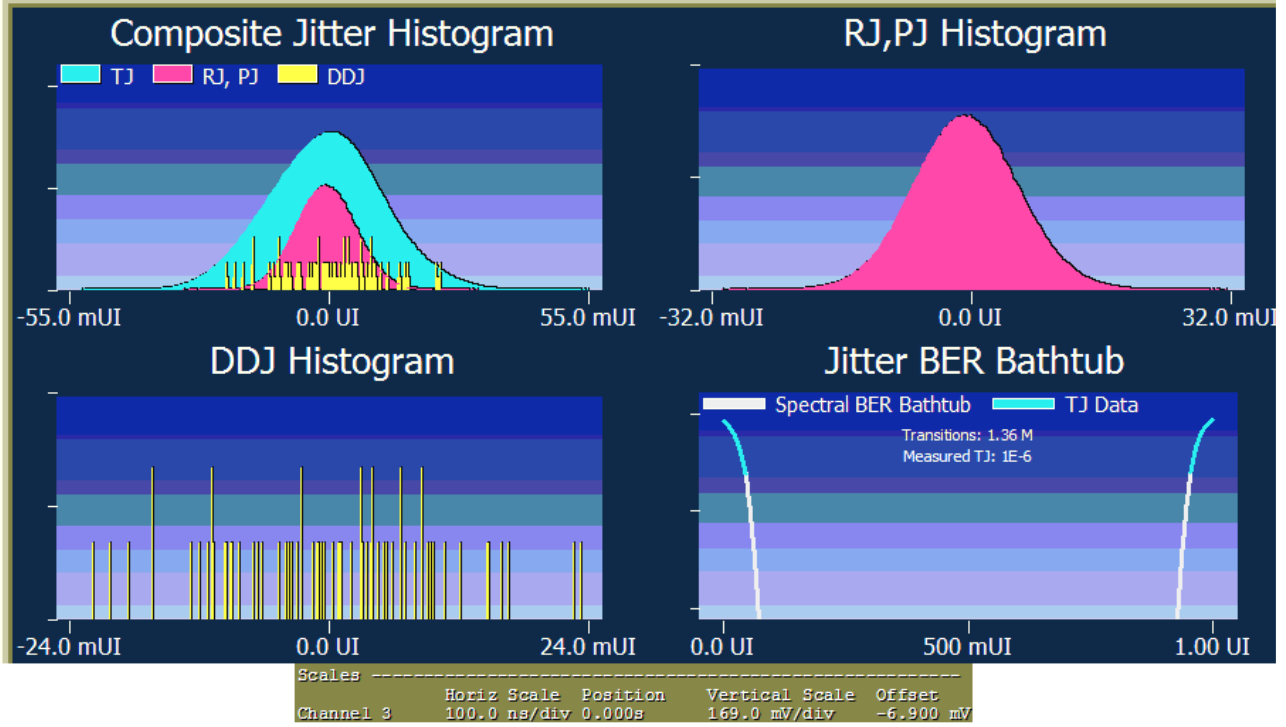
Trial 3: Jitter Separation Image



Trial 4

Trial 4: Jitter Separation Image

Jitter



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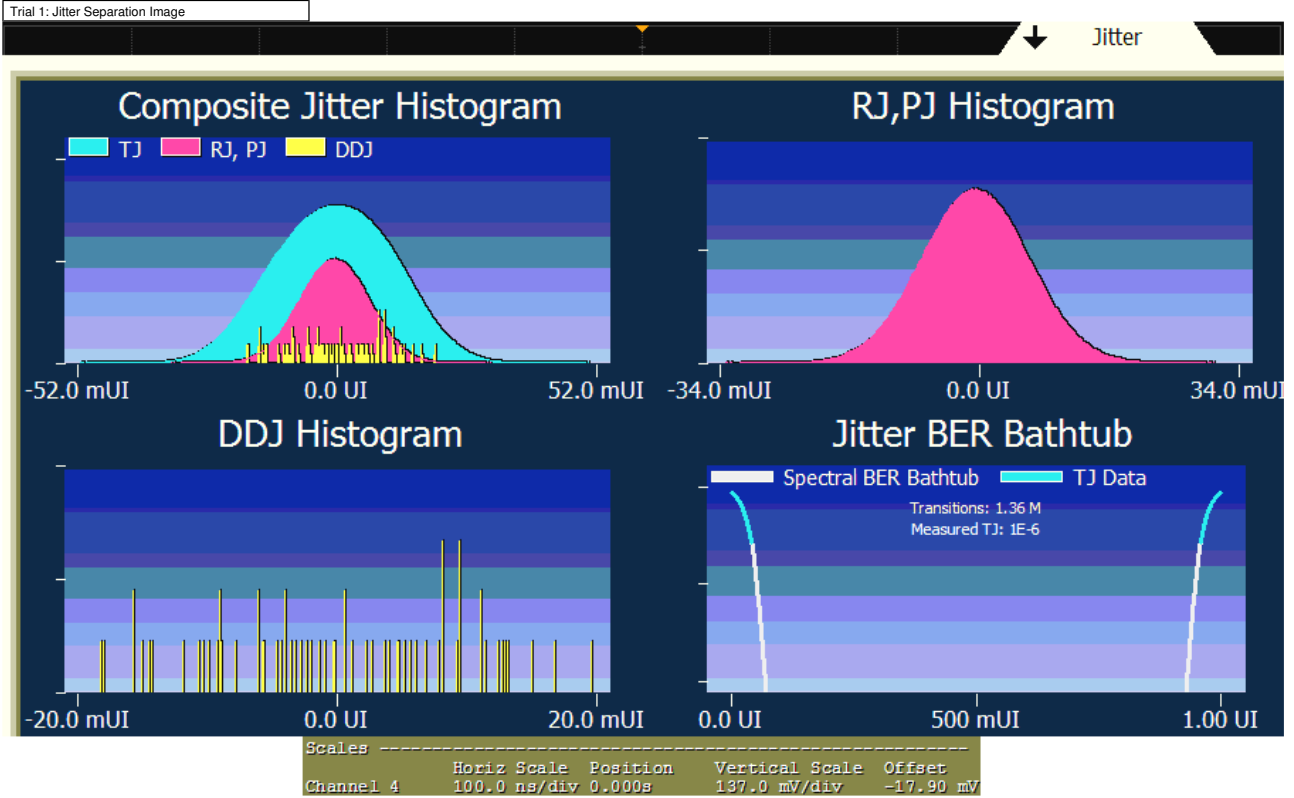
✓ Lane 3 - Non-ISI Jitter Test (High BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 276.0000 mUI Lane 3 Non ISI Jitter Test (High BitRate) (Worst of 4 Trials) 73.3000 mUI # Trials Run: 4 Worst Trial: Trial 4

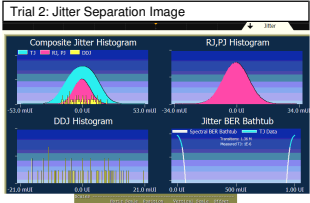
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ)	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	71.98 mUI	73.92 %																			
	StdDev	1.005 mUI	364.0 m%																			
	Range	2.200 mUI	797.1 m%																			
	Min	71.10 mUI	73.44 %																			
	Max	73.30 mUI	74.24 %																			
	Sum	287.9 mUI	295.7 %																			
✓	Trial 1	72.2000 mUI	73.8%	(See image)	1.00000000 M	26.7402 ps	107.6 mUI	3.4 mUI	8.5 mUI	35.5 mUI	6.0 mUI	35.4 mUI	38.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 2	71.1000 mUI	74.2%	(See image)	1.00000000 M	26.3327 ps	108.7 mUI	3.4 mUI	9.1 mUI	36.0 mUI	6.1 mUI	37.6 mUI	38.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 3	71.3000 mUI	74.2%	(See image)	1.00000000 M	26.4067 ps	111.8 mUI	3.4 mUI	8.8 mUI	37.9 mUI	6.2 mUI	40.5 mUI	40.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	
✓	Trial 4 (Worst)	73.3000 mUI	73.4%	(See image)	1.00000000 M	27.1474 ps	109.6 mUI	3.7 mUI	10.4 mUI	38.1 mUI	6.0 mUI	36.3 mUI	39.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbps	

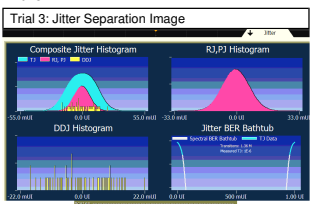
Trial 1



Trial 2



Trial 3

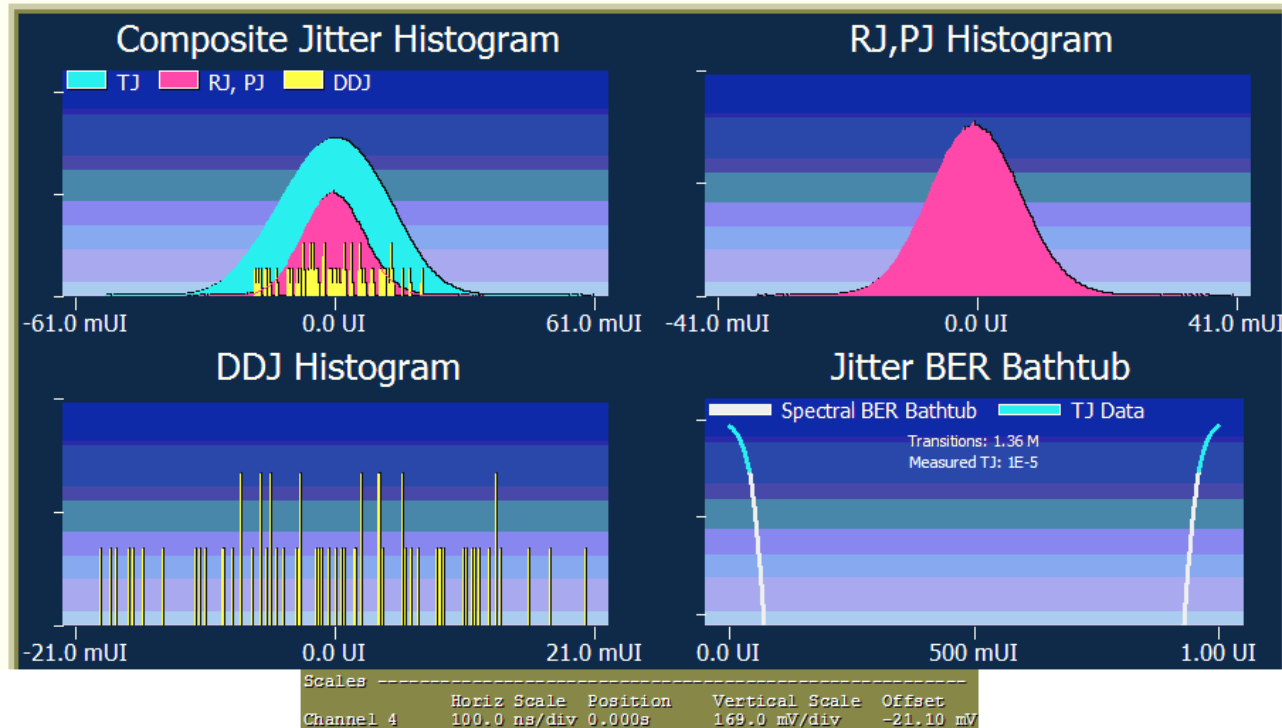


Trial 4



Trial 4: Jitter Separation Image

Jitter



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✓ Lane 0 - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

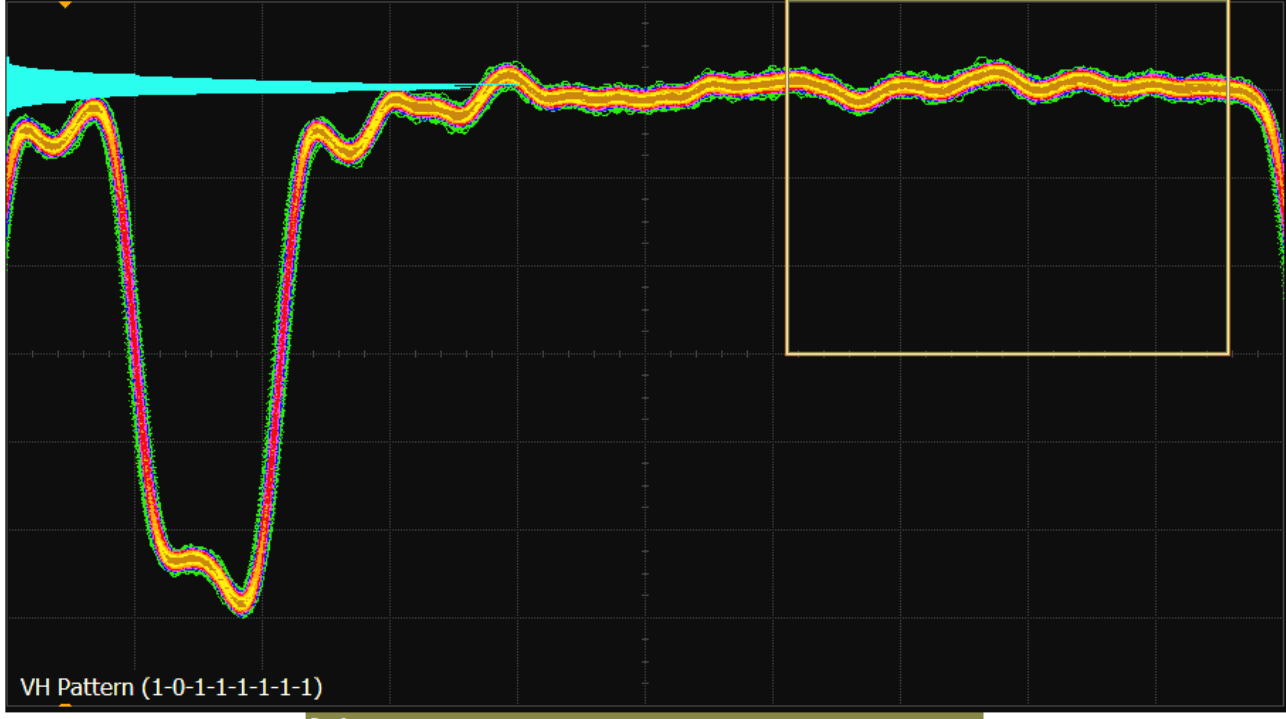
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
 Pass Limits: [100.0 mdB to 5.1000 dB] Lane 0 Non-PreEmphasis Level Test (Swing 2/Swing 1) (Worst of 2 Trials) 2.6131 dB # Trials Run: 2 Worst Trial: Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Level VH Image (Swing 1)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitF
	Avg	2.601 dB	49.76 %																				
	StdDev	17.16 mdB	28.28 m%																				
	Range	24.27 mdB	40.00 m%																				
	Min	2.589 dB	49.74 %																				
	Max	2.613 dB	49.78 %																				
	Sum	5.202 dB	99.52 %																				
✓	Trial 1	2.5889 dB	49.8%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	397.440 mV	422.410 mV	819.850 mV	291.842 mV	316.701 mV	608.543 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2 (Worst)	2.6131 dB	49.7%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	396.092 mV	418.110 mV	814.202 mV	290.671 mV	311.993 mV	602.664 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

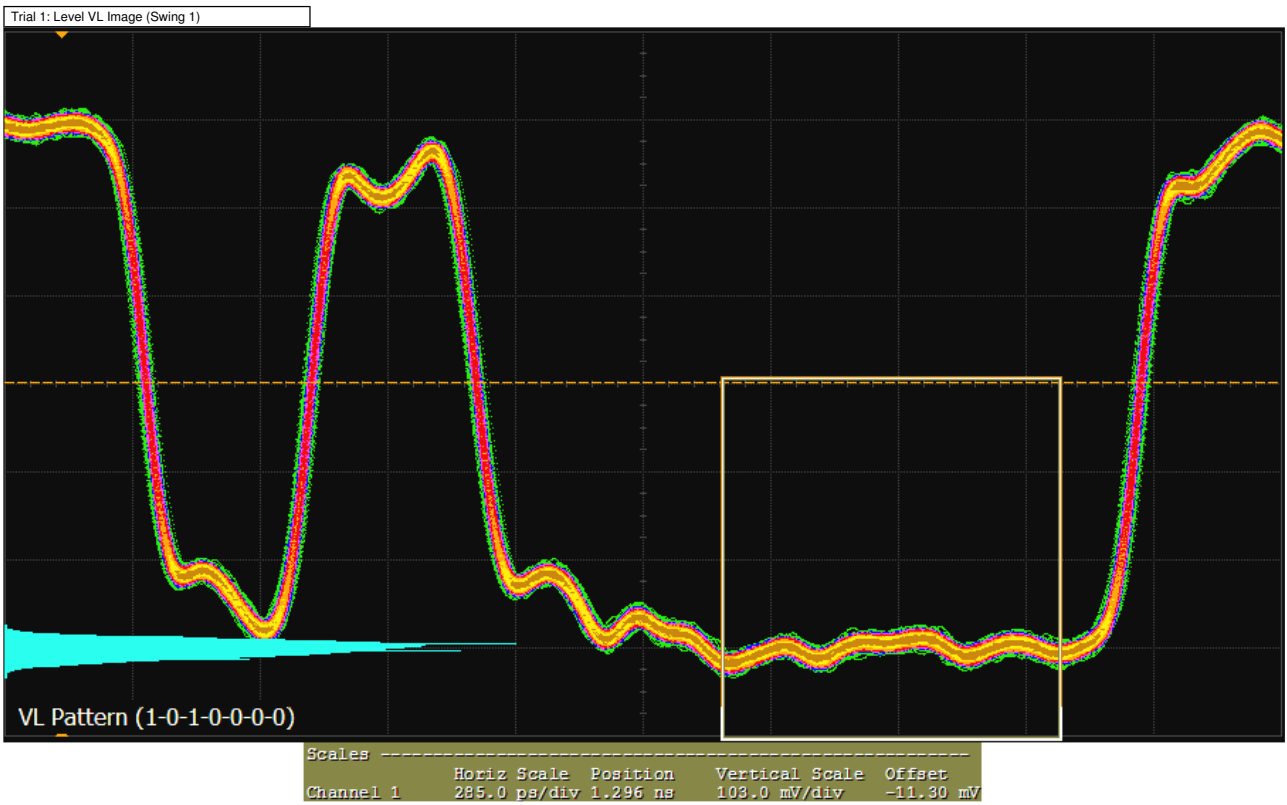
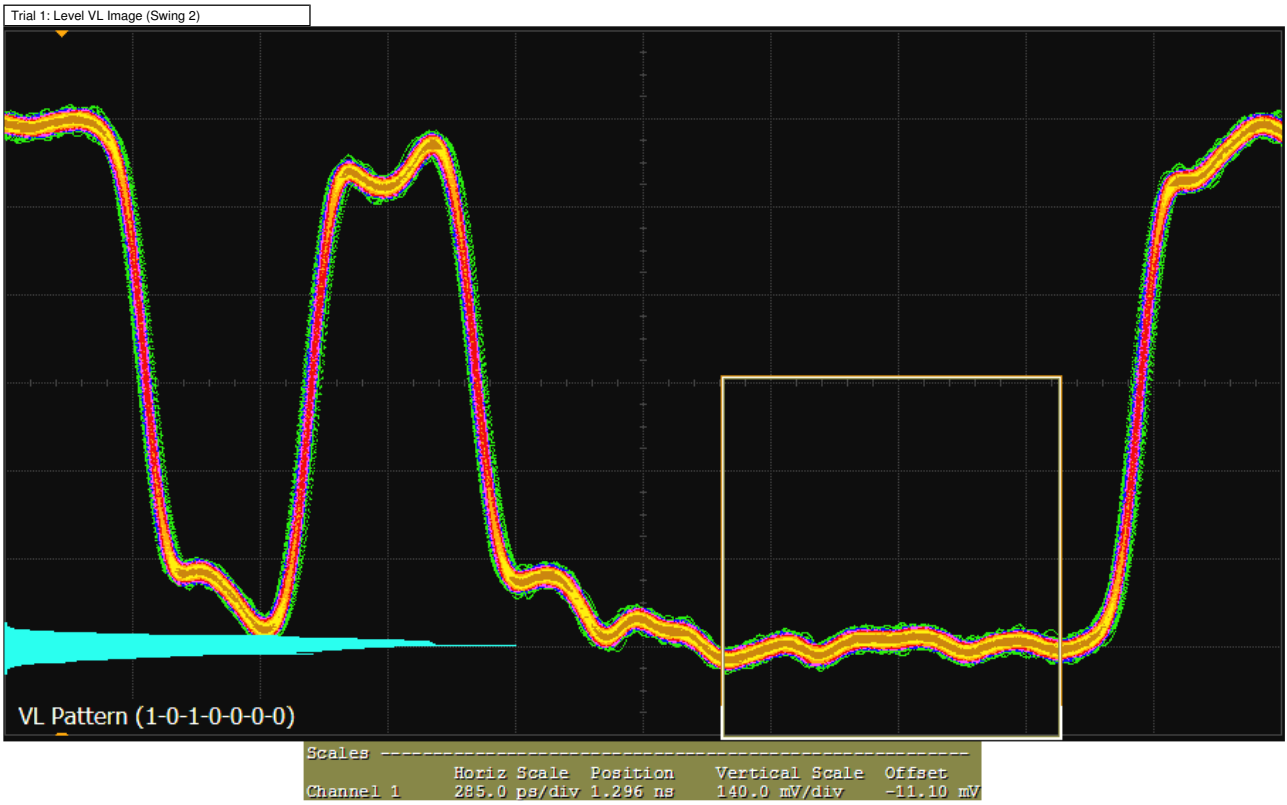
Trial 1

Trial 1: Level VH Image (Swing 2)

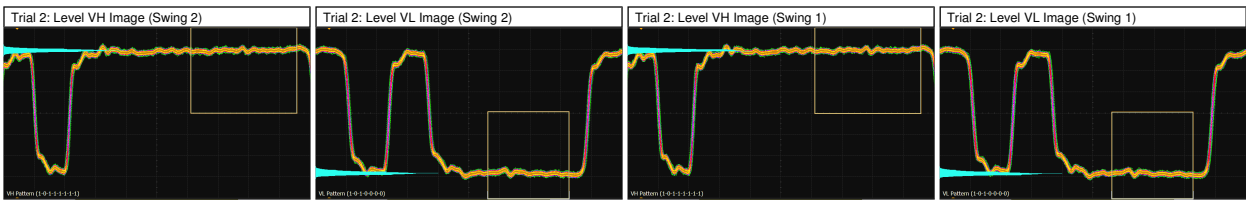


VH Pattern (1-0-1-1-1-1-1)

Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 1		326.0 ps/div	1.481 ns	140.0 mV/div	-11.10 mV



Trial 2



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✓ Lane 1 - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

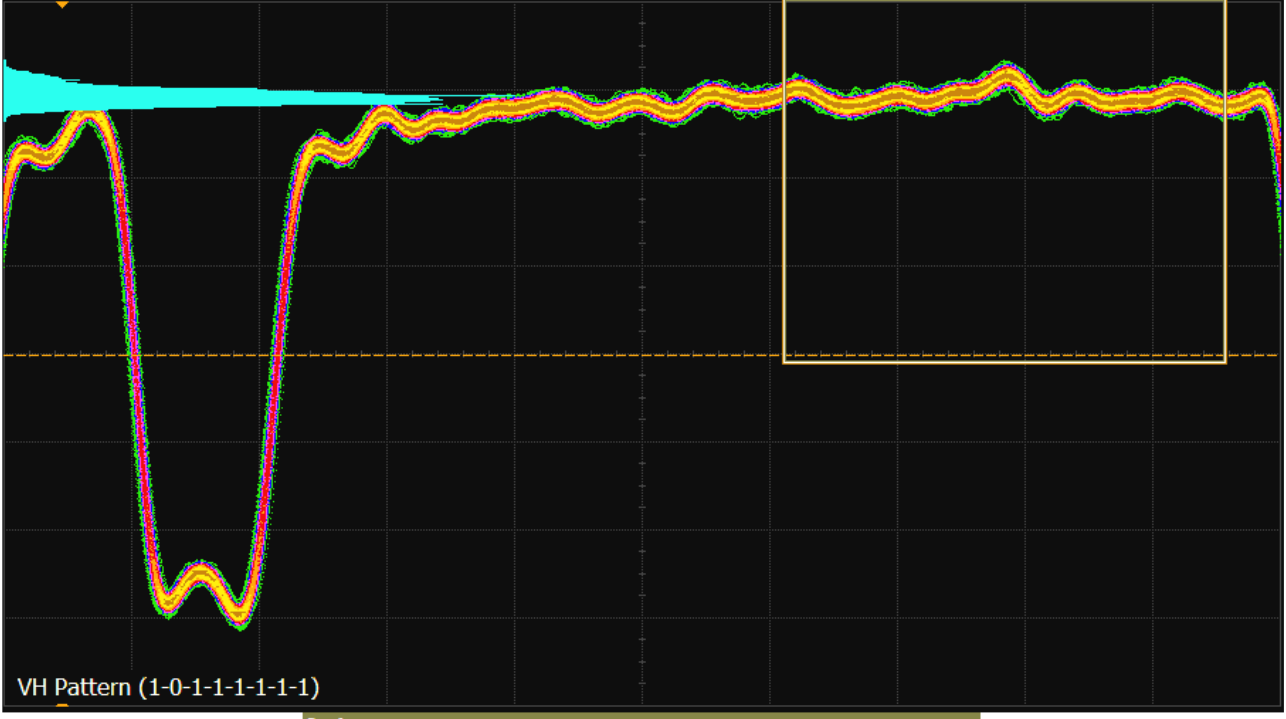
Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
 Pass Limits: [100.0 mdB to 5.1000 dB] Lane 1 Non-PreEmphasis Level Test (Swing 2/Swing 1) (Worst of 2 Trials) 2.5650 dB # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

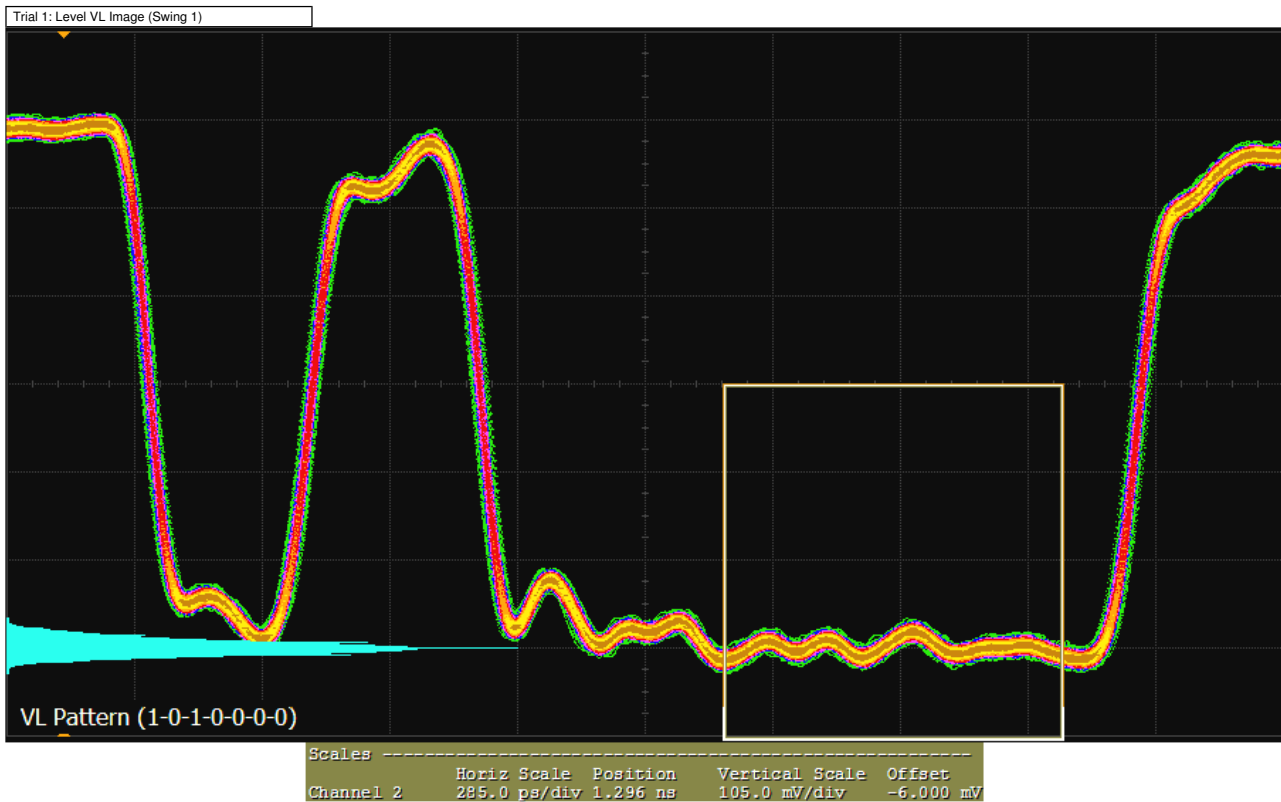
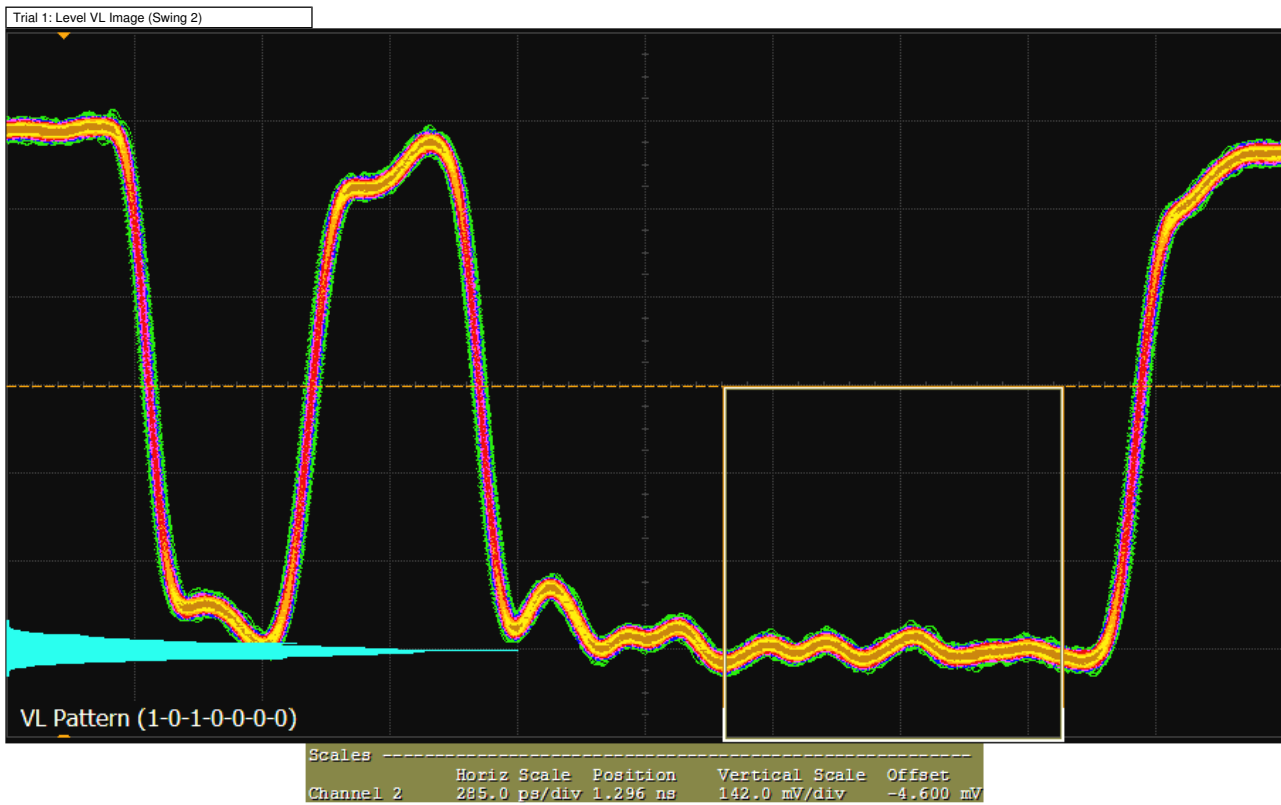
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Level VH Image (Swing 1)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitF
	Avg	2.578 dB	49.56 %																				
	StdDev	18.30 mdB	366.3 m%																				
	Range	25.87 mdB	518.0 m%																				
	Min	2.565 dB	49.30 %																				
	Max	2.591 dB	49.82 %																				
	Sum	5.156 dB	99.12 %																				
✓	Trial 1 (Worst)	2.5650 dB	49.3%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	401.220 mV	418.548 mV	819.768 mV	296.202 mV	313.953 mV	610.155 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2	2.5909 dB	49.8%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	398.058 mV	416.513 mV	814.571 mV	293.032 mV	311.452 mV	604.484 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

Trial 1

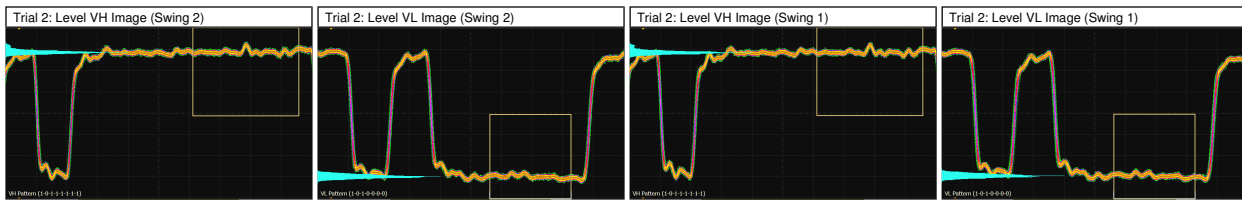
Trial 1: Level VH Image (Swing 2)



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 2		326.0 ps/div	1.481 ns	142.0 mV/div	-4.600 mV



Trial 2



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✓ Lane 2 - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [100.0 mdB to 5.1000 dB] **Lane 2 Non-PreEmphasis Level Test (Swing 2/Swing 1) (Worst of 2 Trials)** 2.5002 dB **# Trials Run:** 2 **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

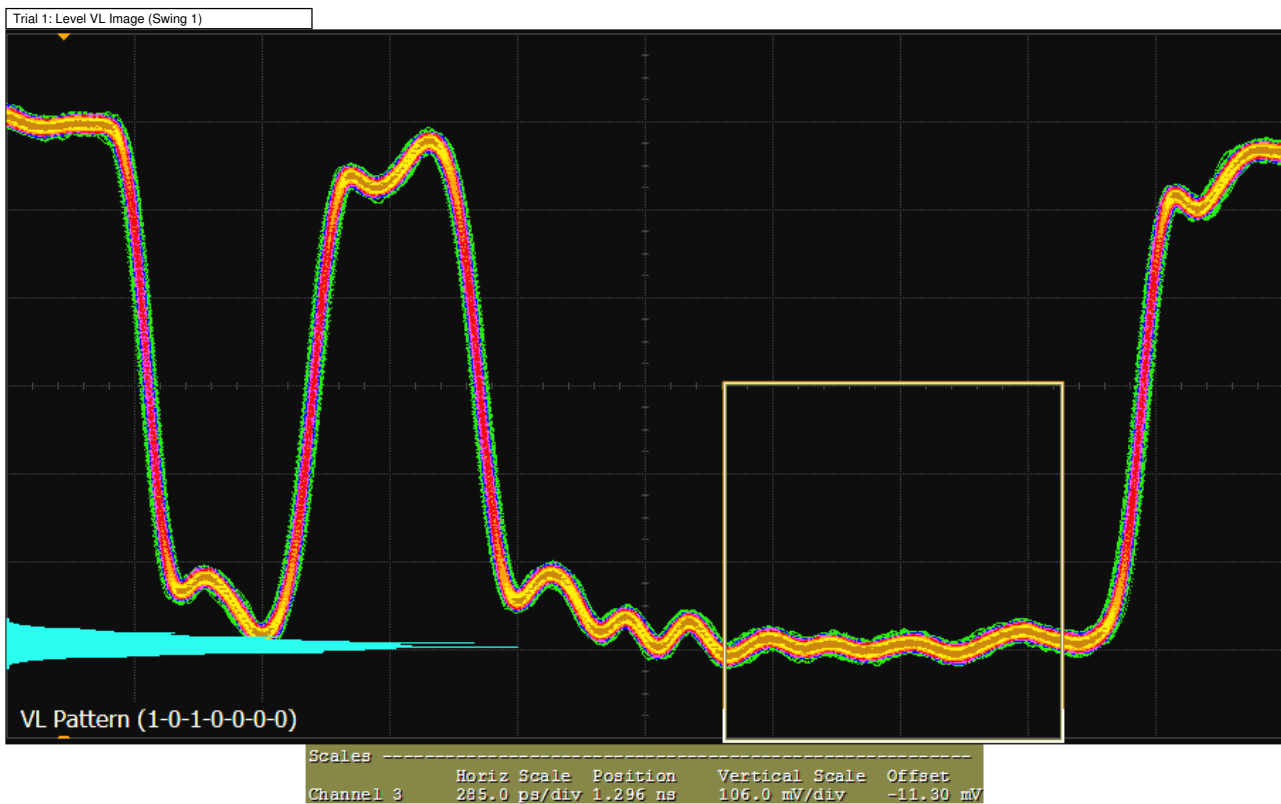
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Level VH Image (Swing 1)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitF
	Avg	2.508 dB	48.16 %																				
	StdDev	11.34 mdB	226.3 m%																				
	Range	16.04 mdB	320.0 m%																				
	Min	2.500 dB	48.00 %																				
	Max	2.516 dB	48.32 %																				
	Sum	5.016 dB	96.33 %																				
✓	Trial 1 (Worst)	2.5002 dB	48.0%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	401.228 mV	427.992 mV	829.219 mV	298.874 mV	322.942 mV	621.816 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2	2.5162 dB	48.3%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	398.274 mV	416.661 mV	814.935 mV	296.021 mV	313.957 mV	609.977 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

Trial 1

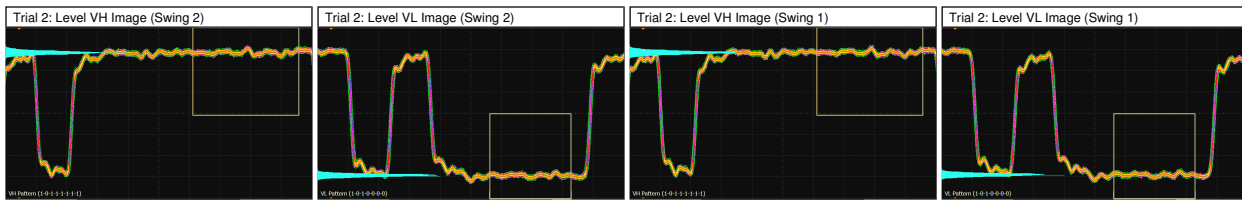
Trial 1: Level VH Image (Swing 2)



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	326.0 ps/div	1.481 ns	141.0 mV/div	-8.400 mV	



Trial 2



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✓ Lane 3 - Non-PreEmphasis Level Test (Swing 2/ Swing 1) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

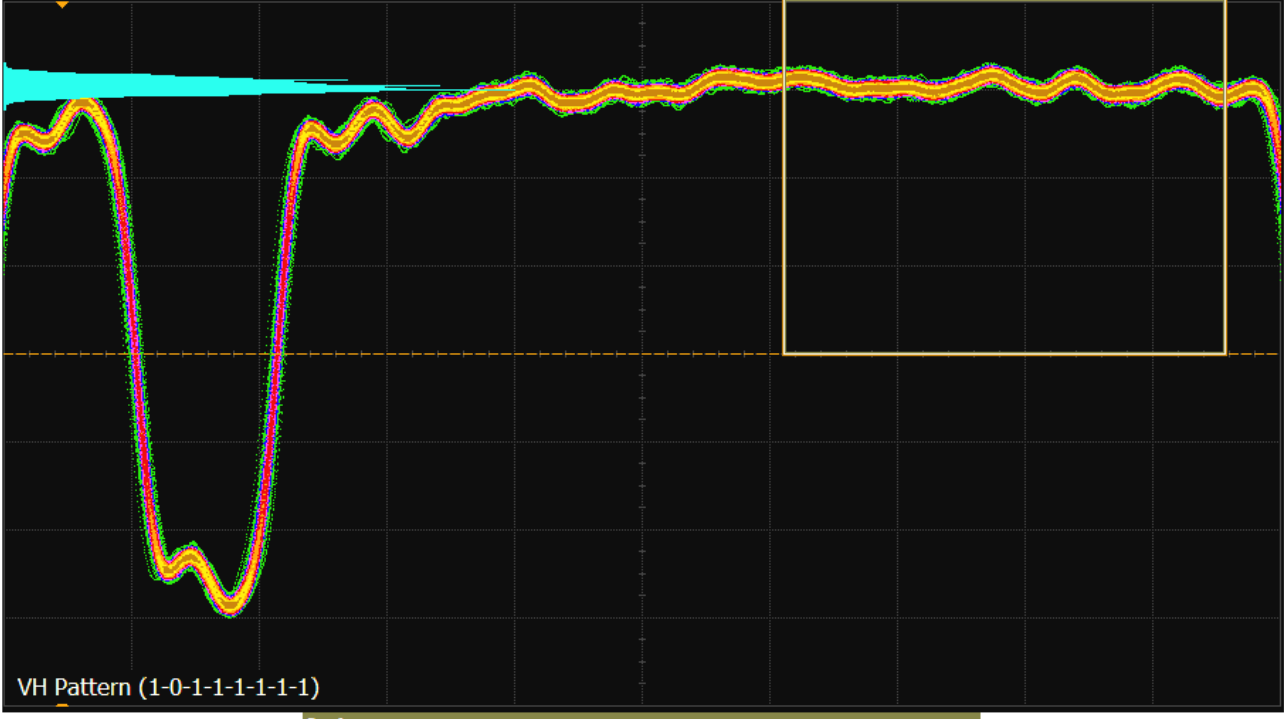
Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [100.0 mdB to 5.1000 dB] **Lane 3 Non-PreEmphasis Level Test (Swing 2/Swing 1) (Worst of 2 Trials)** 2.6964 dB **# Trials Run:** 2 **Worst Trial:** Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Level VH Image (Swing 1)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitR
	Avg	2.678 dB	48.44 %																				
	StdDev	25.97 mdB	519.0 m%																				
	Range	36.72 mdB	734.0 m%																				
	Min	2.660 dB	48.07 %																				
	Max	2.696 dB	48.81 %																				
	Sum	5.356 dB	96.88 %																				
✓	Trial 1	2.6597 dB	48.8%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	395.694 mV	419.681 mV	815.375 mV	288.867 mV	311.442 mV	600.309 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2 (Worst)	2.6964 dB	48.1%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	395.436 mV	418.812 mV	814.248 mV	286.992 mV	309.957 mV	596.950 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

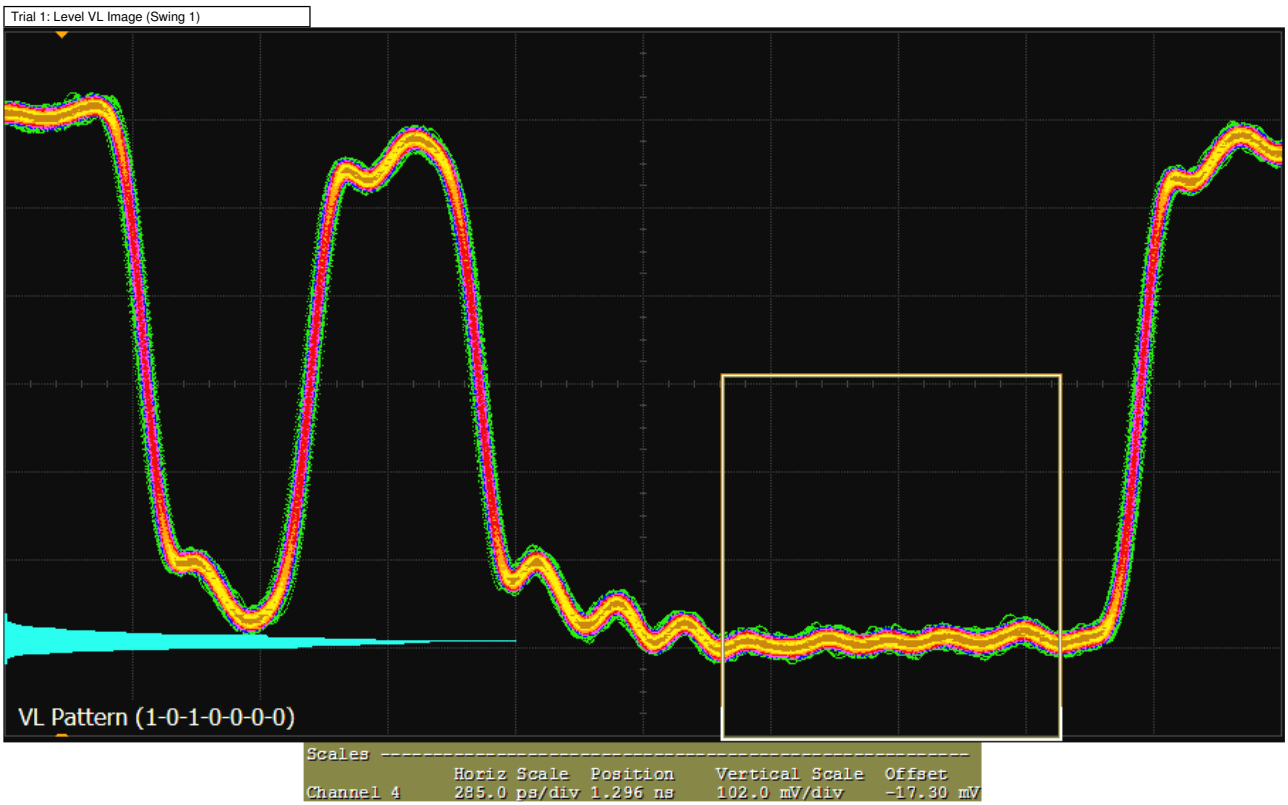
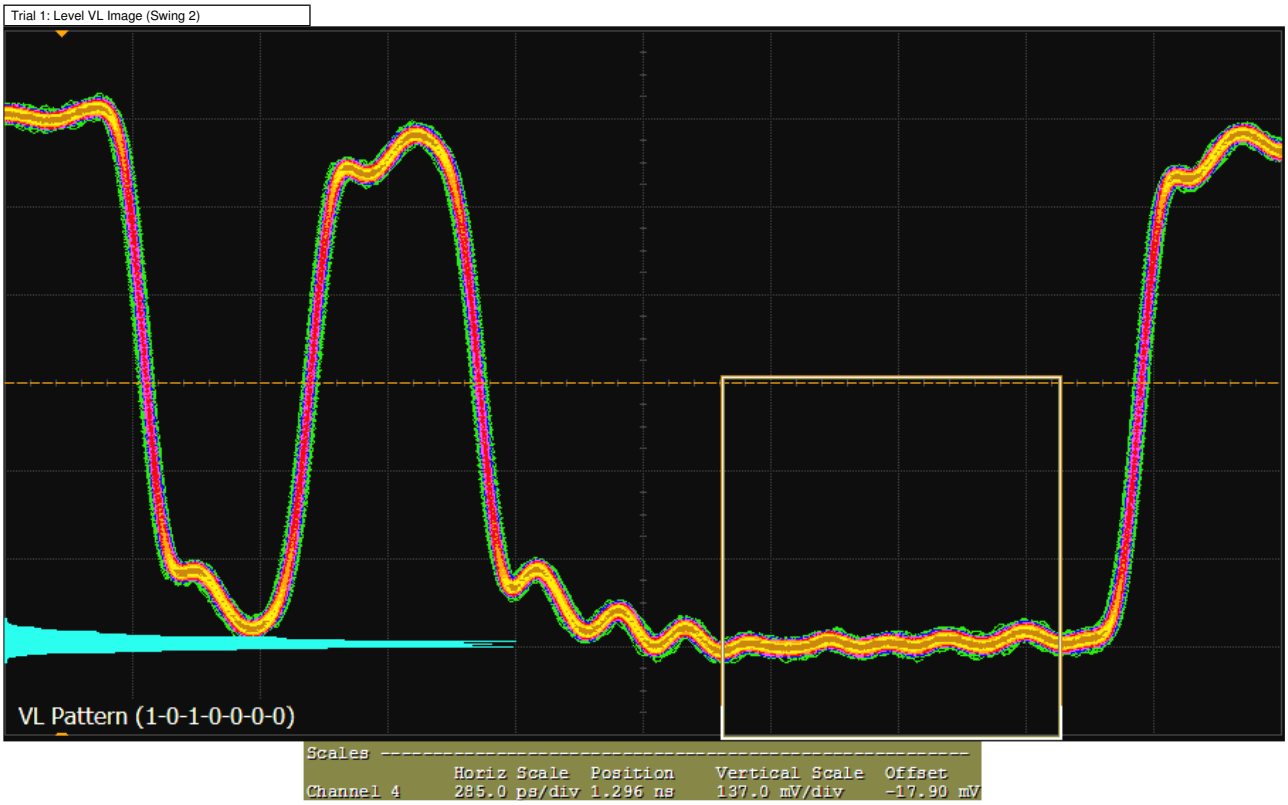
Trial 1

Trial 1: Level VH Image (Swing 2)

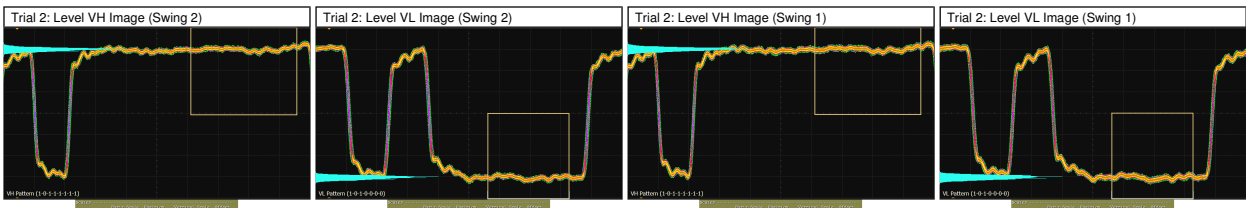


Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	326.0 ps/div	1.482 ns	137.0 mV/div	-17.90 mV





Trial 2



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✓ Lane 0 - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

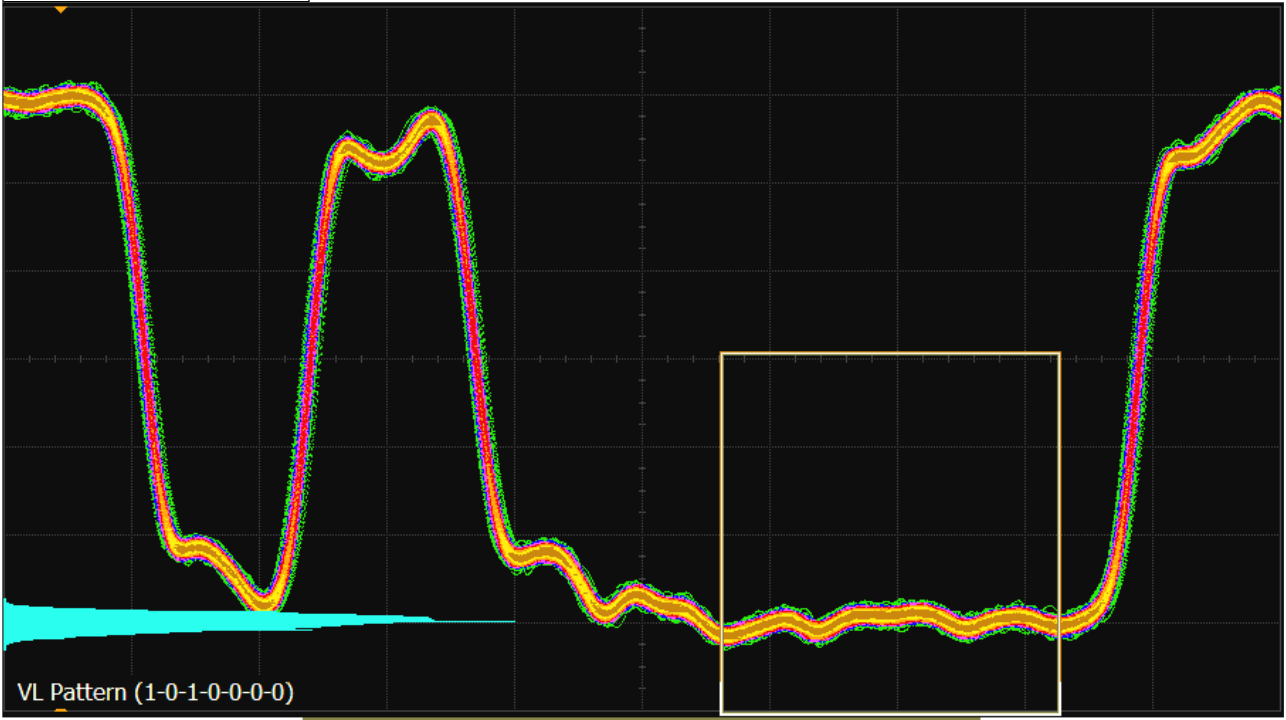
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: <= 250 mdB PreEmphasis (Pre-emphasis 0) (Worst of 8 Trials) -546 mdB # Trials Run: 8 Worst Trial: Trial 8

Overall Summary + details of 8 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-1.277 dB	610.8 %											
	StdDev	705.2 mdB	282.1 %											
	Range	1.517 dB	607.2 %											
	Min	-2.064 dB	318.4 %											
	Max	-546.4 mdB	925.6 %											
	Sum	-10.21 dB	4.886 k%											
✓	Trial 1	-1.894 dB	857.6% (See image)	(See image)	(See image)	1000	659.238 mV	819.850 mV	-1.894 dB	2.7 Gbps	Swing 2 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-2.024 dB	909.6% (See image)	(See image)	(See image)	1000	482.050 mV	608.543 mV	-2.024 dB	2.7 Gbps	Swing 1 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-2.064 dB	925.6% (See image)	(See image)	(See image)	1000	338.319 mV	429.059 mV	-2.064 dB	2.7 Gbps	Swing 0 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	-1.733 dB	793.2% (See image)	(See image)	(See image)	1000	829.258 mV	1.012316 V	-1.733 dB	2.7 Gbps	Swing 3 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 5	-595 mdB	338.0% (See image)	(See image)	(See image)	1000	760.296 mV	814.202 mV	-595 mdB	1.62 Gbps	Swing 2 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 6	-642 mdB	356.8% (See image)	(See image)	(See image)	1000	559.753 mV	602.664 mV	-642 mdB	1.62 Gbps	Swing 1 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	-717 mdB	386.8% (See image)	(See image)	(See image)	1000	389.368 mV	422.883 mV	-717 mdB	1.62 Gbps	Swing 0 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 8 (Worst)	-546 mdB	318.4% (See image)	(See image)	(See image)	1000	944.975 mV	1.006326 V	-546 mdB	1.62 Gbps	Swing 3 0	Pre-emphasis 0	SSC Disabled	Level 0

Trial 1

Trial 1: VL NonPreEmphasis Image

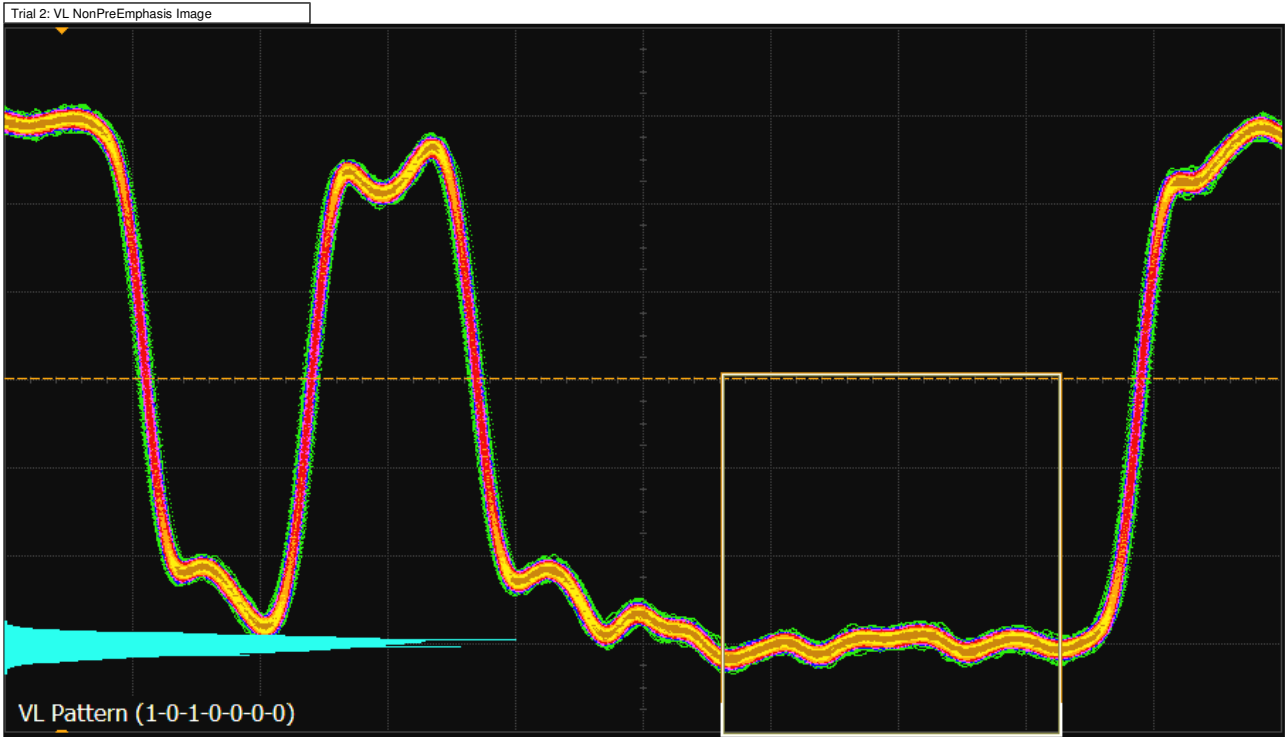


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	285.0 ps/div	1.296 ns	140.0 mV/div	-11.10 mV

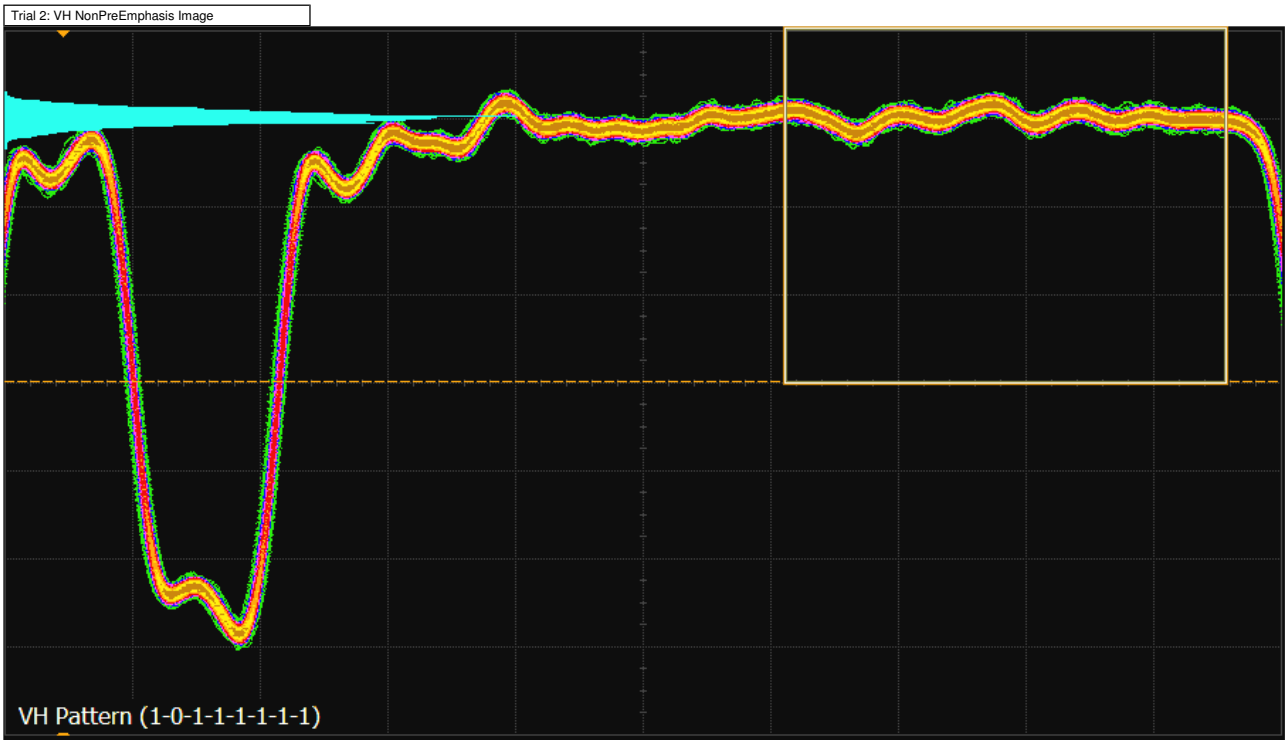


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	326.0 ps/div	1.481 ns	140.0 mV/div	-11.10 mV

Trial 2

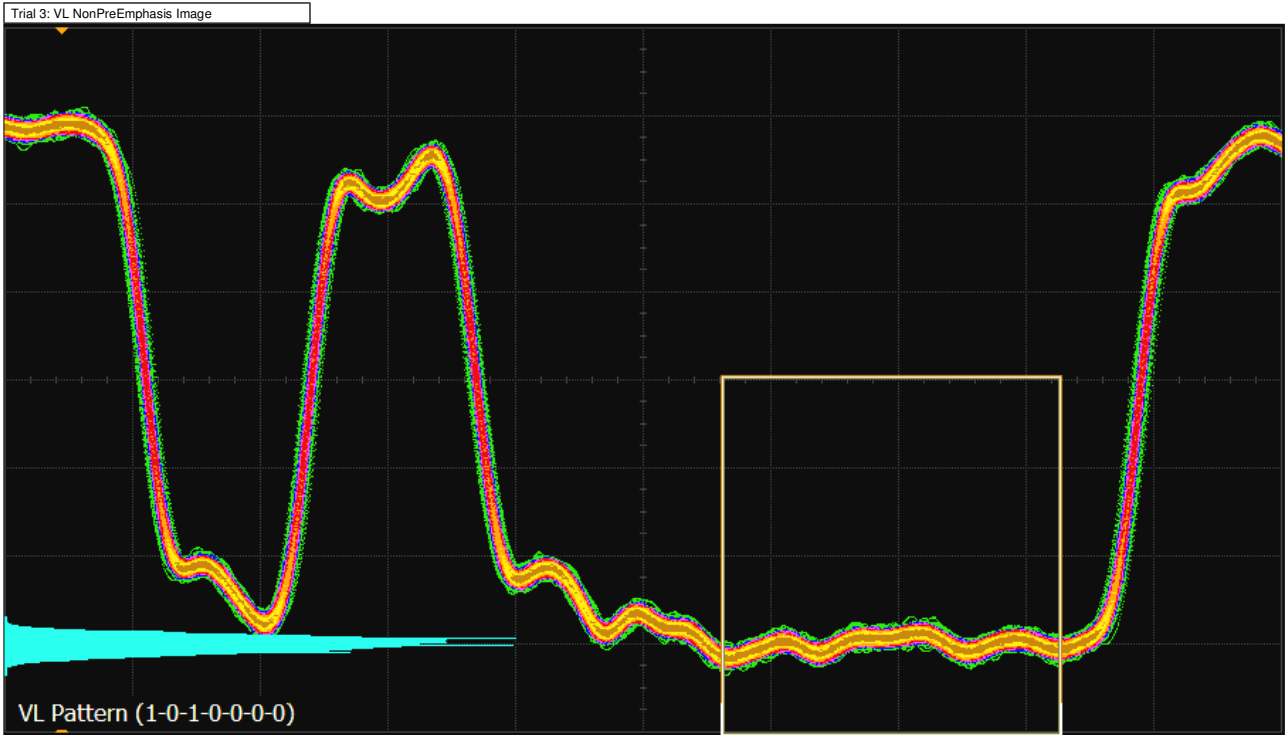


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	285.0 ps/div	1.296 ns	103.0 mV/div	-11.30 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	326.0 ps/div	1.481 ns	103.0 mV/div	-11.30 mV

Trial 3

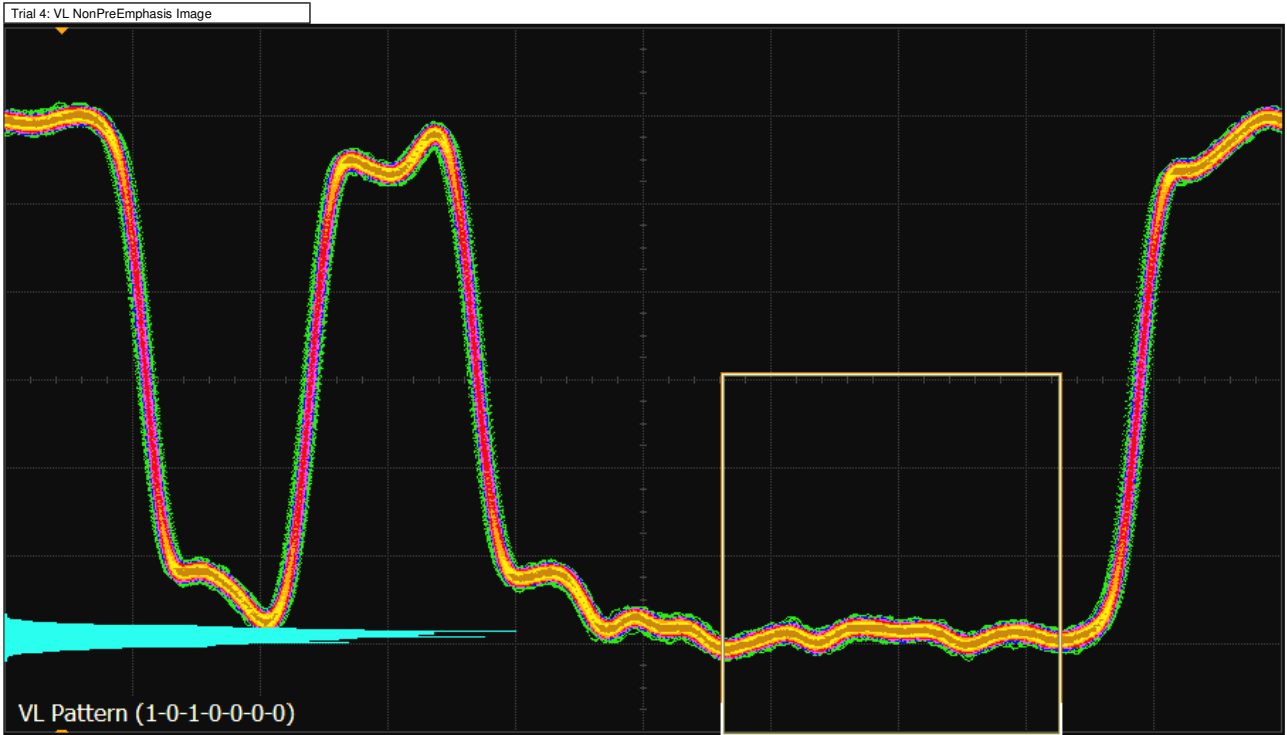


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	285.0 ps/div	1.296 ns	73.50 mV/div	-9.300 mV



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	326.0 ps/div	1.482 ns	73.50 mV/div	-9.300 mV

Trial 4



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	285.0 ps/div	1.296 ns	171.0 mV/div	-11.40 mV

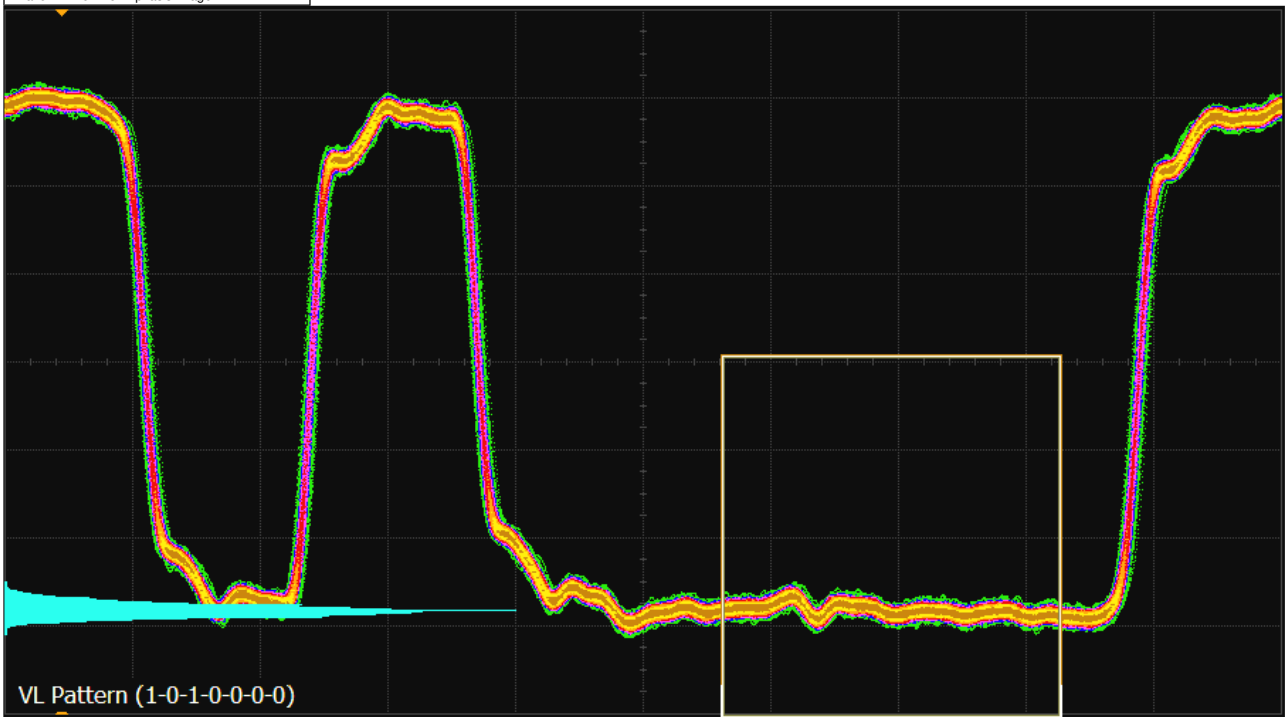
Trial 4: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	326.0 ps/div	1.492 ns	171.0 mV/div	-11.40 mV

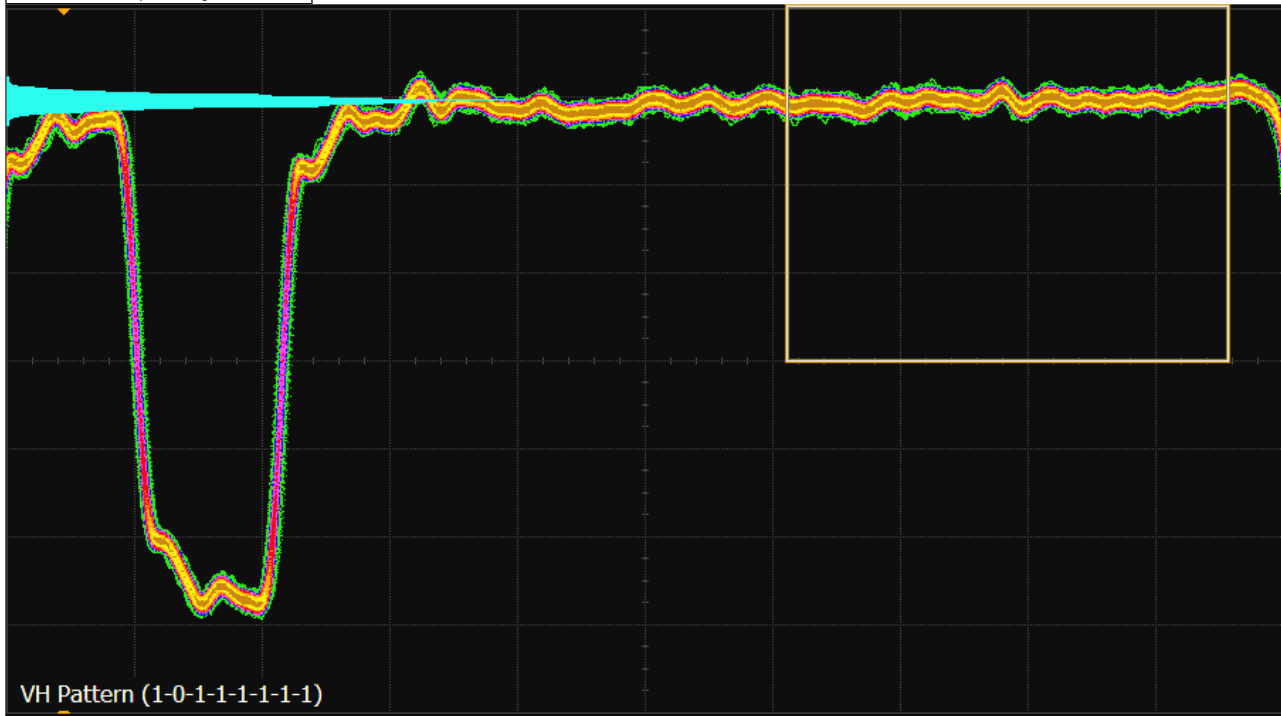
Trial 5

Trial 5: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	475.0 ps/div	2.161 ns	143.0 mV/div	-14.80 mV

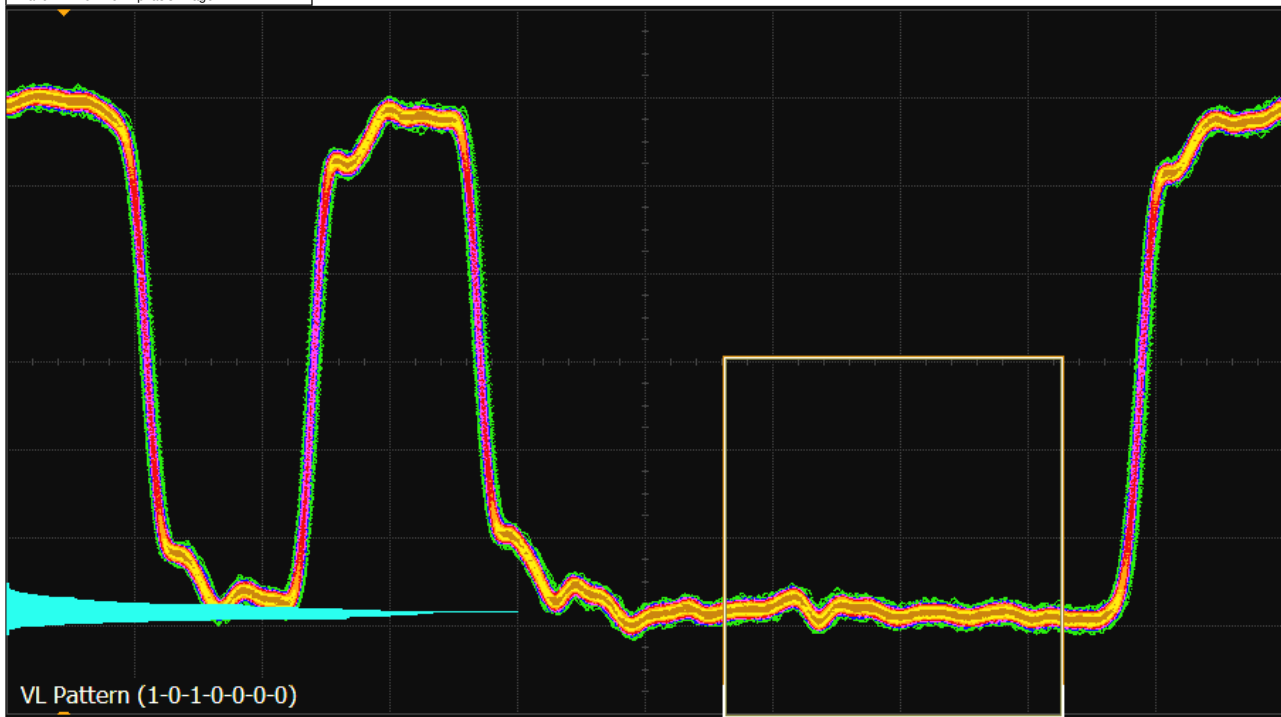
Trial 5: VH NonPreEmphasis Image



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	543.0 ps/div	2.469 ns	143.0 mV/div	-14.80 mV

Trial 6

Trial 6: VL NonPreEmphasis Image



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	475.0 ps/div	2.161 ns	106.0 mV/div	-17.10 mV

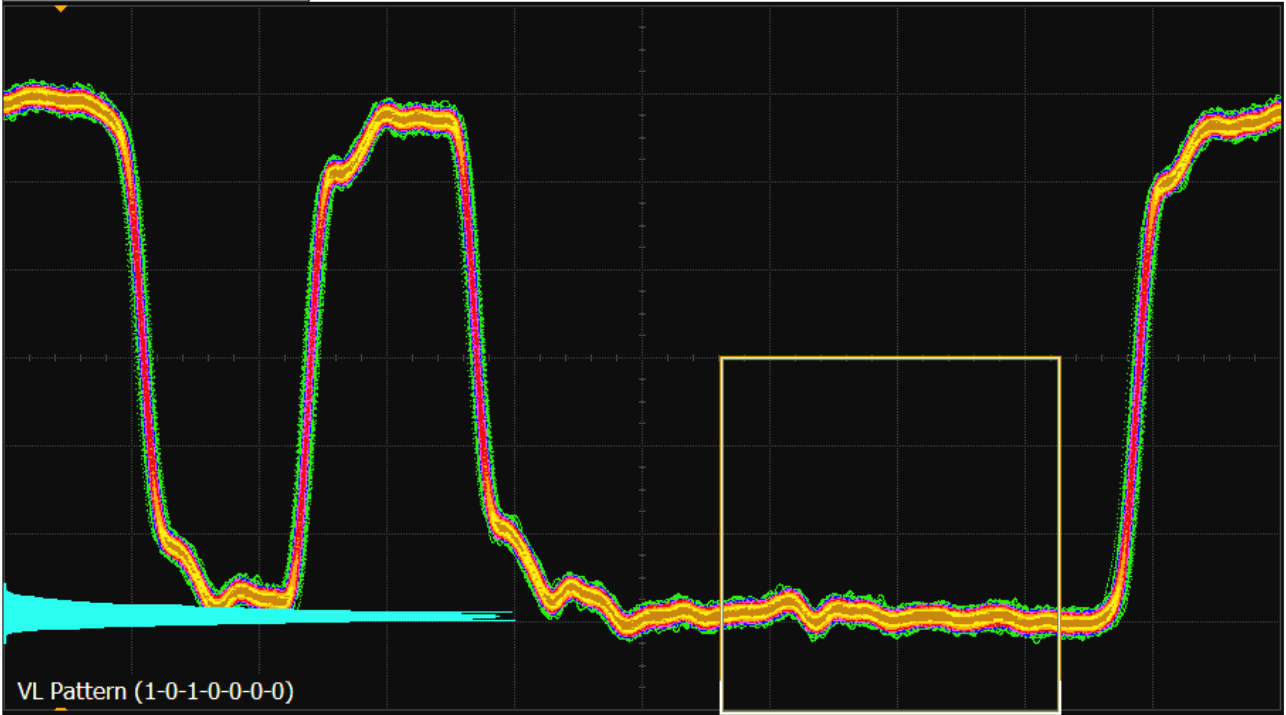
Trial 6: VH NonPreEmphasis Image



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	543.0 ps/div	2.469 ns	106.0 mV/div	-17.10 mV

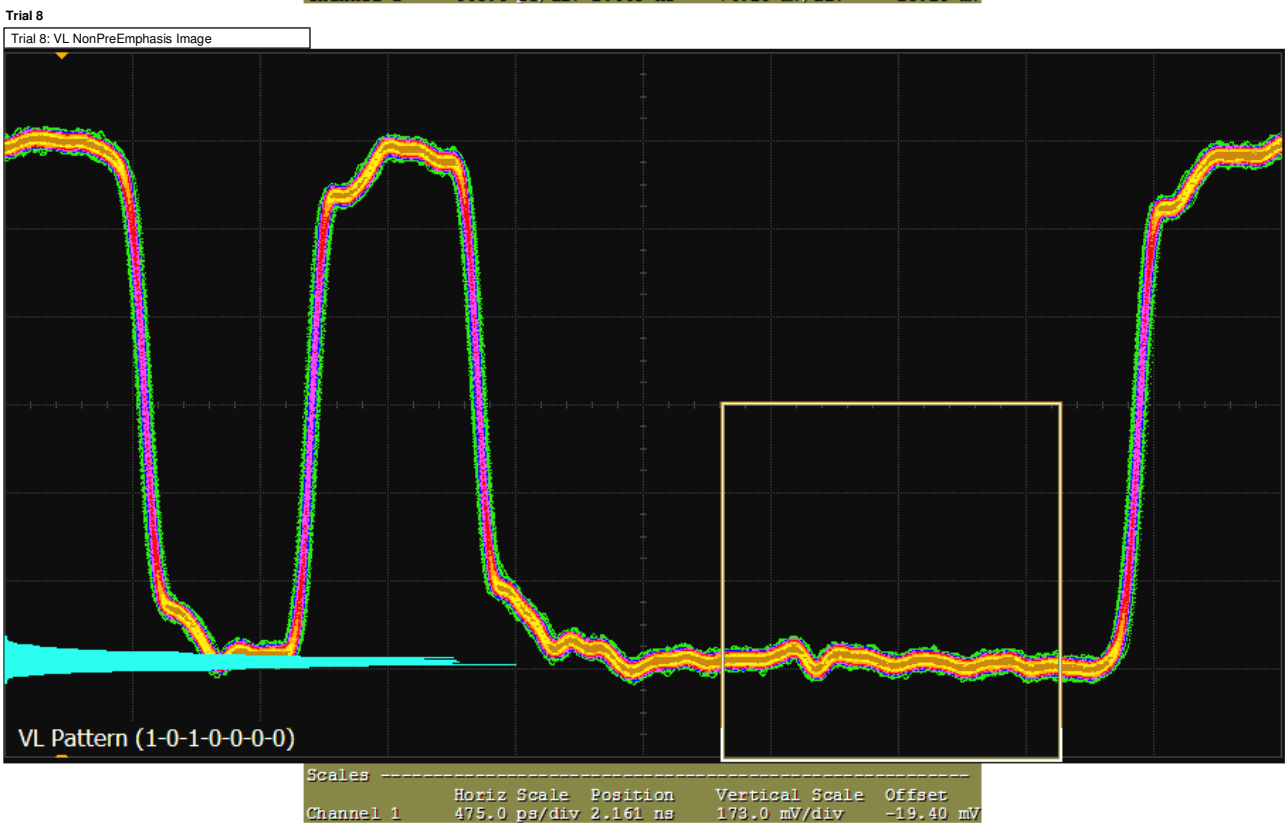
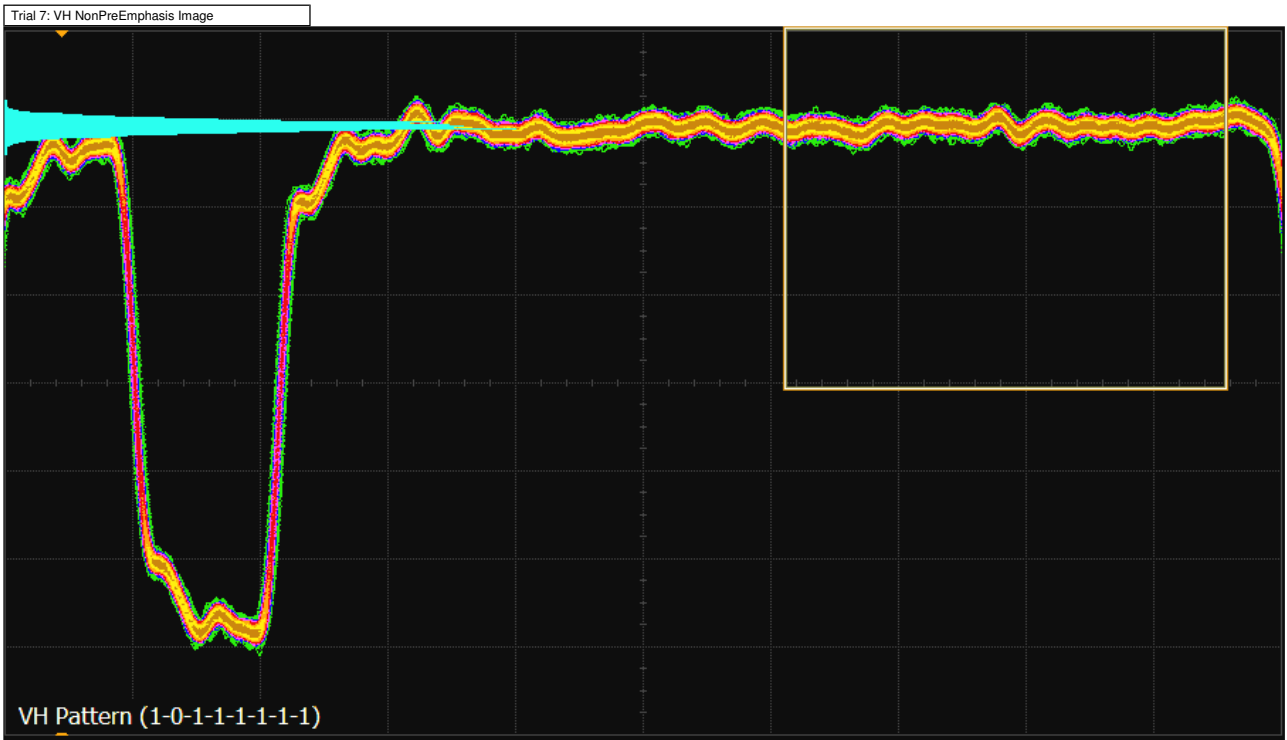
Trial 7

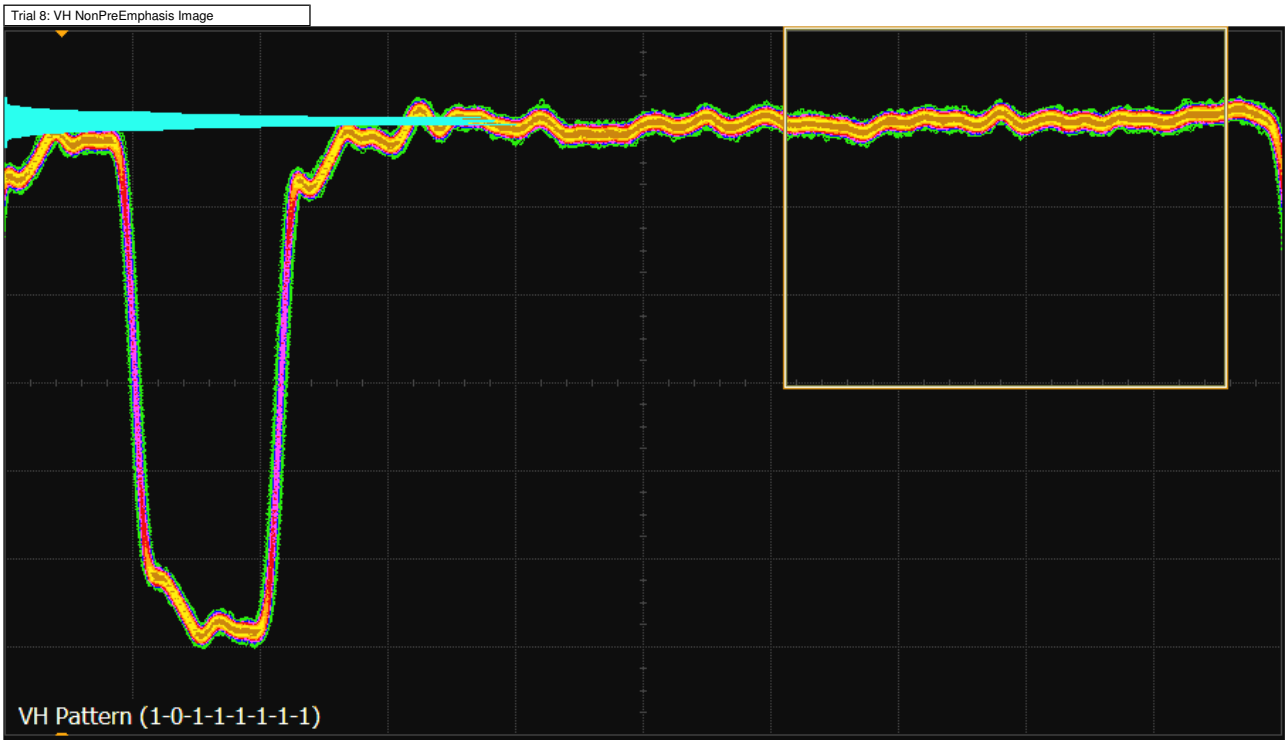
Trial 7: VL NonPreEmphasis Image



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	74.20 mV/div	-13.20 mV







Scales -----				
	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	543.0 ps/div	2.469 ns	173.0 mV/div	-19.40 mV

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✓ Lane 1 - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

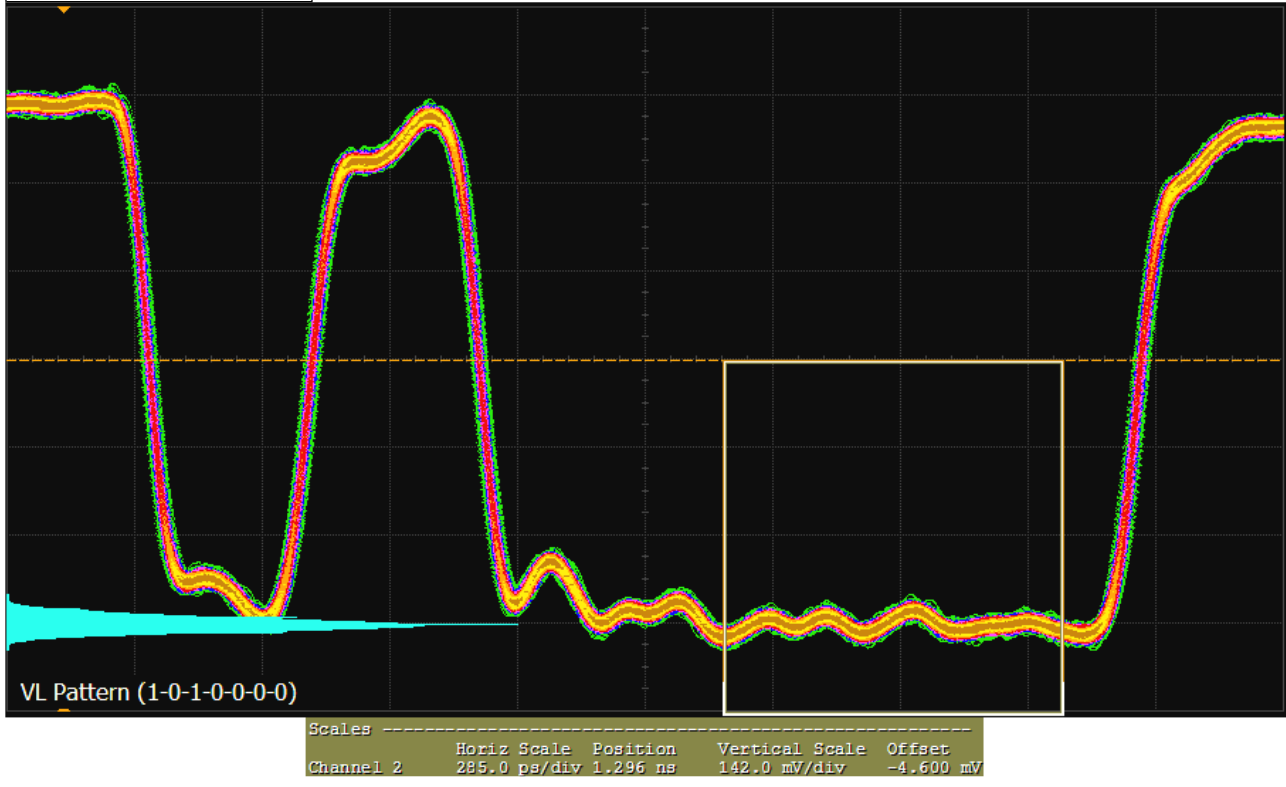
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: <= 250 mdB PreEmphasis(Pre-emphasis 0) (Worst of 8 Trials) -514 mdB # Trials Run: 8 Worst Trial: Trial 8

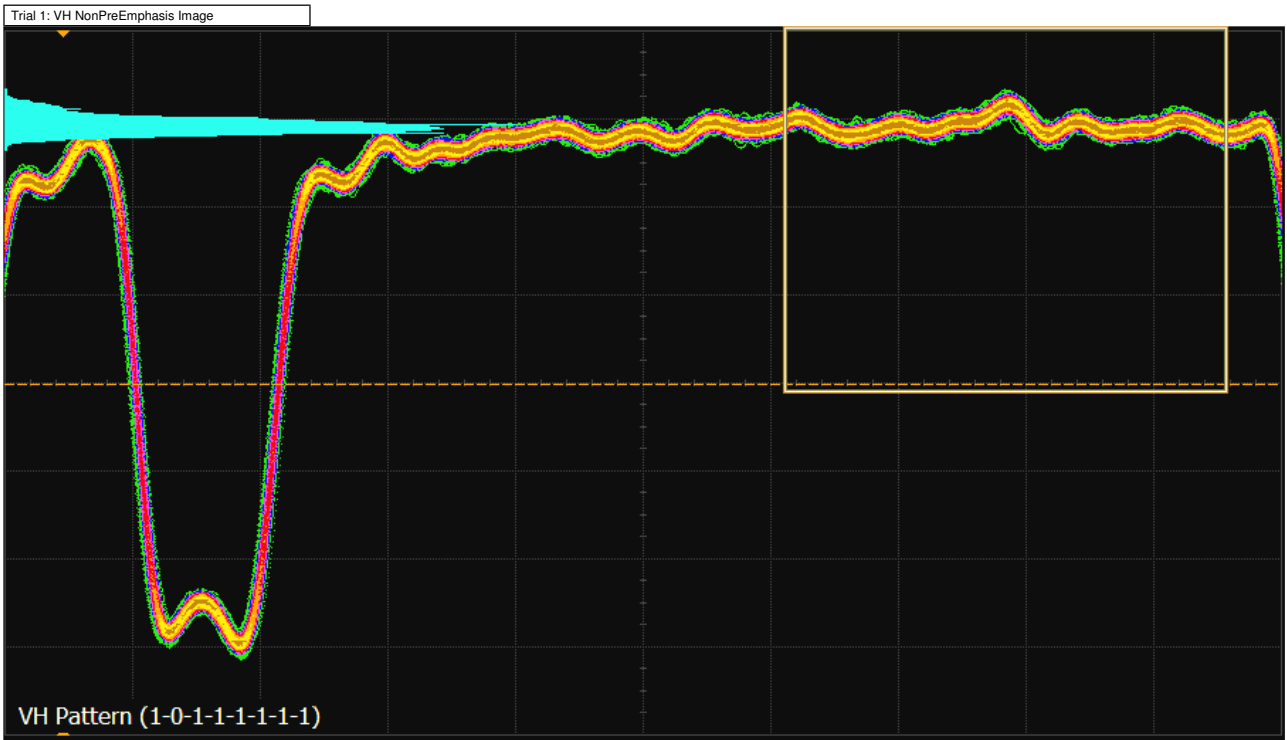
Overall Summary + details of 8 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-1.053 dB	521.3 %											
	StdDev	454.2 mdB	181.8 %											
	Range	1.086 dB	434.4 %											
	Min	-1.600 dB	305.6 %											
	Max	-514.2 mdB	740.0 %											
	Sum	-8.426 dB	4.170 k%											
✓	Trial 1	-1.426 dB	670.4% (See image)	(See image)	(See image)	1000	695.662 mV	819.768 mV	-1.426 dB	2.7 Gbps	Swing 2 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-1.524 dB	709.6% (See image)	(See image)	(See image)	1000	511.980 mV	610.155 mV	-1.524 dB	2.7 Gbps	Swing 1 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-1.600 dB	740.0% (See image)	(See image)	(See image)	1000	357.736 mV	430.084 mV	-1.600 dB	2.7 Gbps	Swing 0 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	-1.319 dB	627.6% (See image)	(See image)	(See image)	1000	868.602 mV	1.010999 V	-1.319 dB	2.7 Gbps	Swing 3 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 5	-617 mdB	346.8% (See image)	(See image)	(See image)	1000	758.683 mV	814.571 mV	-617 mdB	1.62 Gbps	Swing 2 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 6	-674 mdB	369.6% (See image)	(See image)	(See image)	1000	559.335 mV	604.484 mV	-674 mdB	1.62 Gbps	Swing 1 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	-752 mdB	400.8% (See image)	(See image)	(See image)	1000	390.075 mV	425.355 mV	-752 mdB	1.62 Gbps	Swing 0 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 8 (Worst)	-514 mdB	305.6% (See image)	(See image)	(See image)	1000	949.266 mV	1.007163 V	-514 mdB	1.62 Gbps	Swing 3 0	Pre-emphasis 0	SSC Disabled	Level 0

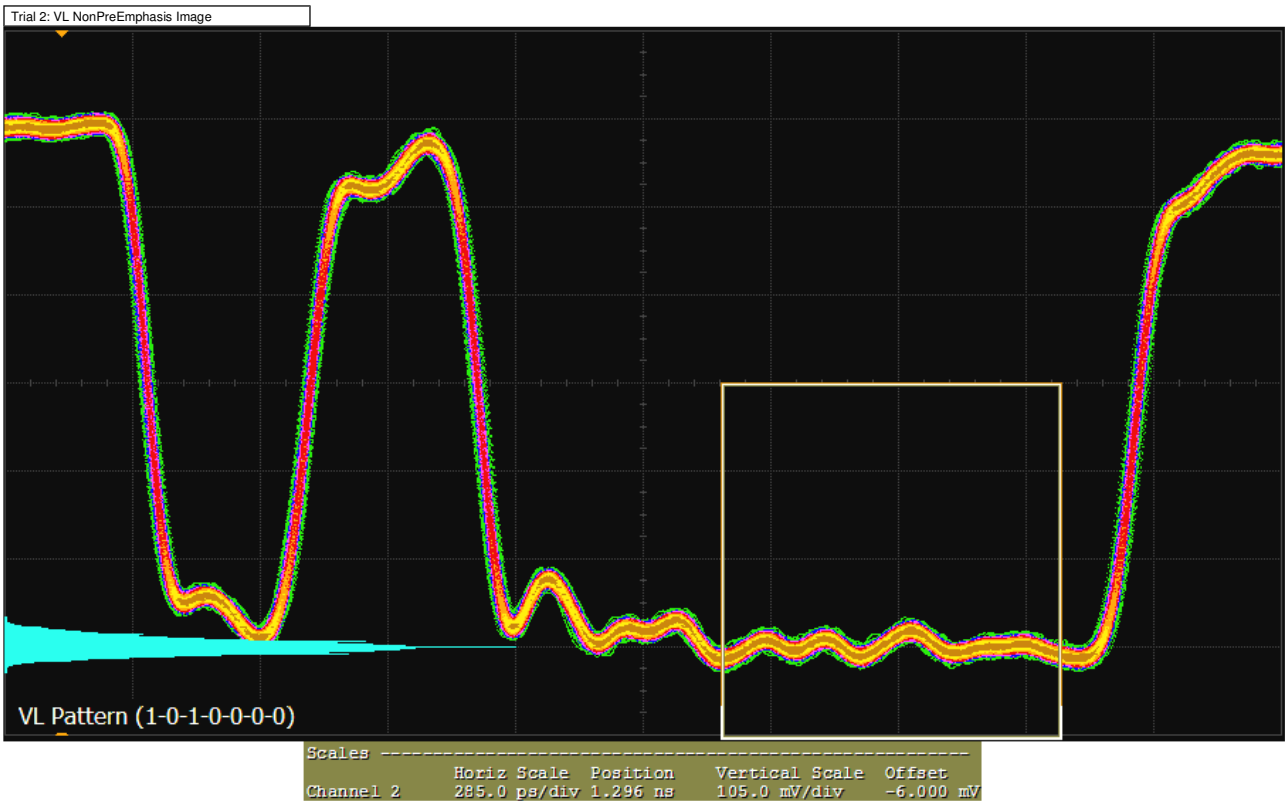
Trial 1

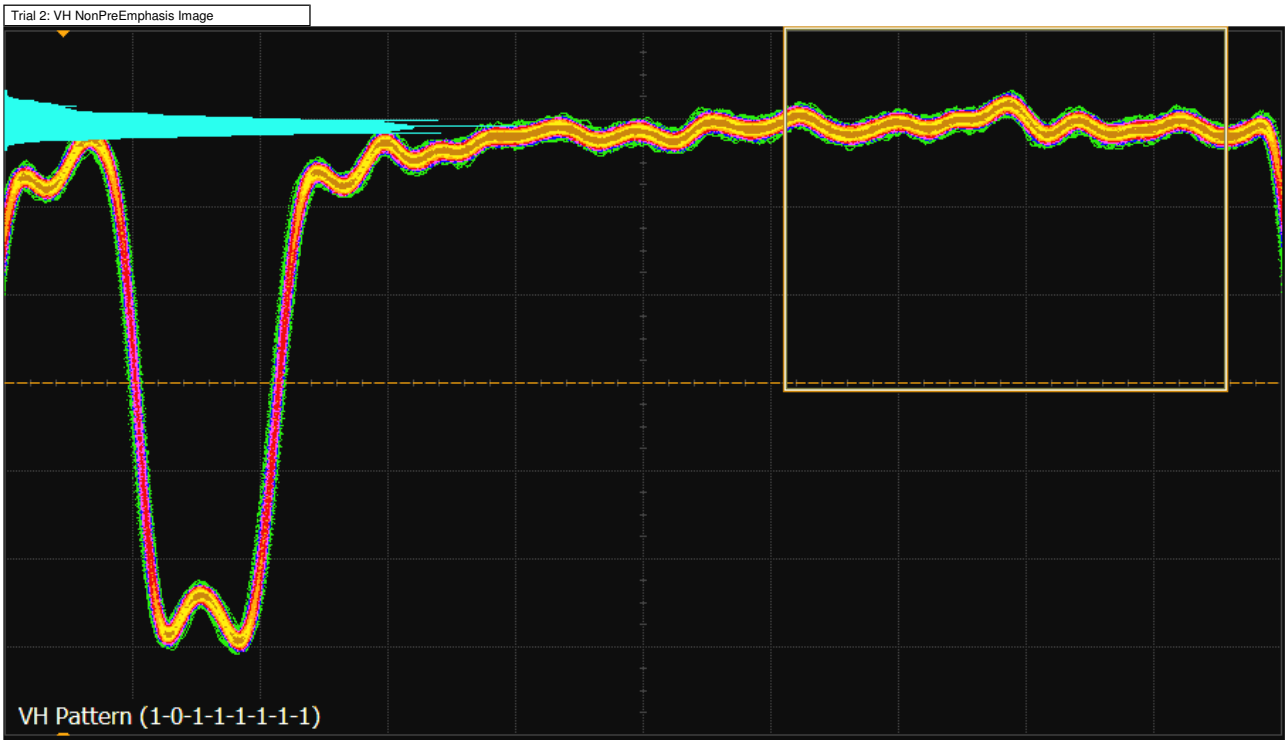
Trial 1: VL NonPreEmphasis Image





Trial 2





Trial 3



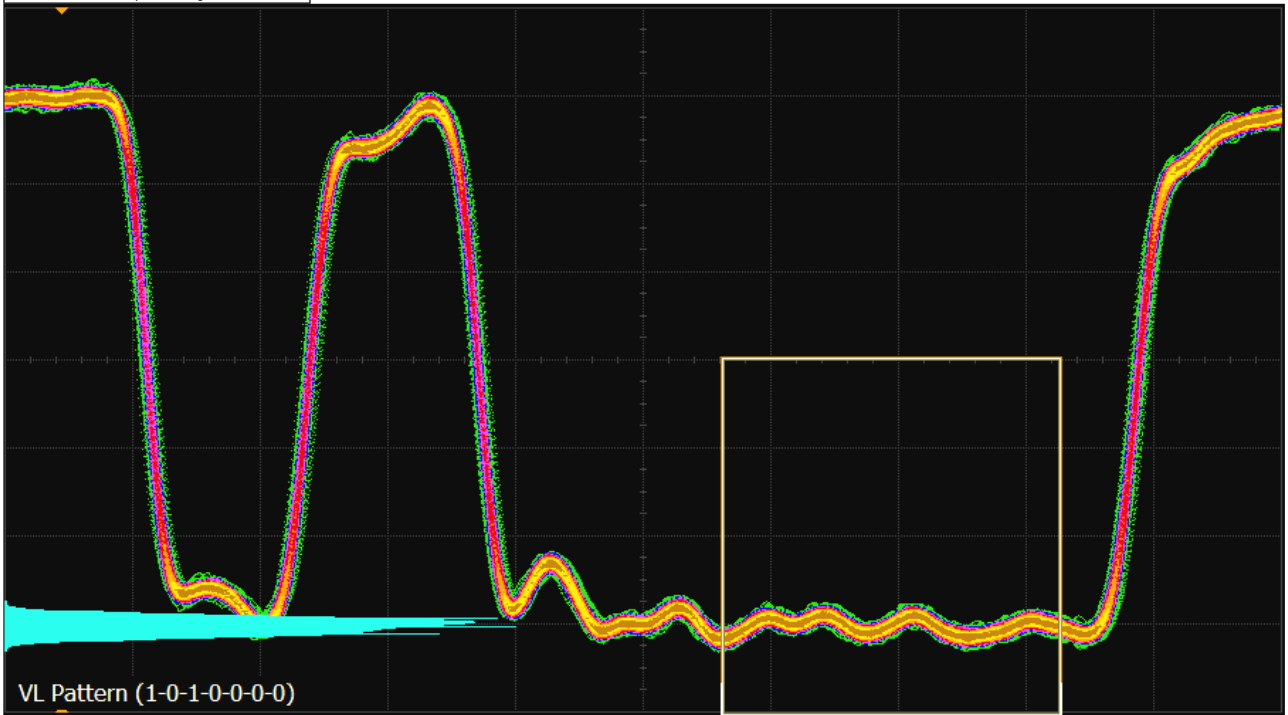
Trial 3: VH NonPreEmphasis Image



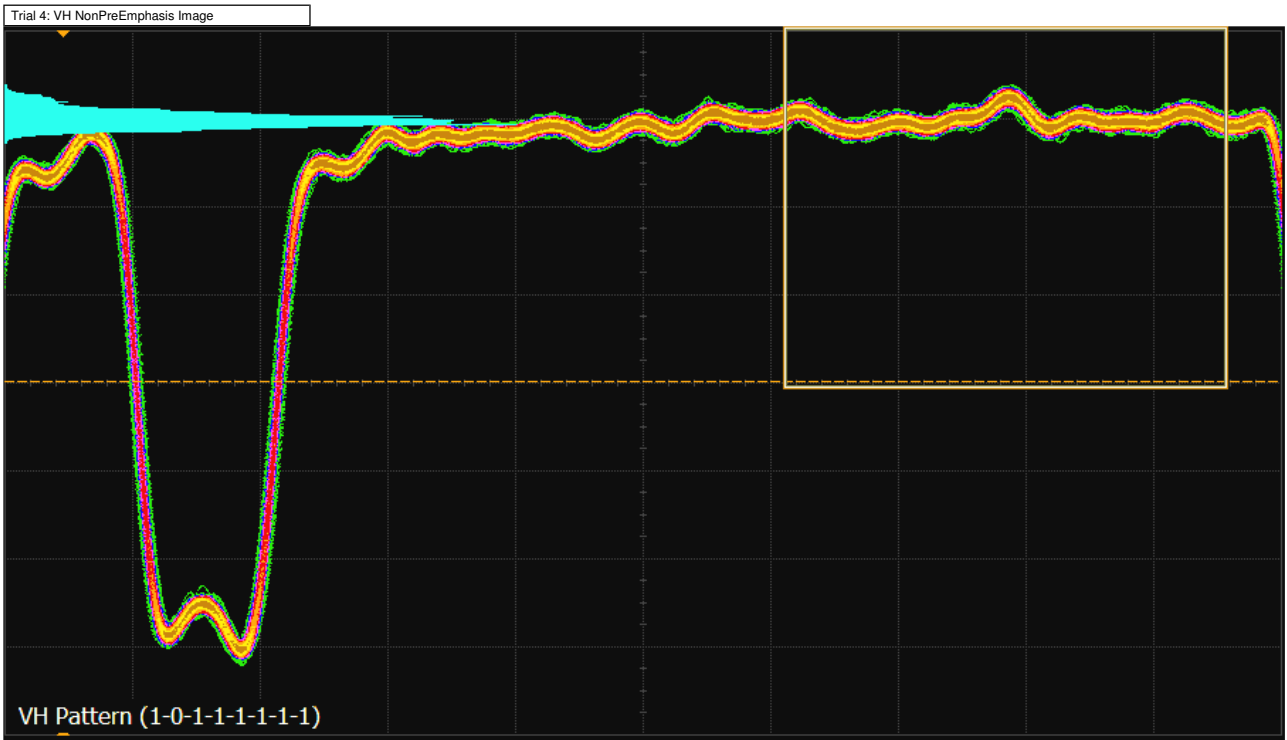
Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	326.0 ps/div	1.481 ns	73.50 mV/div	-8.300 mV

Trial 4

Trial 4: VL NonPreEmphasis Image

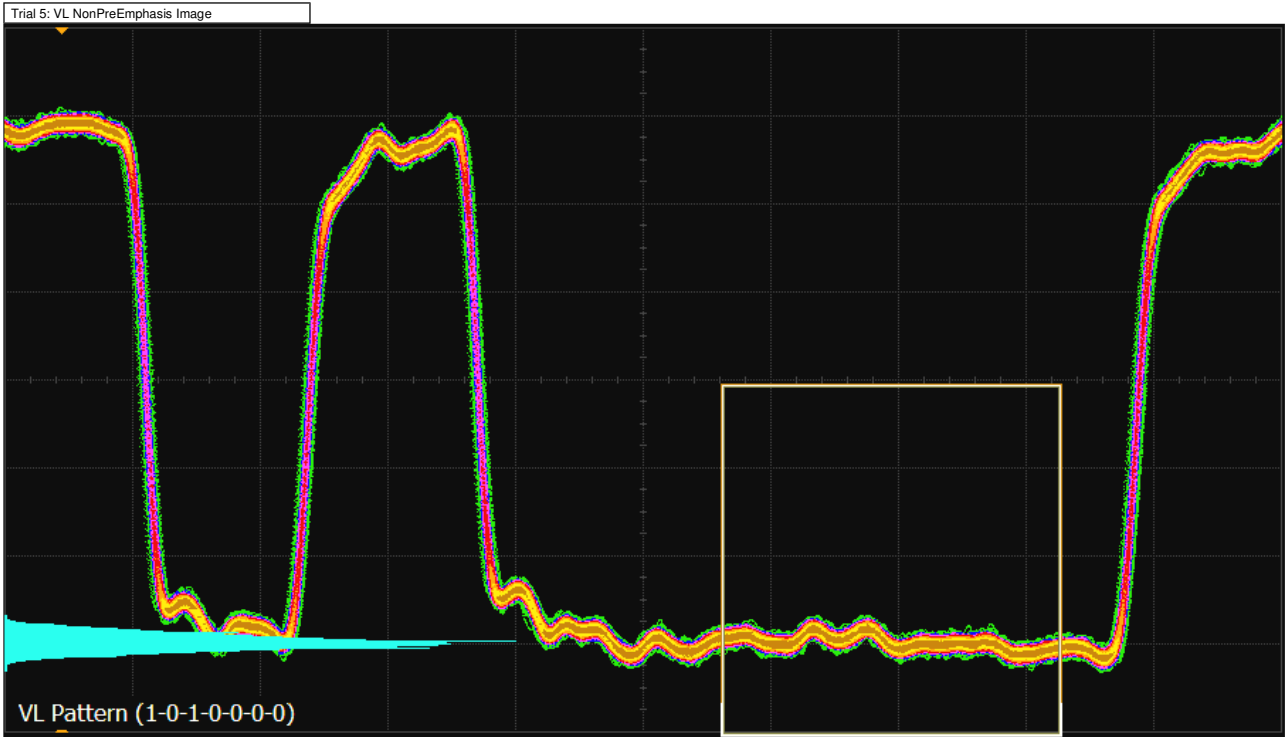


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	285.0 ps/div	1.296 ns	172.0 mV/div	-4.700 mV

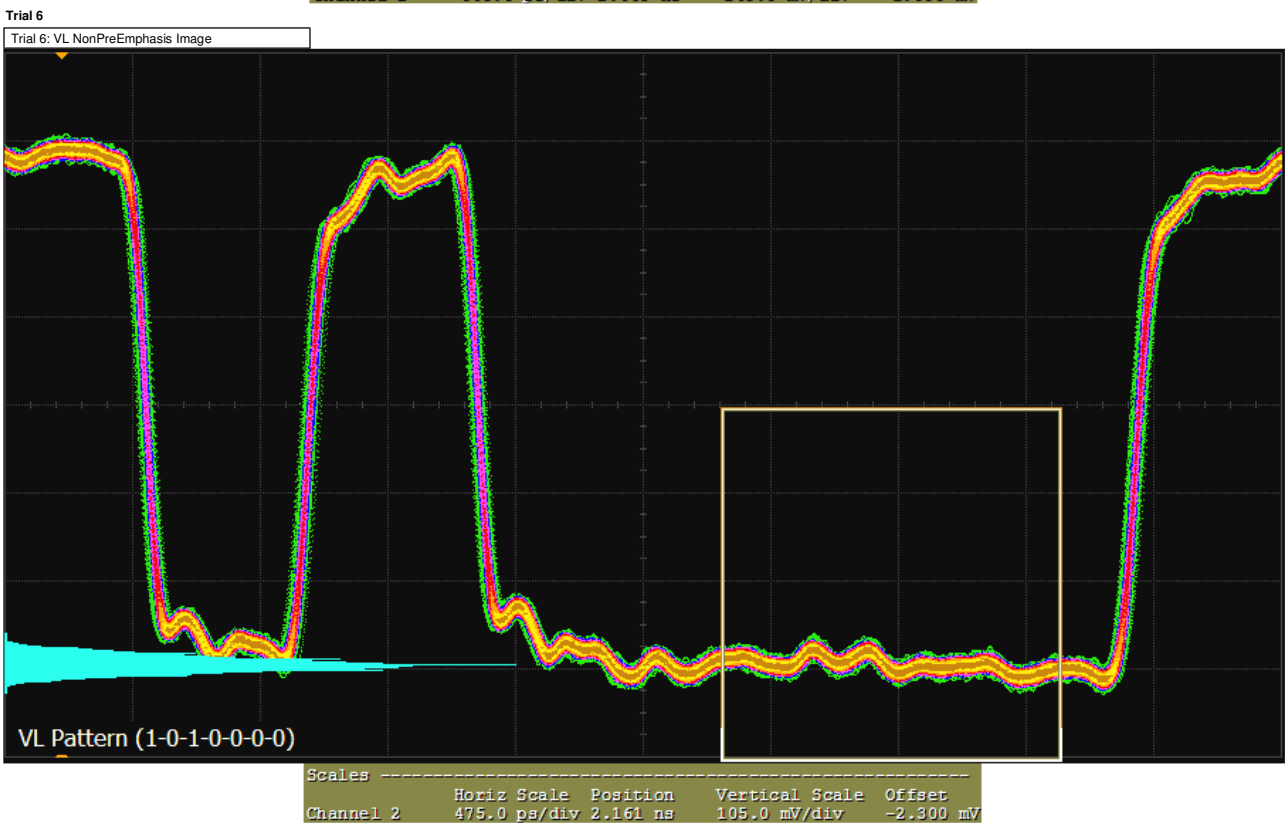
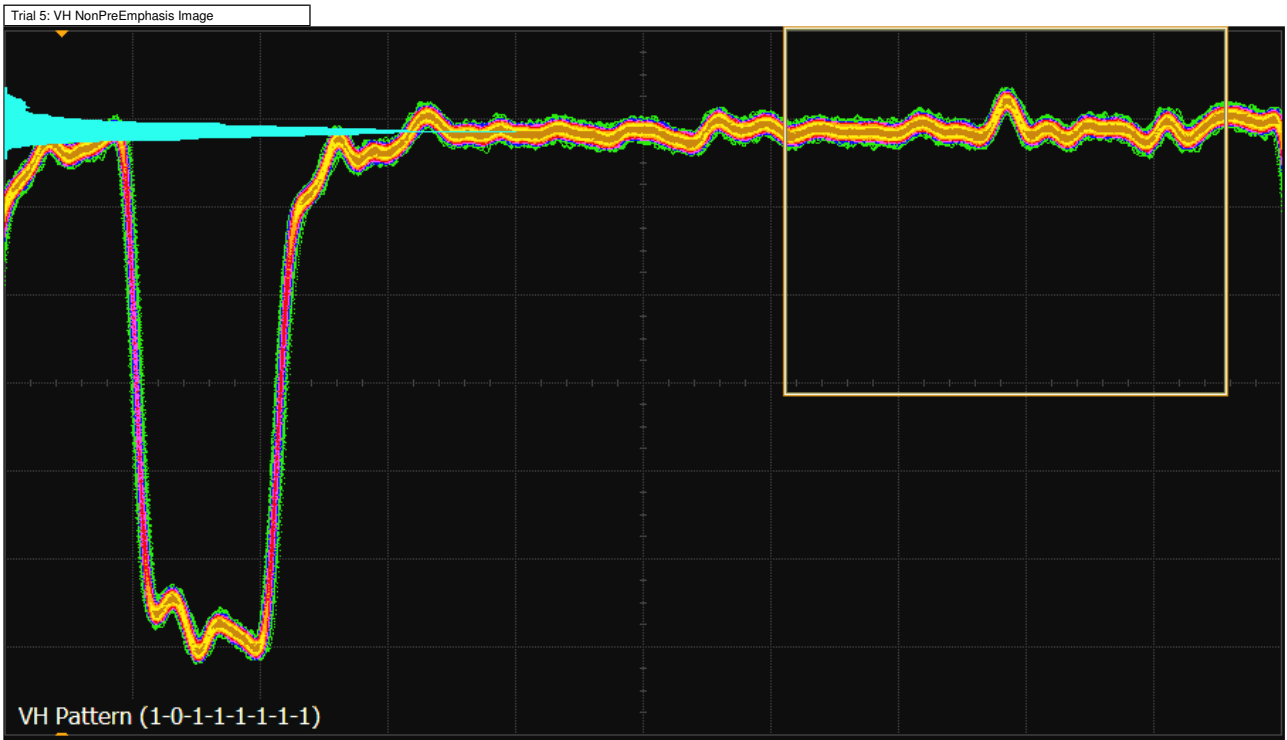


Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	326.0 ps/div	1.481 ns	172.0 mV/div	-4.700 mV

Trial 5



Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	475.0 ps/div	2.161 ns	143.0 mV/div	1.000 mV





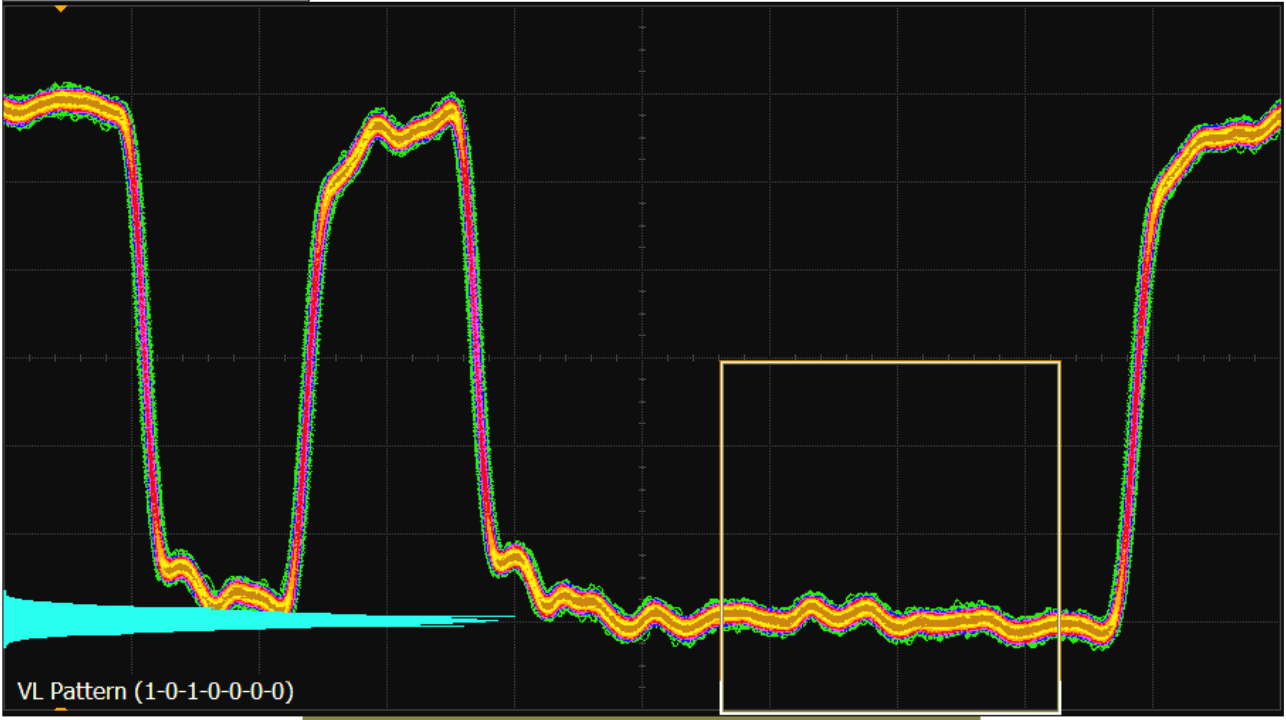
Trial 6: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	543.0 ps/div	2.469 ns	105.0 mV/div	-2.300 mV

Trial 7

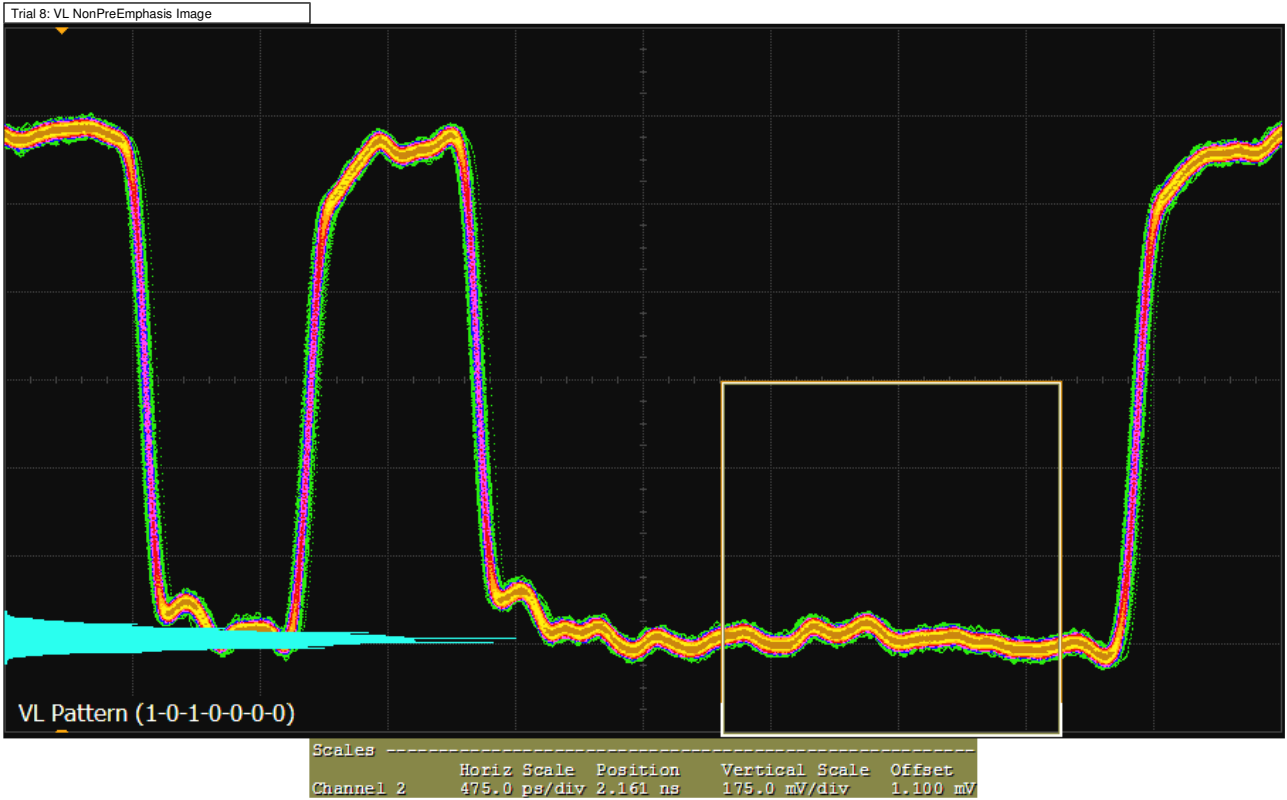
Trial 7: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	475.0 ps/div	2.161 ns	75.10 mV/div	-4.800 mV



Trial 8



Trial 8: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	543.0 ps/div	2.469 ns	175.0 mV/div	1.100 mV

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✓ Lane 2 - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

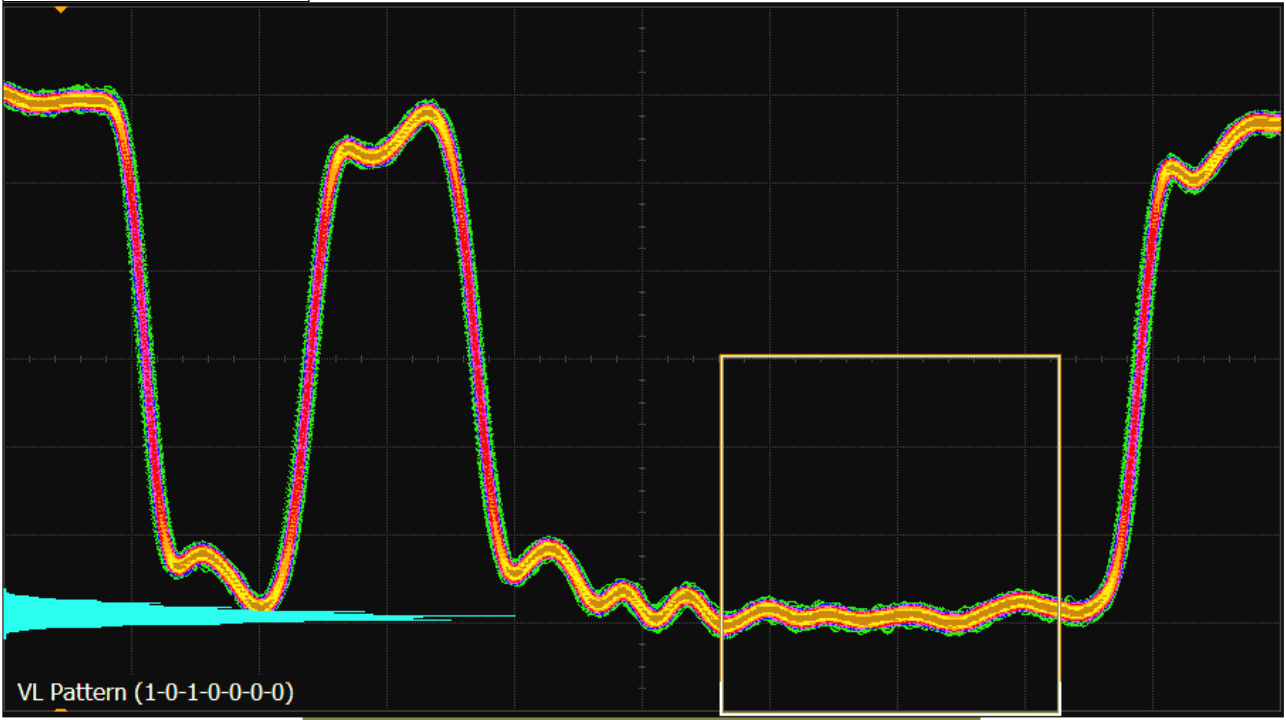
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: <= 250 mdB PreEmphasis(Pre-emphasis 0) (Worst of 8 Trials) -641 mdB # Trials Run: 8 Worst Trial: Trial 8

Overall Summary + details of 8 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-1.170 dB	567.9 %											
	StdDev	445.9 mdB	178.4 %											
	Range	1.095 dB	438.0 %											
	Min	-1.736 dB	356.4 %											
	Max	-641.4 mdB	794.4 %											
	Sum	-9.357 dB	4.543 k%											
✓	Trial 1	-1.528 dB	711.2% (See image)	(See image)	(See image)	1000	695.474 mV	829.219 mV	-1.528 dB	2.7 Gbps	Swing 2 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 2	-1.641 dB	756.4% (See image)	(See image)	(See image)	1000	514.796 mV	621.816 mV	-1.641 dB	2.7 Gbps	Swing 1 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 3	-1.736 dB	794.4% (See image)	(See image)	(See image)	1000	362.682 mV	442.925 mV	-1.736 dB	2.7 Gbps	Swing 0 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 4	-1.386 dB	654.4% (See image)	(See image)	(See image)	1000	853.109 mV	1.000731 V	-1.386 dB	2.7 Gbps	Swing 3 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 5	-767 mdB	406.8% (See image)	(See image)	(See image)	1000	746.089 mV	814.935 mV	-767 mdB	1.62 Gbps	Swing 2 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 6	-852 mdB	440.8% (See image)	(See image)	(See image)	1000	552.960 mV	609.977 mV	-852 mdB	1.62 Gbps	Swing 1 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 7	-806 mdB	422.4% (See image)	(See image)	(See image)	1000	385.586 mV	423.088 mV	-806 mdB	1.62 Gbps	Swing 0 0	Pre-emphasis 0	SSC Disabled	Level 0
✓	Trial 8 (Worst)	-641 mdB	356.4% (See image)	(See image)	(See image)	1000	925.083 mV	995.978 mV	-641 mdB	1.62 Gbps	Swing 3 0	Pre-emphasis 0	SSC Disabled	Level 0

Trial 1

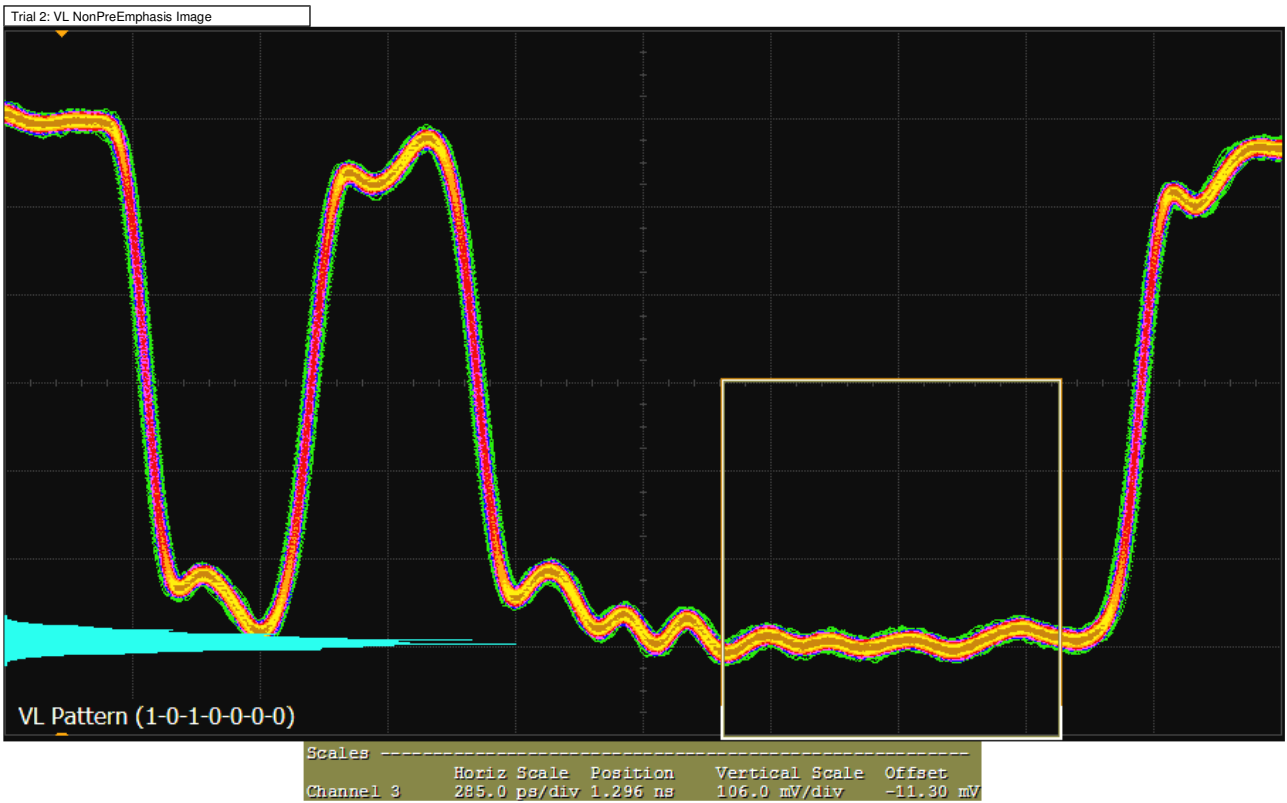
Trial 1: VL NonPreEmphasis Image

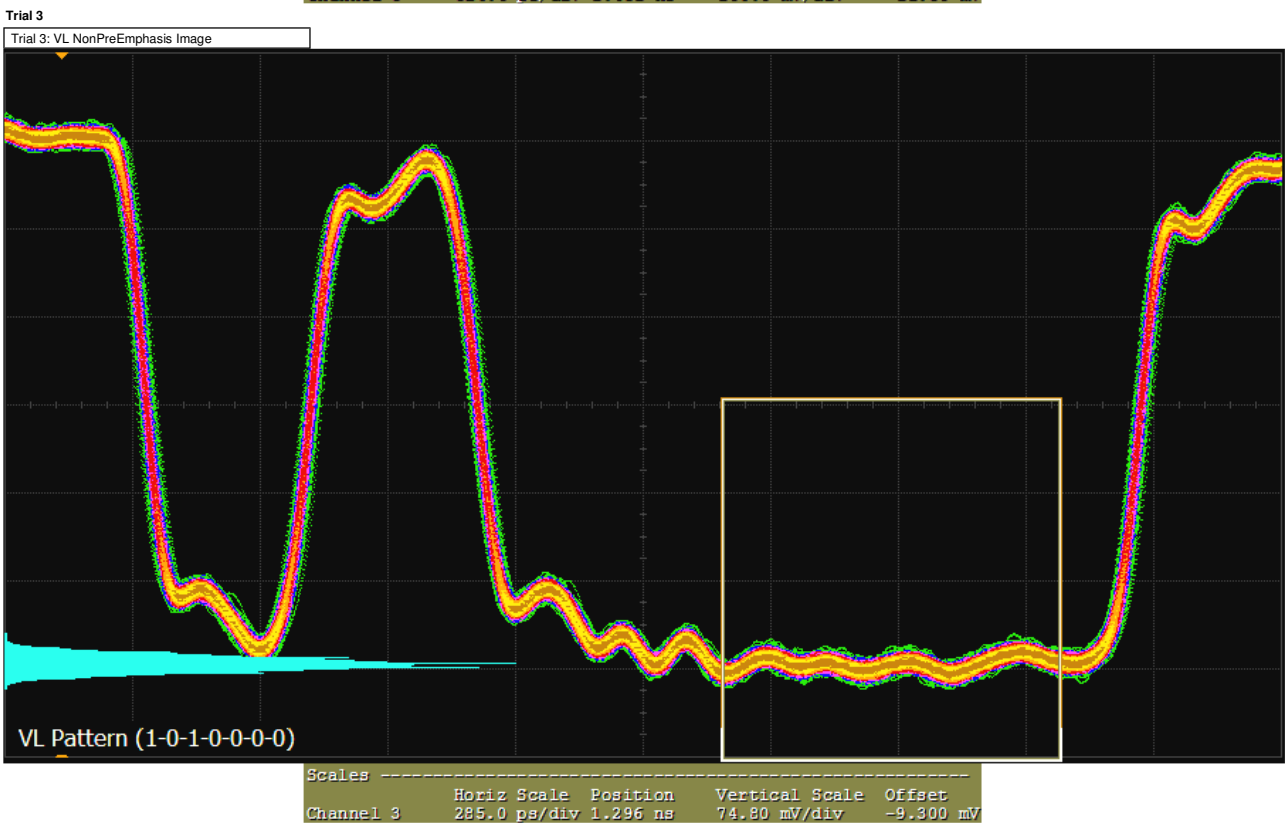


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	285.0 ps/div	1.296 ns	141.0 mV/div	-8.400 mV



Trial 2





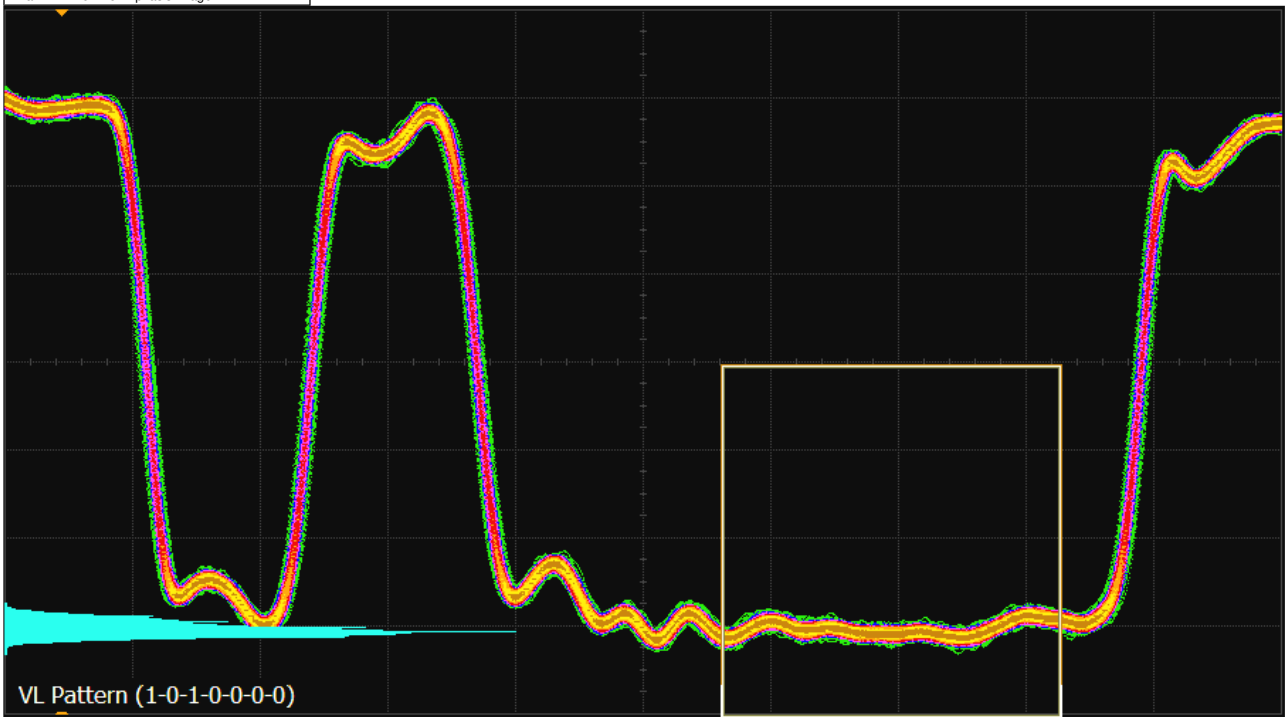
Trial 3: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	326.0 ps/div	1.492 ns	74.80 mV/div	-9.300 mV

Trial 4

Trial 4: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	285.0 ps/div	1.296 ns	171.0 mV/div	-3.400 mV

Trial 4: VH NonPreEmphasis Image

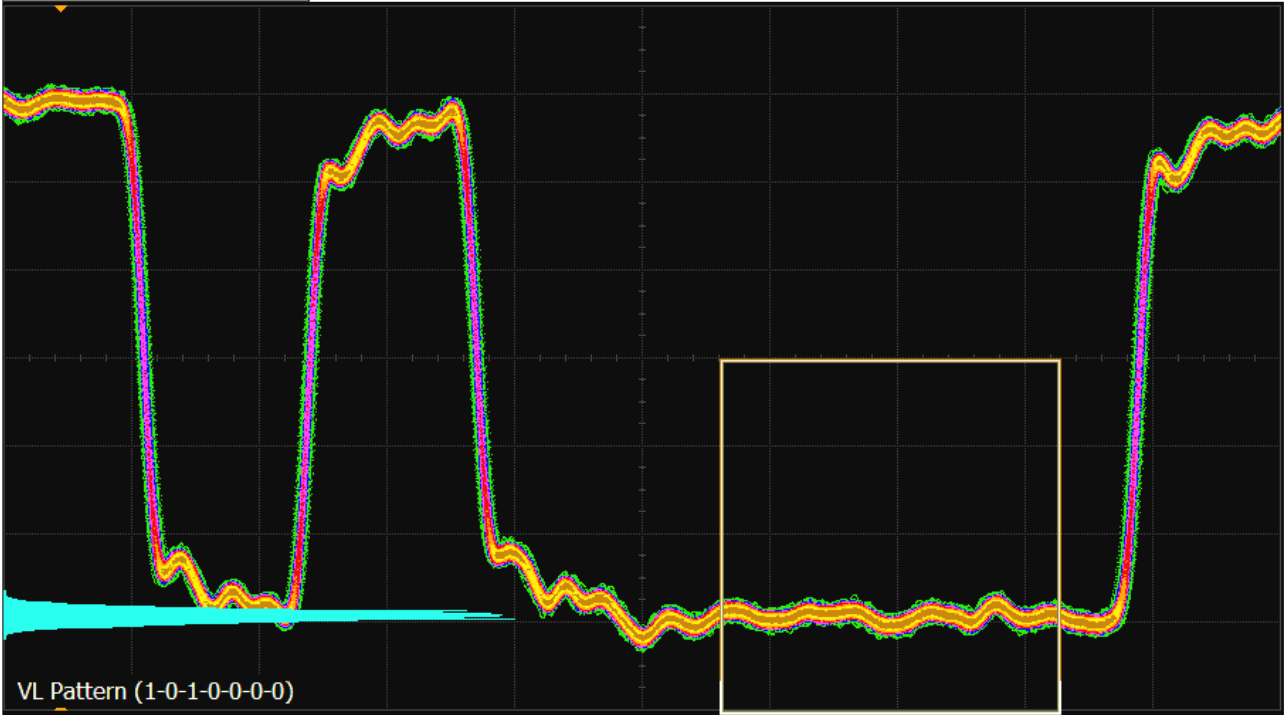


VH Pattern (1-0-1-1-1-1-1-1)

Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	326.0 ps/div	1.492 ns	171.0 mV/div	-3.400 mV

Trial 5

Trial 5: VL NonPreEmphasis Image



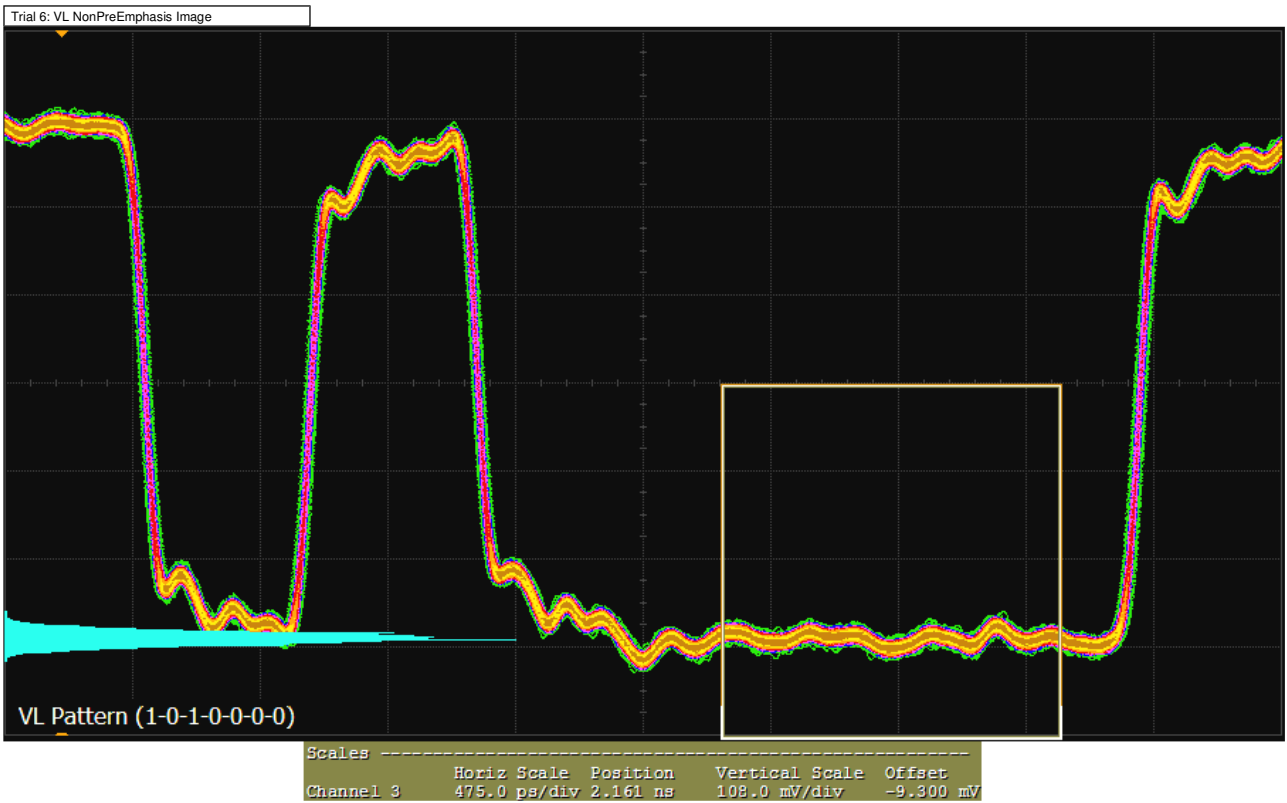
VL Pattern (1-0-1-0-0-0-0)

Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	145.0 mV/div	-700.0 $\mu$ V





Trial 6



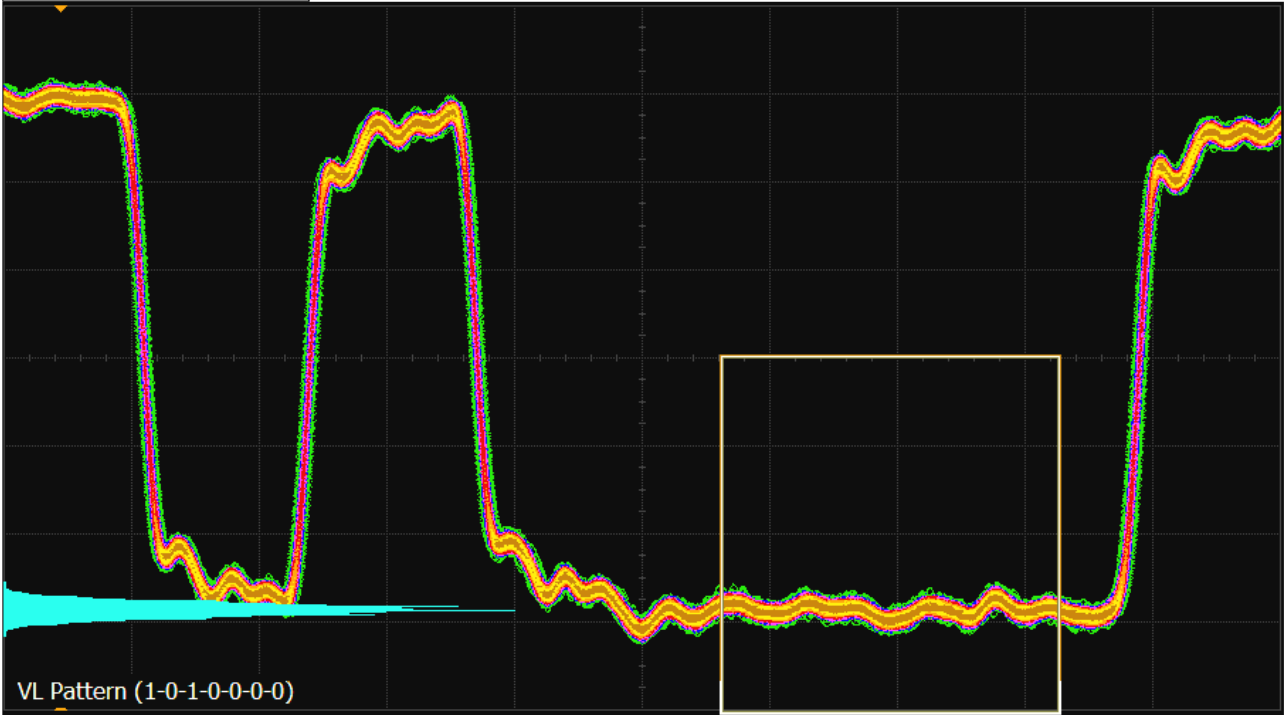
Trial 6: VH NonPreEmphasis Image



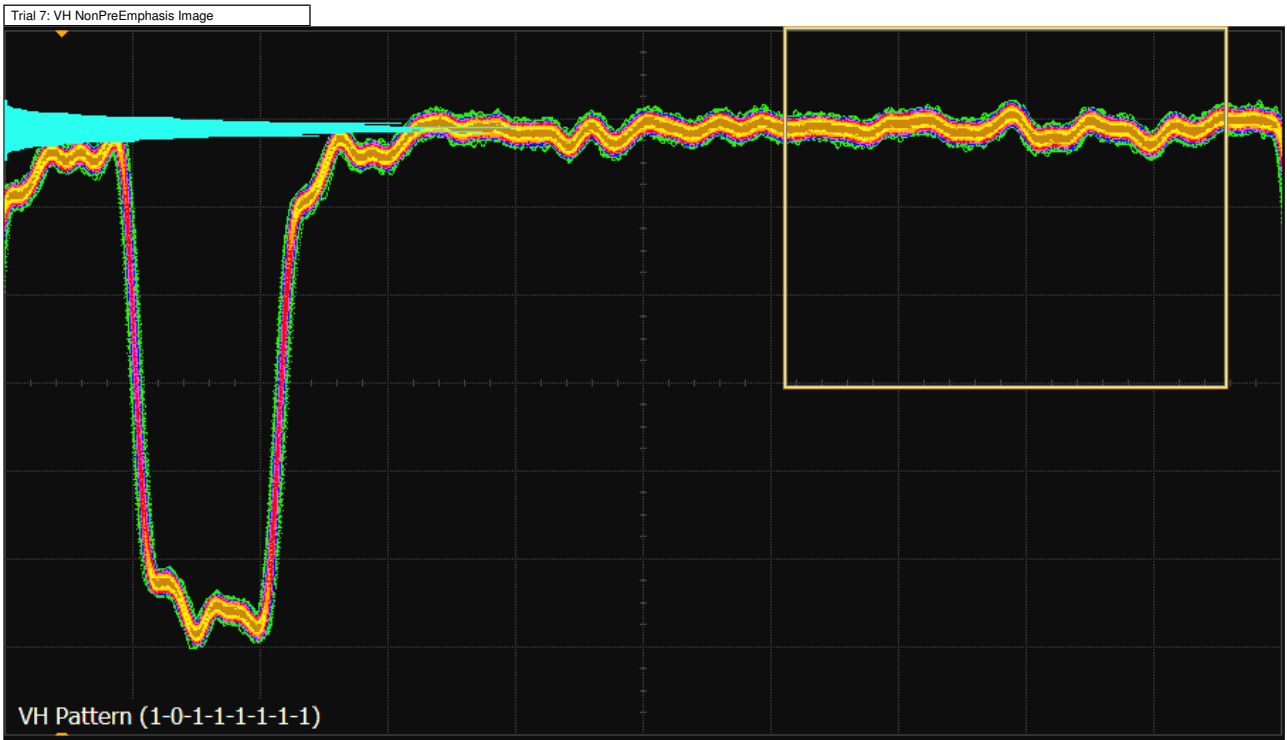
Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	543.0 ps/div	2.469 ns	108.0 mV/div	-9.300 mV

Trial 7

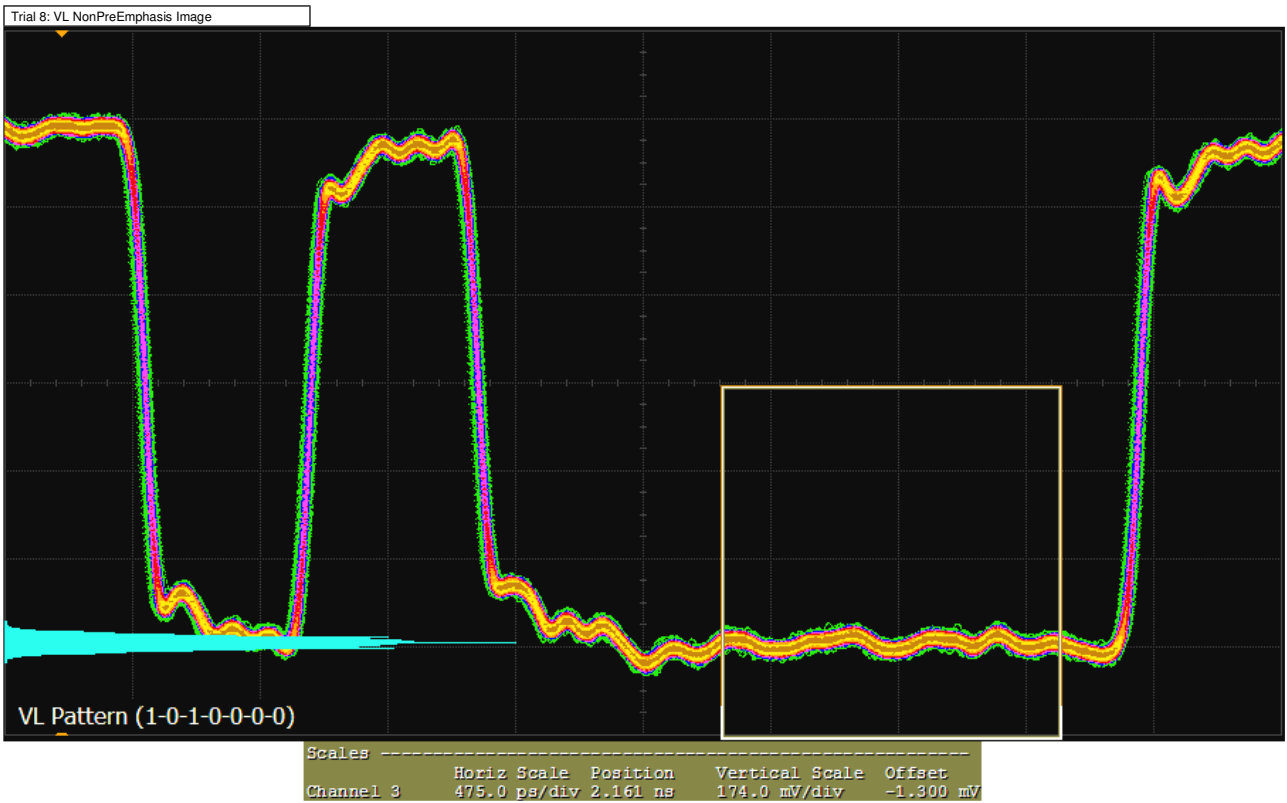
Trial 7: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	73.40 mV/div	-11.30 mV



Trial 8



Trial 8: VH NonPreEmphasis Image



Scales				
	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	543.0 ps/div	2.469 ns	174.0 mV/div	-1.300 mV

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✔ Lane 3 - Pre-Emphasis Level Test (Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass    Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

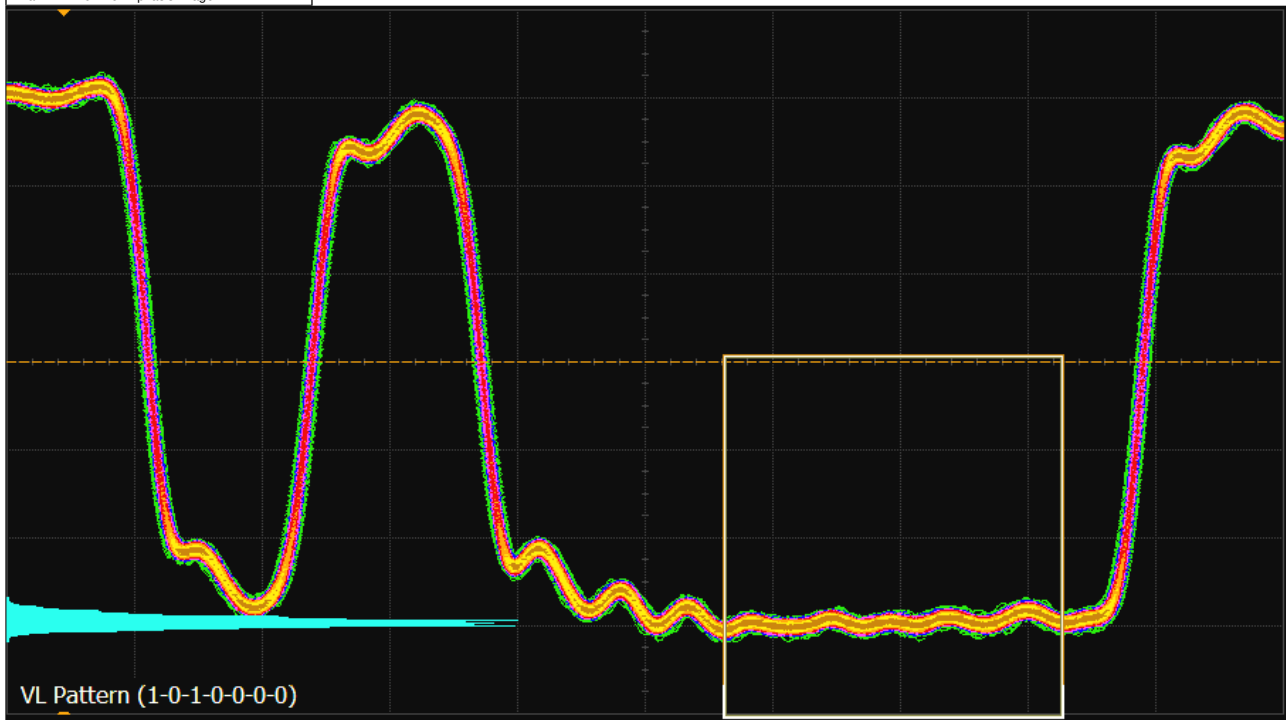
Pass Limits: <= 250 mdB    PreEmphasis(Pre-emphasis 0) (Worst of 8 Trials) -727 mdB    # Trials Run: 8    Worst Trial: Trial 8

Overall Summary + details of 8 worst trials

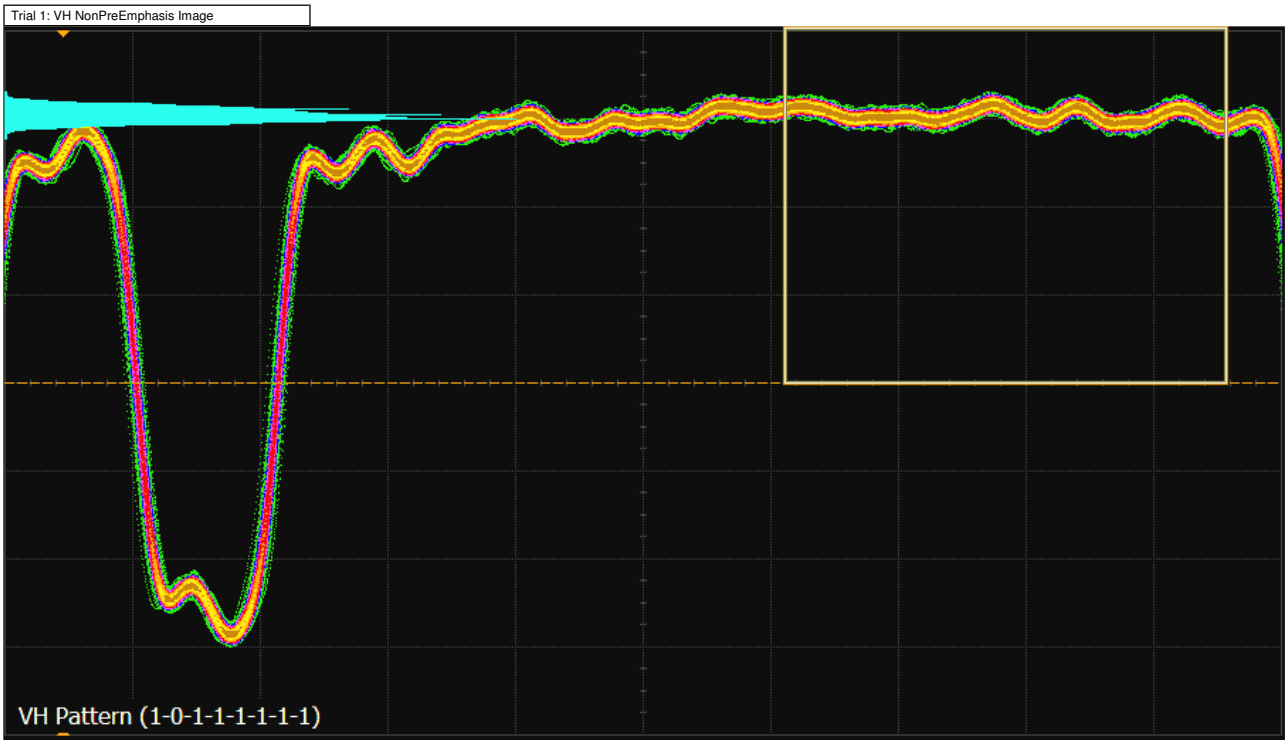
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VH NonPreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	<i>-1.088 dB</i>	<i>535.3 %</i>											
	<i>StdDev</i>	<i>255.7 mdB</i>	<i>102.3 %</i>											
	<i>Range</i>	<i>713.6 mdB</i>	<i>285.2 %</i>											
	<i>Min</i>	<i>-1.440 dB</i>	<i>390.8 %</i>											
	<i>Max</i>	<i>-726.9 mdB</i>	<i>676.0 %</i>											
	<i>Sum</i>	<i>-8.706 dB</i>	<i>4.282 k%</i>											
✔	Trial 1	-1.255 dB	602.0% (See image)	(See image)	(See image)	1000	705.712 mV	815.375 mV	-1.255 dB	2.7 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 2	-1.399 dB	659.6% (See image)	(See image)	(See image)	1000	510.985 mV	600.309 mV	-1.399 dB	2.7 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 3	-1.440 dB	676.0% (See image)	(See image)	(See image)	1000	354.068 mV	417.935 mV	-1.440 dB	2.7 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 4	-1.079 dB	531.6% (See image)	(See image)	(See image)	1000	899.368 mV	1.018339 V	-1.079 dB	2.7 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 5	-862 mdB	444.8% (See image)	(See image)	(See image)	1000	737.290 mV	814.248 mV	-862 mdB	1.62 Gbps	Swing 2	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 6	-957 mdB	482.8% (See image)	(See image)	(See image)	1000	534.680 mV	596.950 mV	-957 mdB	1.62 Gbps	Swing 1	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 7	-986 mdB	494.4% (See image)	(See image)	(See image)	1000	370.512 mV	415.061 mV	-986 mdB	1.62 Gbps	Swing 0	Pre-emphasis 0	SSC Disabled	Level 0
✔	Trial 8 (Worst)	-727 mdB	390.8% (See image)	(See image)	(See image)	1000	929.405 mV	1.010531 V	-727 mdB	1.62 Gbps	Swing 3	Pre-emphasis 0	SSC Disabled	Level 0

Trial 1

Trial 1: VL NonPreEmphasis Image



Scales				
Channel	Horiz Scale	Position	Vertical Scale	Offset
4	285.0 ps/div	1.296 ns	137.0 mV/div	-17.90 mV

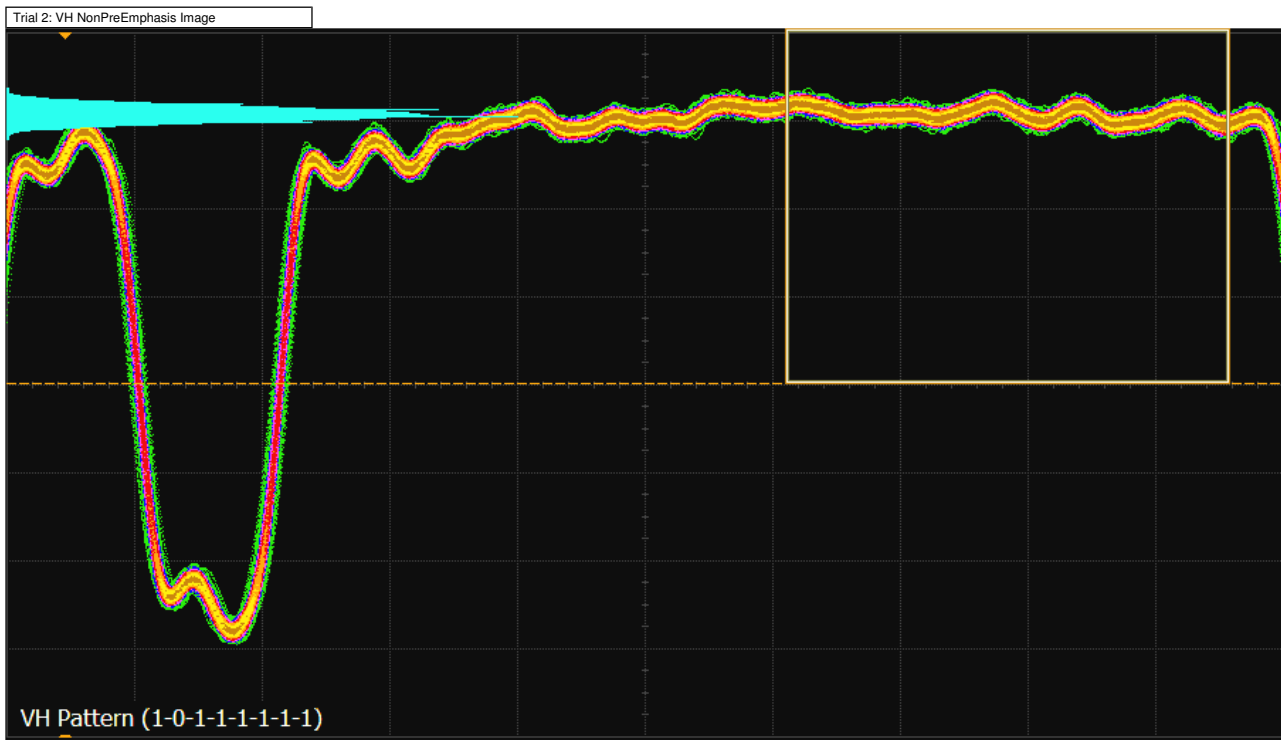


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	326.0 ps/div	1.482 ns	137.0 mV/div	-17.90 mV

Trial 2



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	285.0 ps/div	1.296 ns	102.0 mV/div	-17.30 mV



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	326.0 ps/div	1.482 ns	102.0 mV/div	-17.80 mV

Trial 3

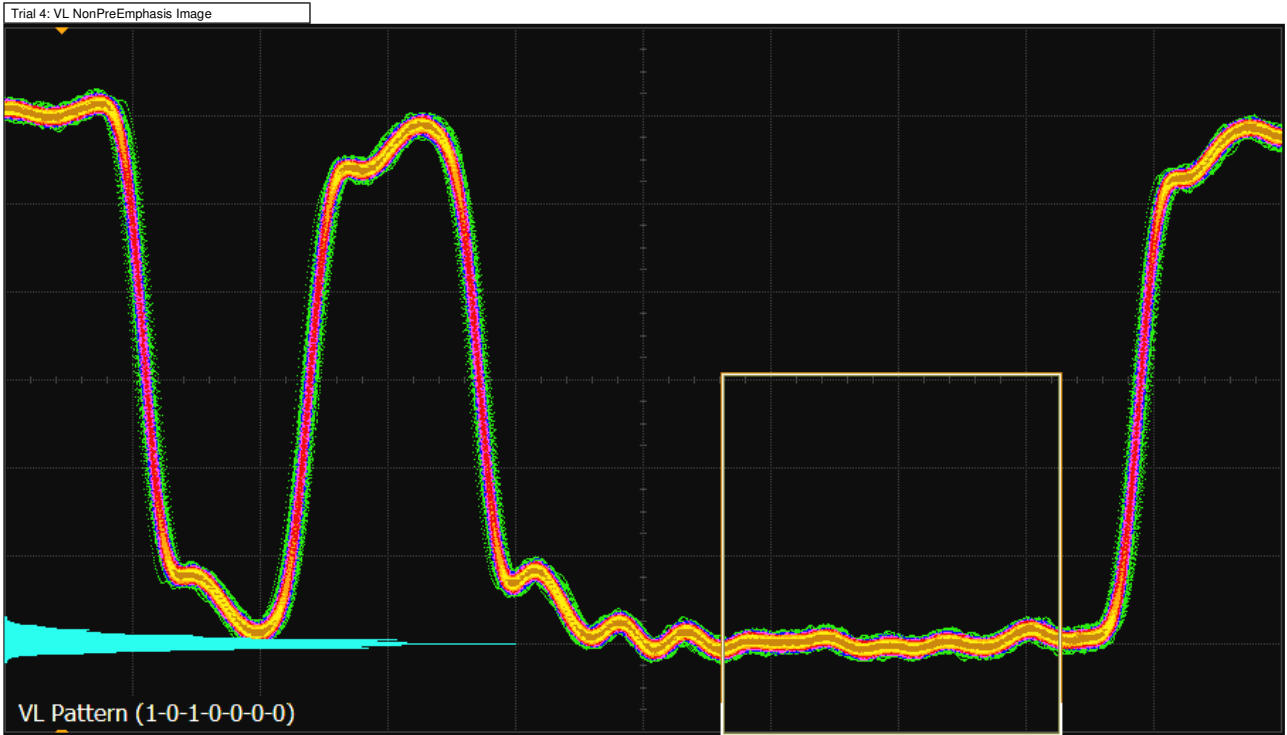


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	285.0 ps/div	1.296 ns	72.40 mV/div	-14.00 mV



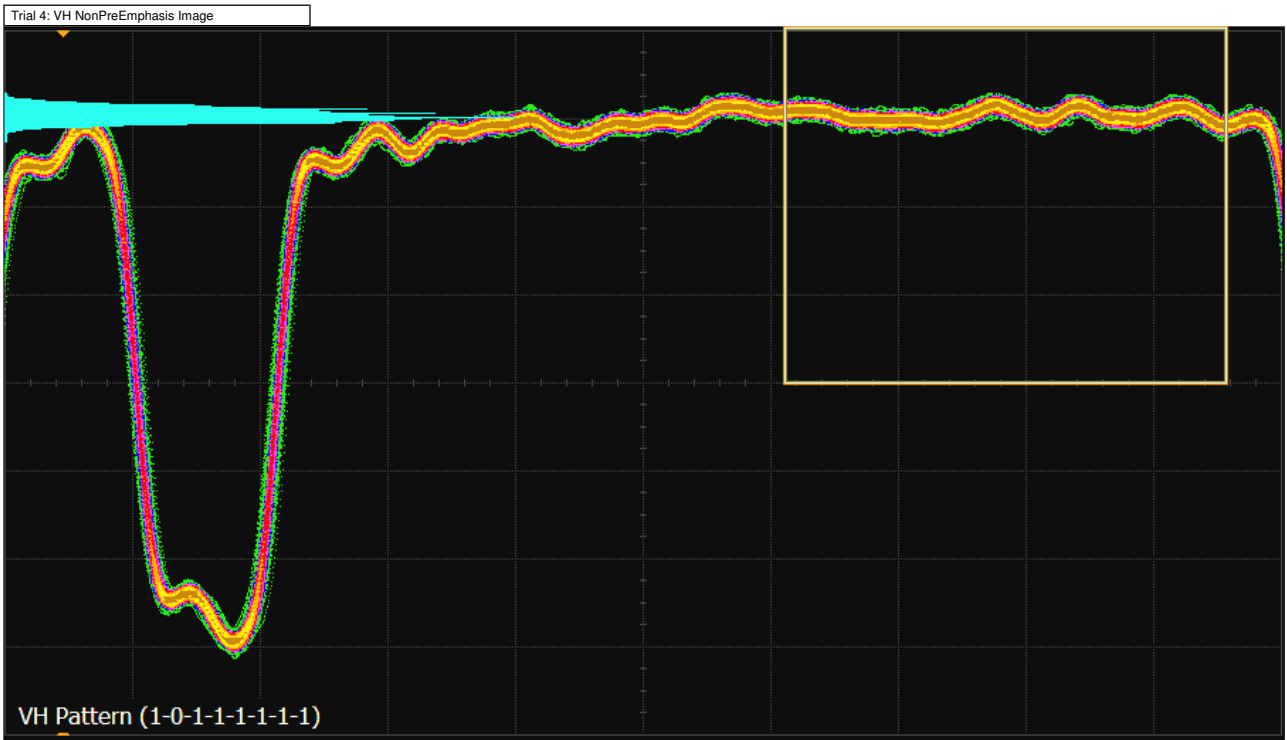
Scales				
Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	326.0 ps/div	1.481 ns	72.40 mV/div	-14.00 mV

Trial 4



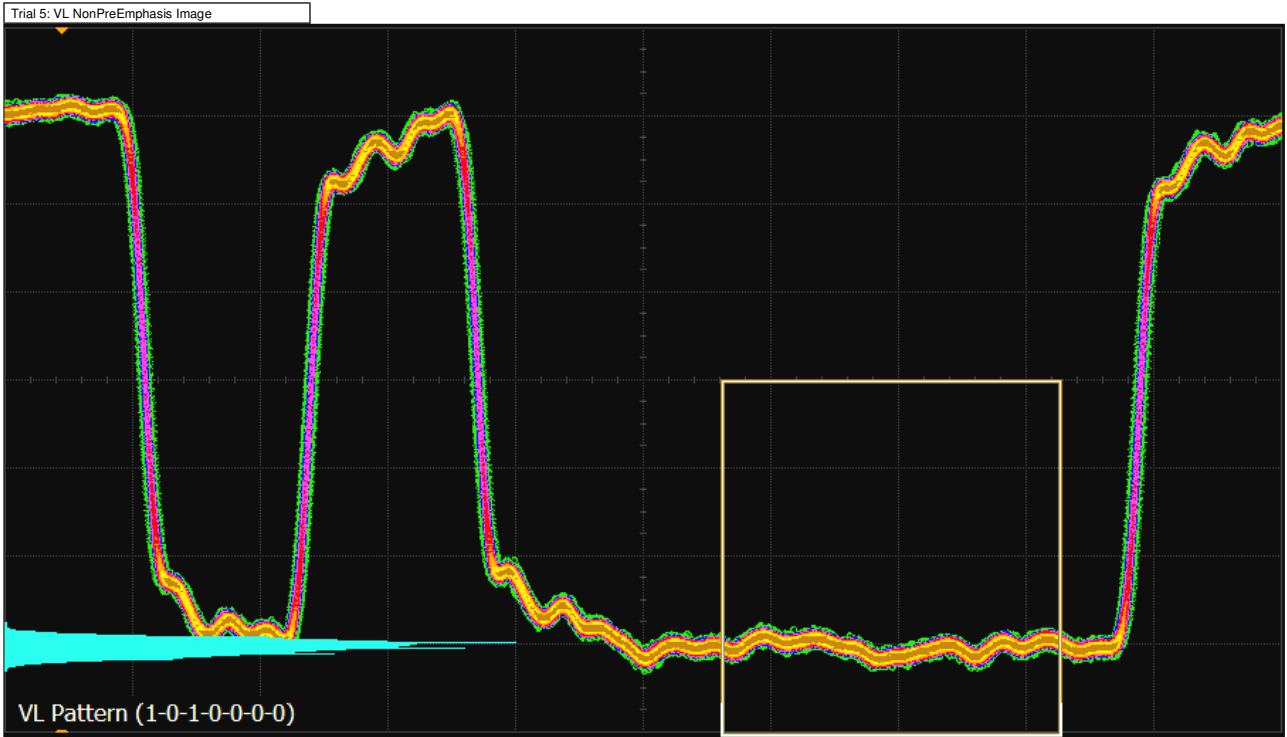
Scales				
Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	285.0 ps/div	1.296 ns	169.0 mV/div	-22.90 mV





Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	326.0 ps/div	1.481 ns	169.0 mV/div	-22.90 mV

Trial 5



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	475.0 ps/div	2.161 ns	137.0 mV/div	-10.60 mV

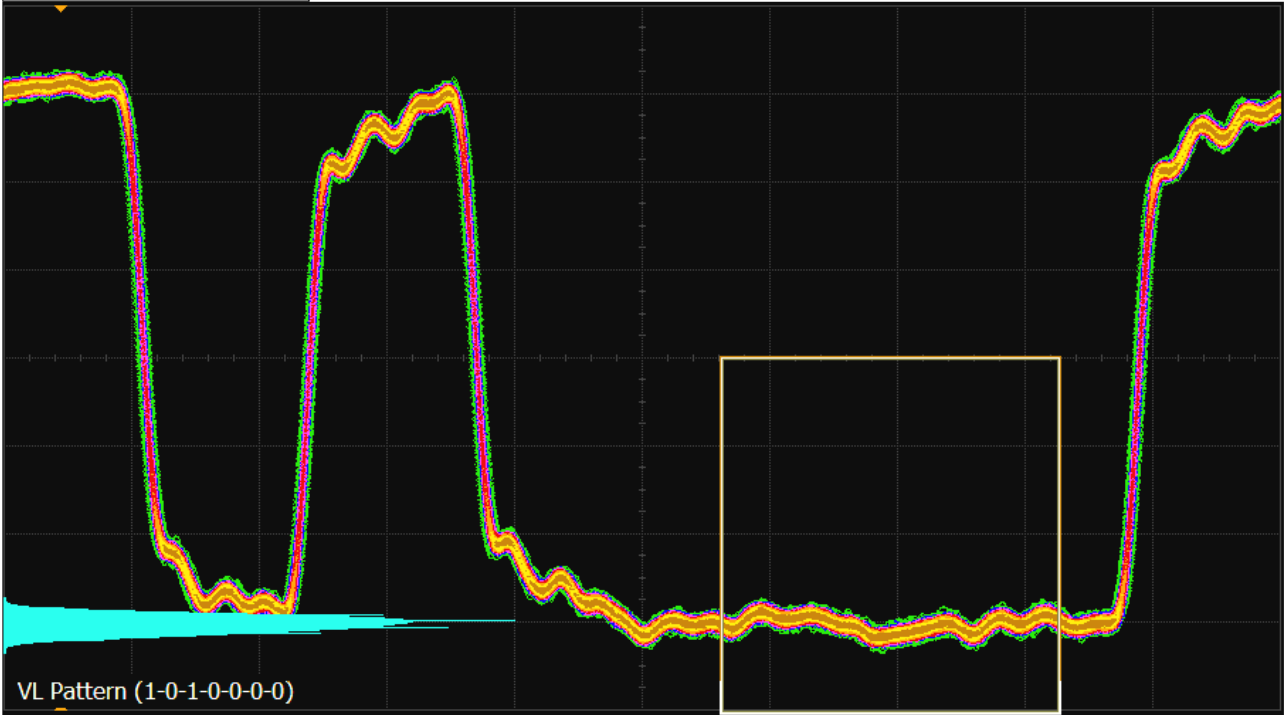
Trial 5: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	543.0 ps/div	2.469 ns	137.0 mV/div	-10.60 mV

Trial 6

Trial 6: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	475.0 ps/div	2.161 ns	101.0 mV/div	-10.70 mV

Trial 6: VH NonPreEmphasis Image

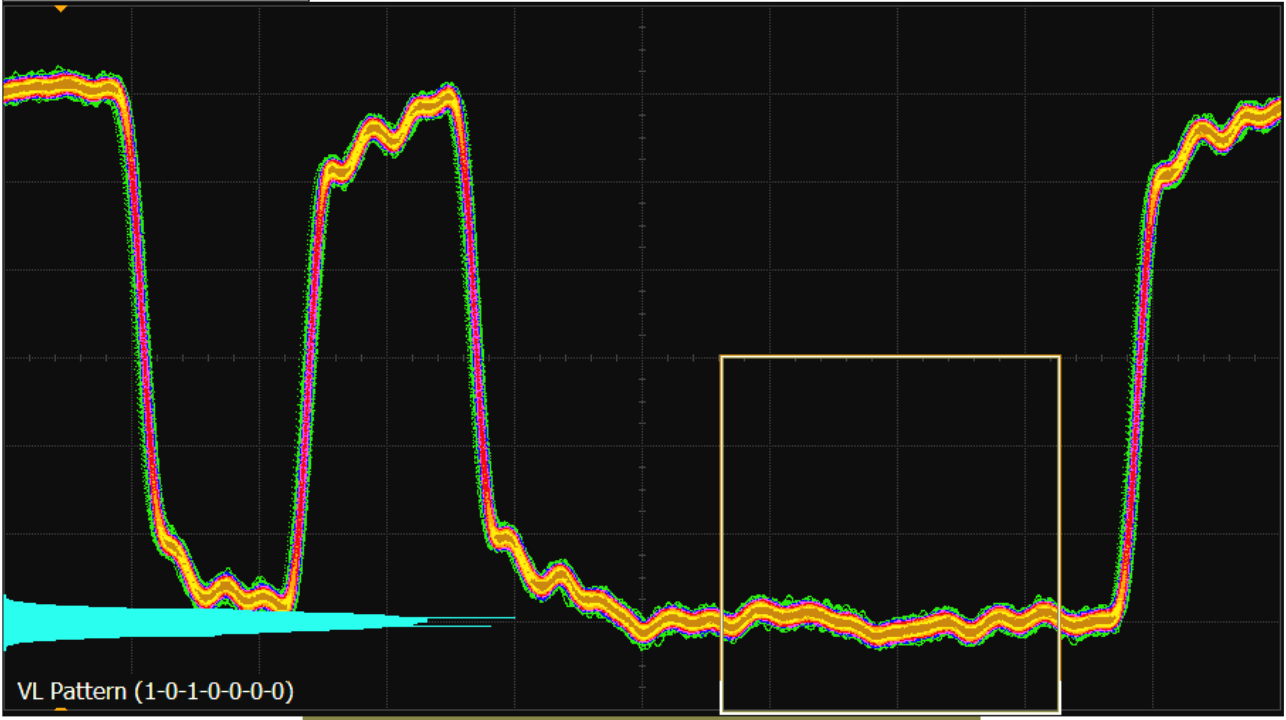


VH Pattern (1-0-1-1-1-1-1)

Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	543.0 ps/div	2.469 ns	101.0 mV/div	-10.70 mV

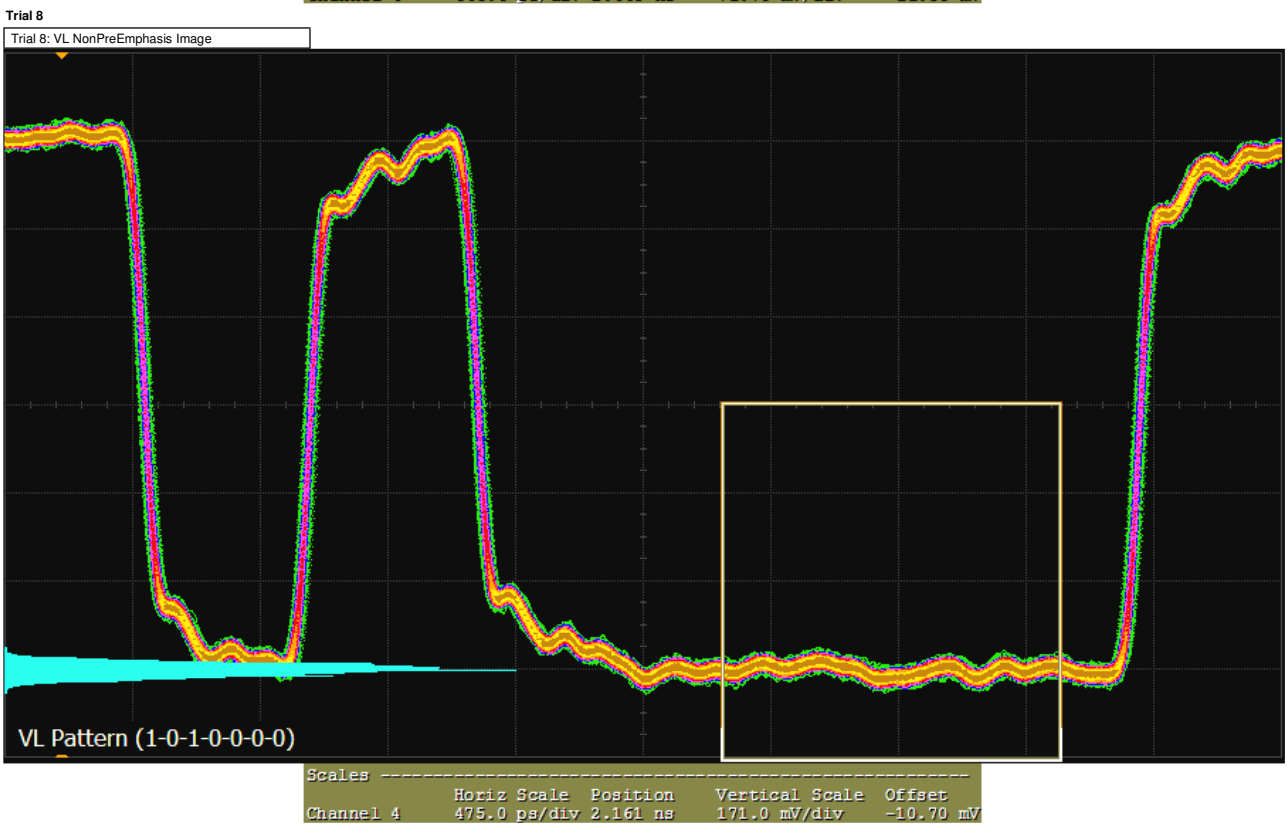
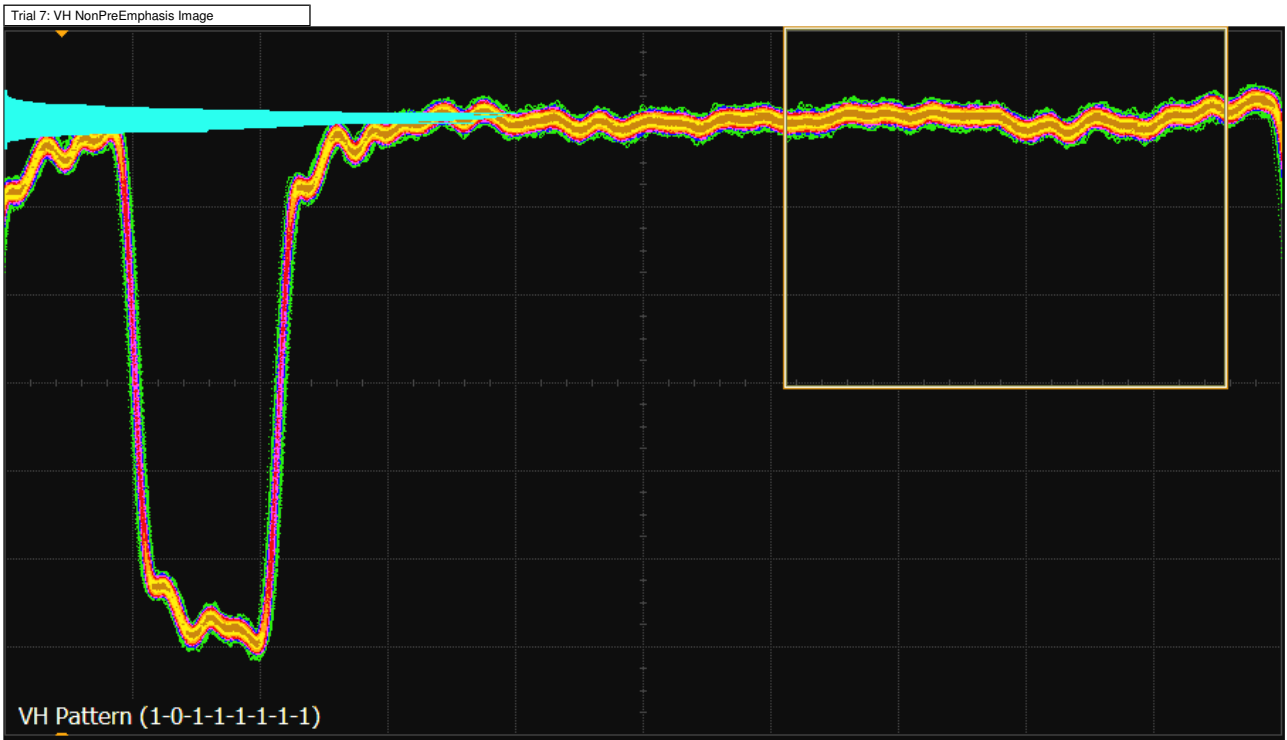
Trial 7

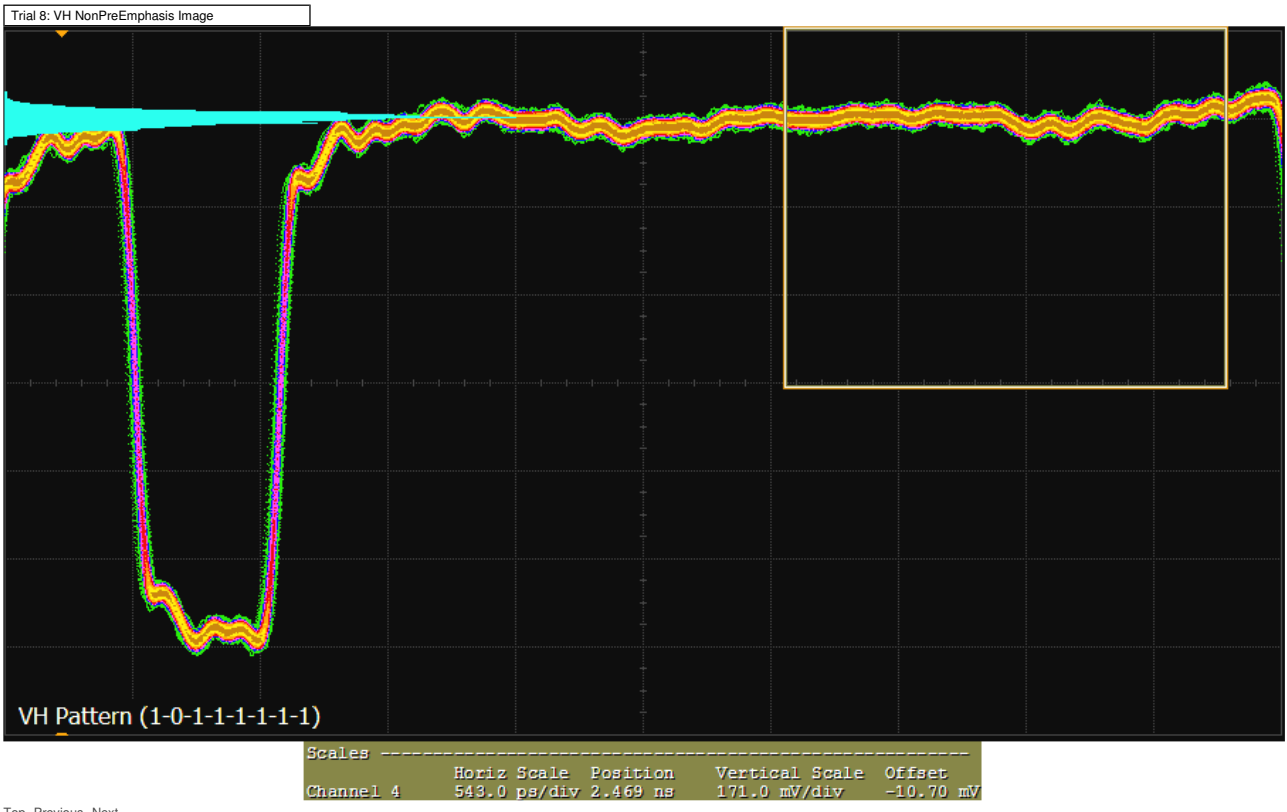
Trial 7: VL NonPreEmphasis Image



VL Pattern (1-0-1-0-0-0-0)

Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	475.0 ps/div	2.161 ns	71.70 mV/div	-11.90 mV





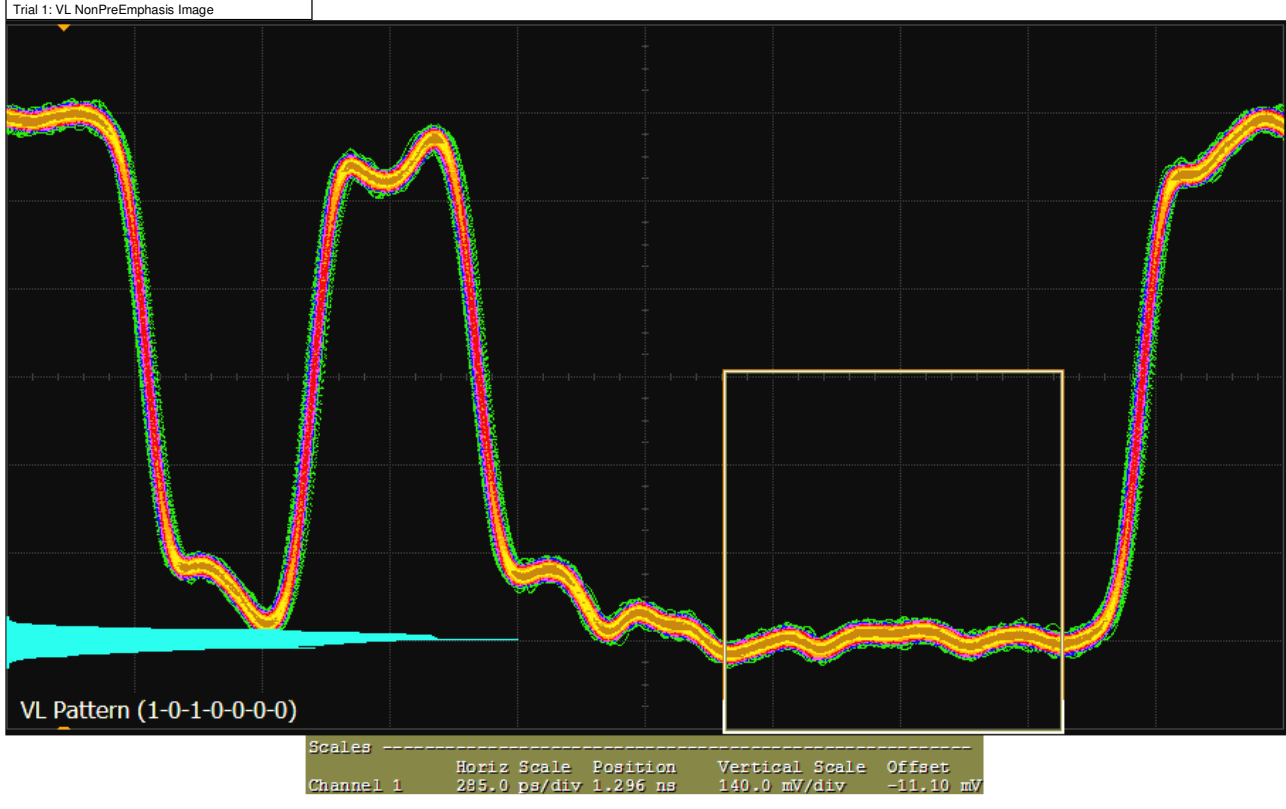
✓ Lane 0 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

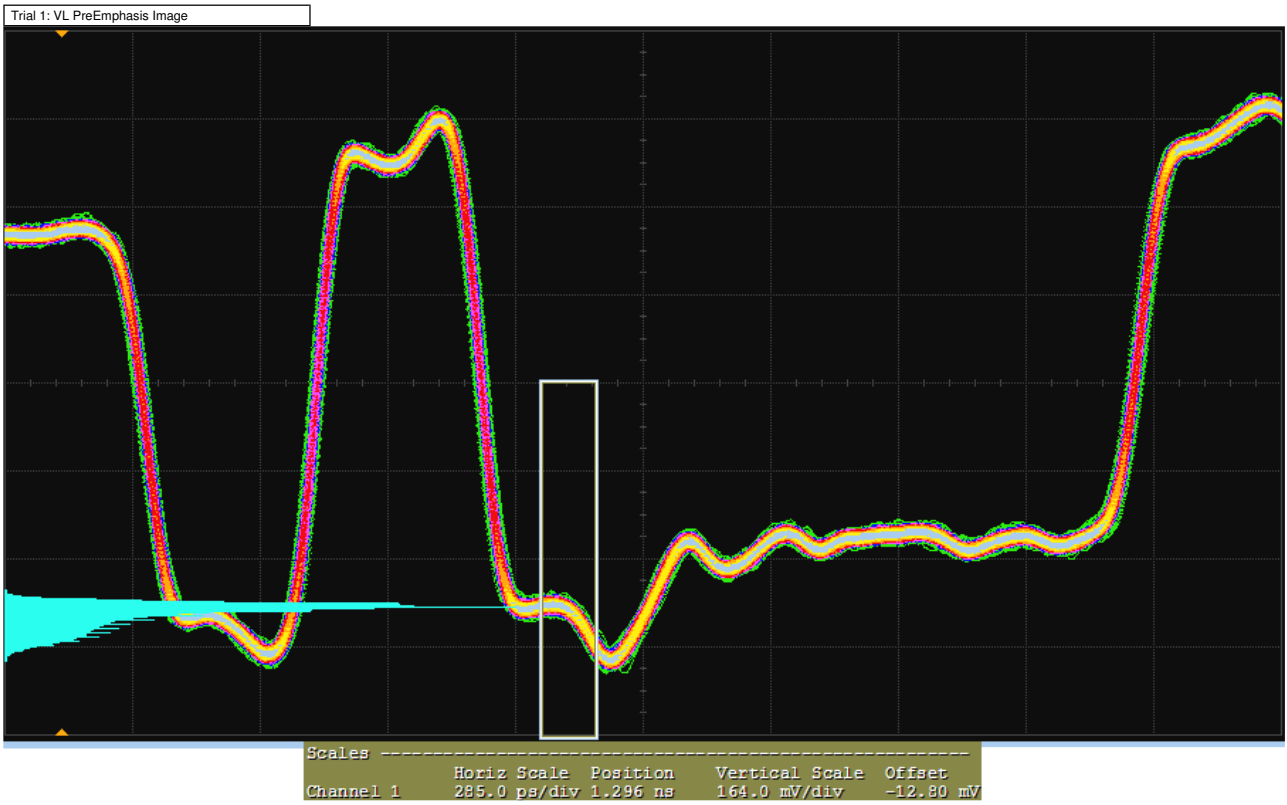
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 2.000 dB | PreEmphasis (Pre-emphasis 1) (Worst of 6 Trials) 5.253 dB | # Trials Run: 6 | Worst Trial: Trial 1

Overall Summary + details of 6 worst trials

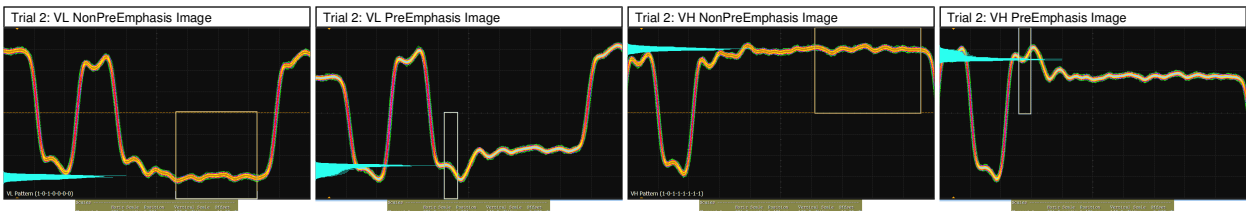
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	5.519 dB	175.9 %													
	StdDev	210.9 mdB	10.54 %													
	Range	566.2 mdB	28.30 %													
	Min	5.253 dB	162.7 %													
	Max	5.819 dB	191.0 %													
	Sum	33.11 dB	1.056 k%													
✓	Trial 1 (Worst)	5.253 dB	162.7% (See image)	(See image)	(See image)	(See image)	(See image)	1000	878.642 mV	596.851 mV	3.359 dB	2.7 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 2	5.528 dB	176.4% (See image)	(See image)	(See image)	(See image)	(See image)	1000	747.753 mV	499.512 mV	3.504 dB	2.7 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 3	5.606 dB	180.3% (See image)	(See image)	(See image)	(See image)	(See image)	1000	527.867 mV	351.082 mV	3.542 dB	2.7 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 4	5.303 dB	165.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	1.016644 V	591.239 mV	4.708 dB	1.62 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 5	5.603 dB	180.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	872.906 mV	493.028 mV	4.962 dB	1.62 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 6	5.819 dB	191.0% (See image)	(See image)	(See image)	(See image)	(See image)	1000	619.112 mV	344.096 mV	5.102 dB	1.62 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0

Trial 1

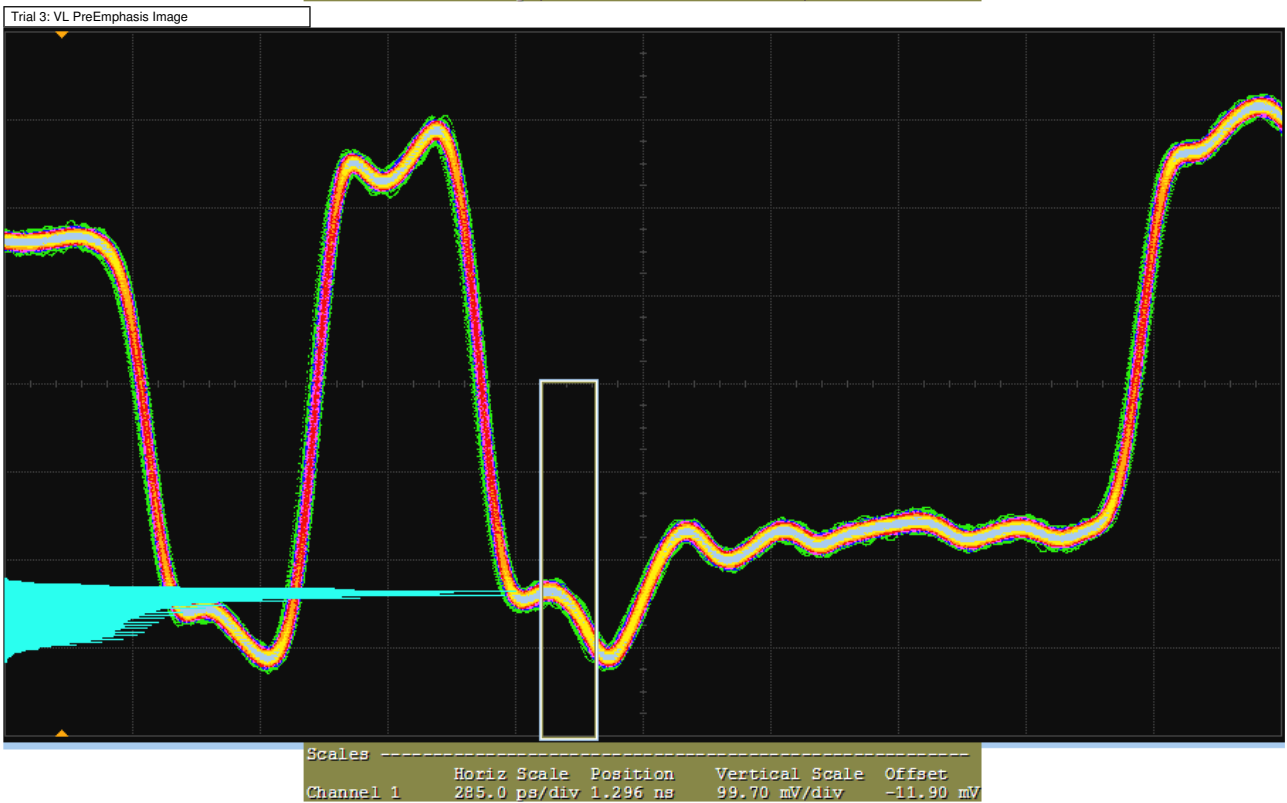
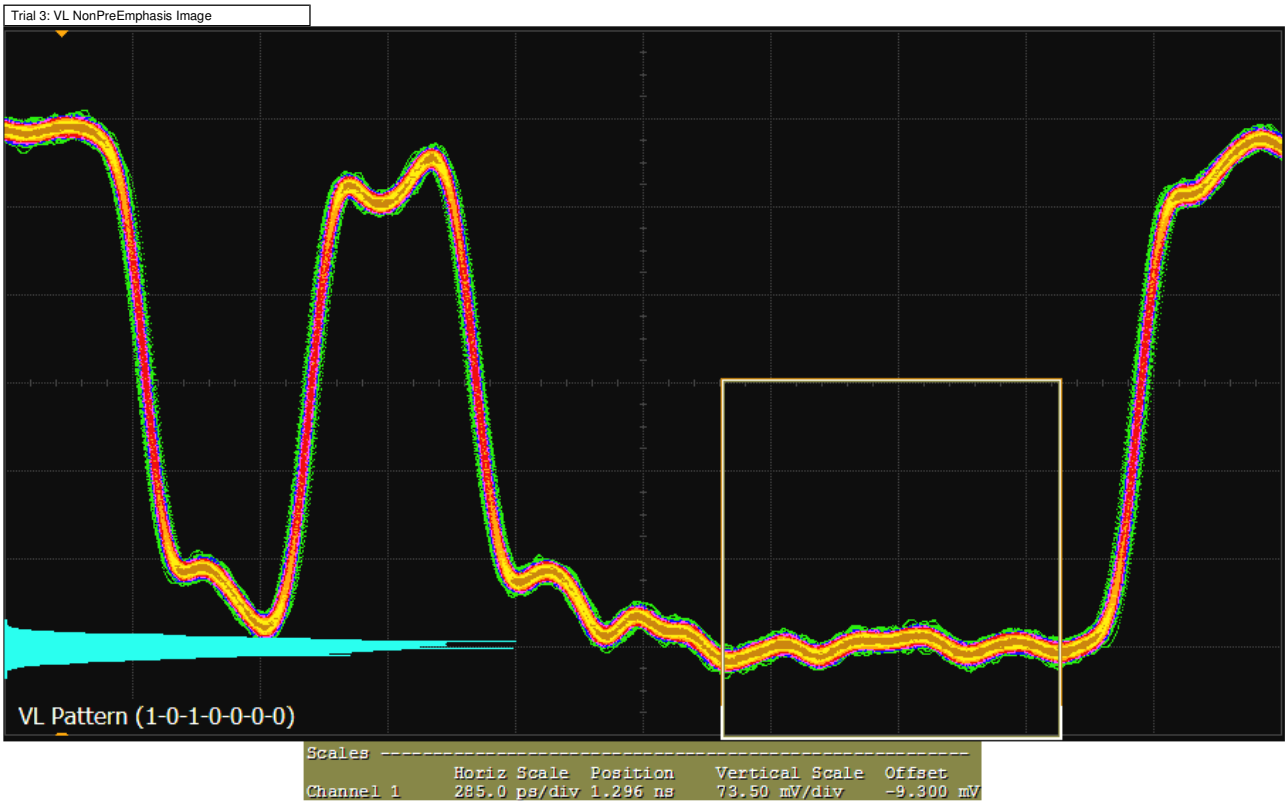




Trial 2



Trial 3

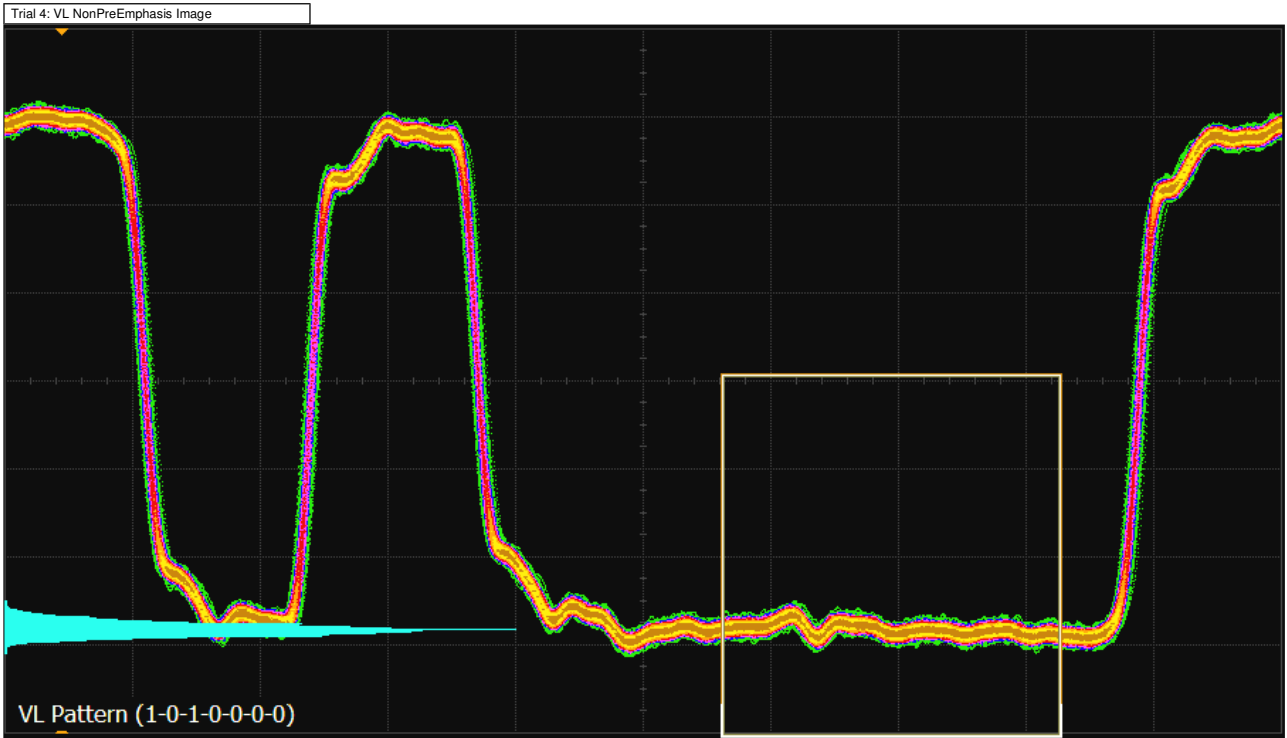




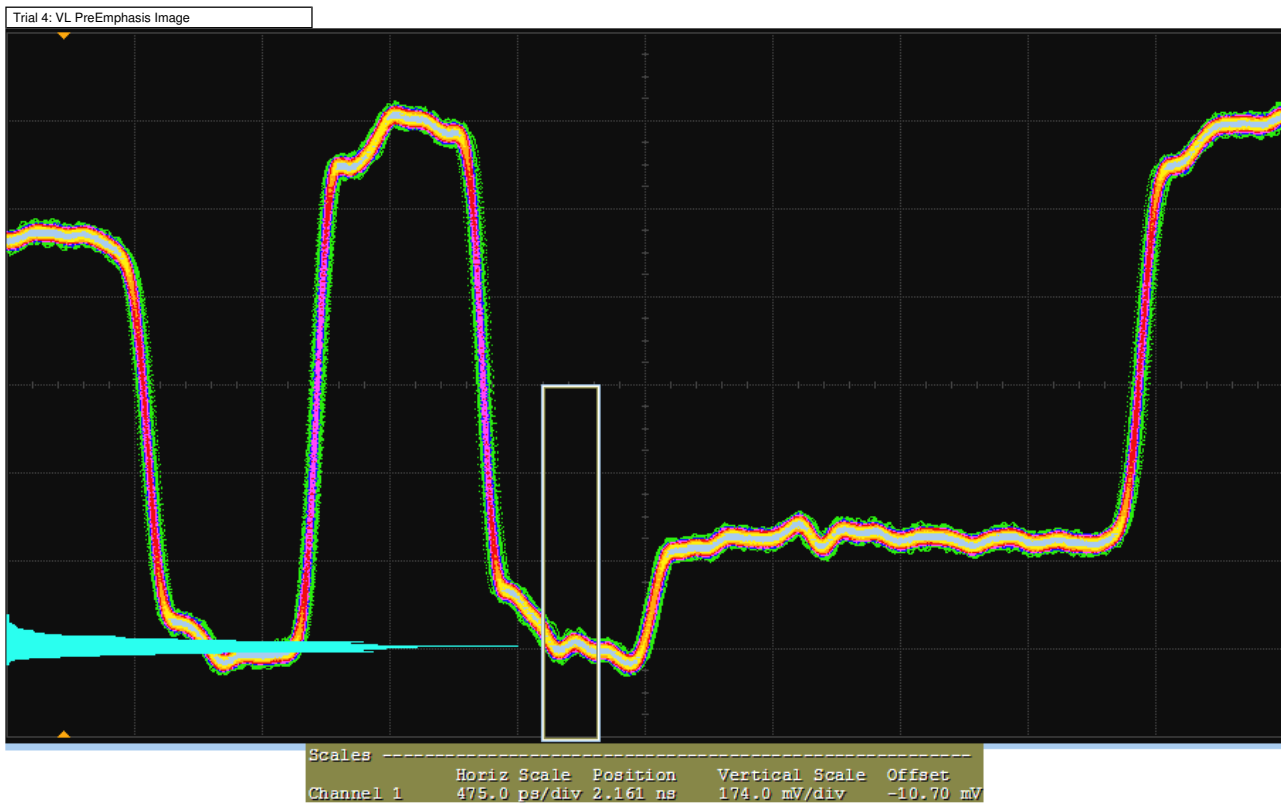


Scales				
	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	326.0 ps/div	1.482 ns	73.50 mV/div	-9.300 mV

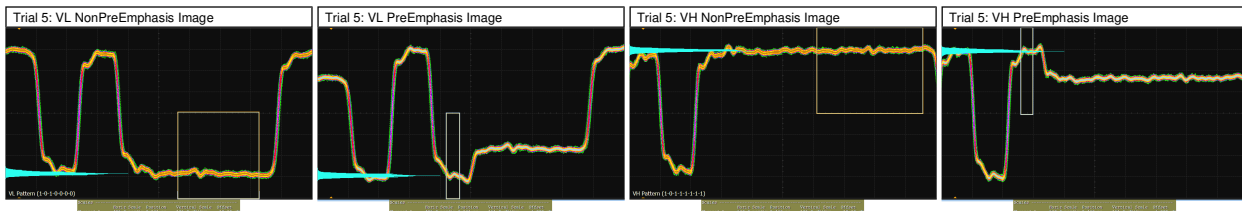
Trial 4



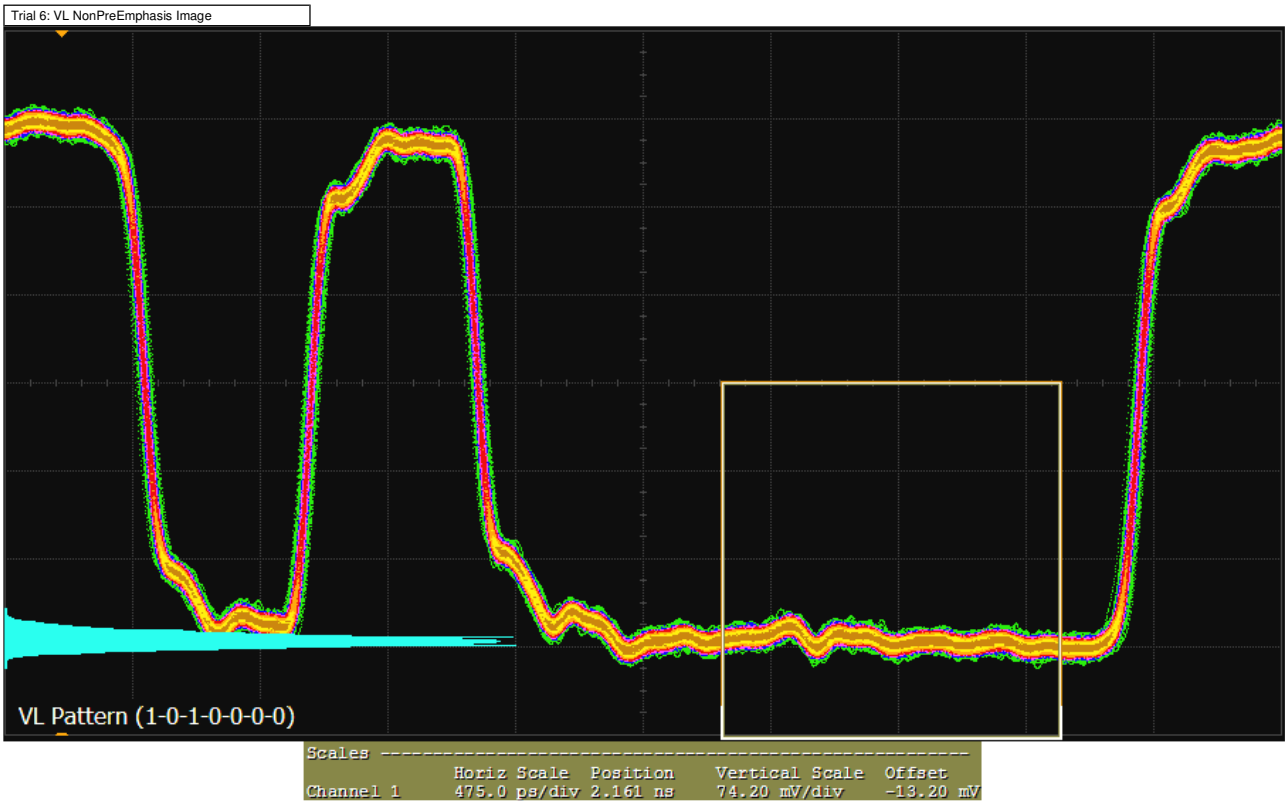
Scales				
	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	475.0 ps/div	2.161 ns	143.0 mV/div	-14.80 mV

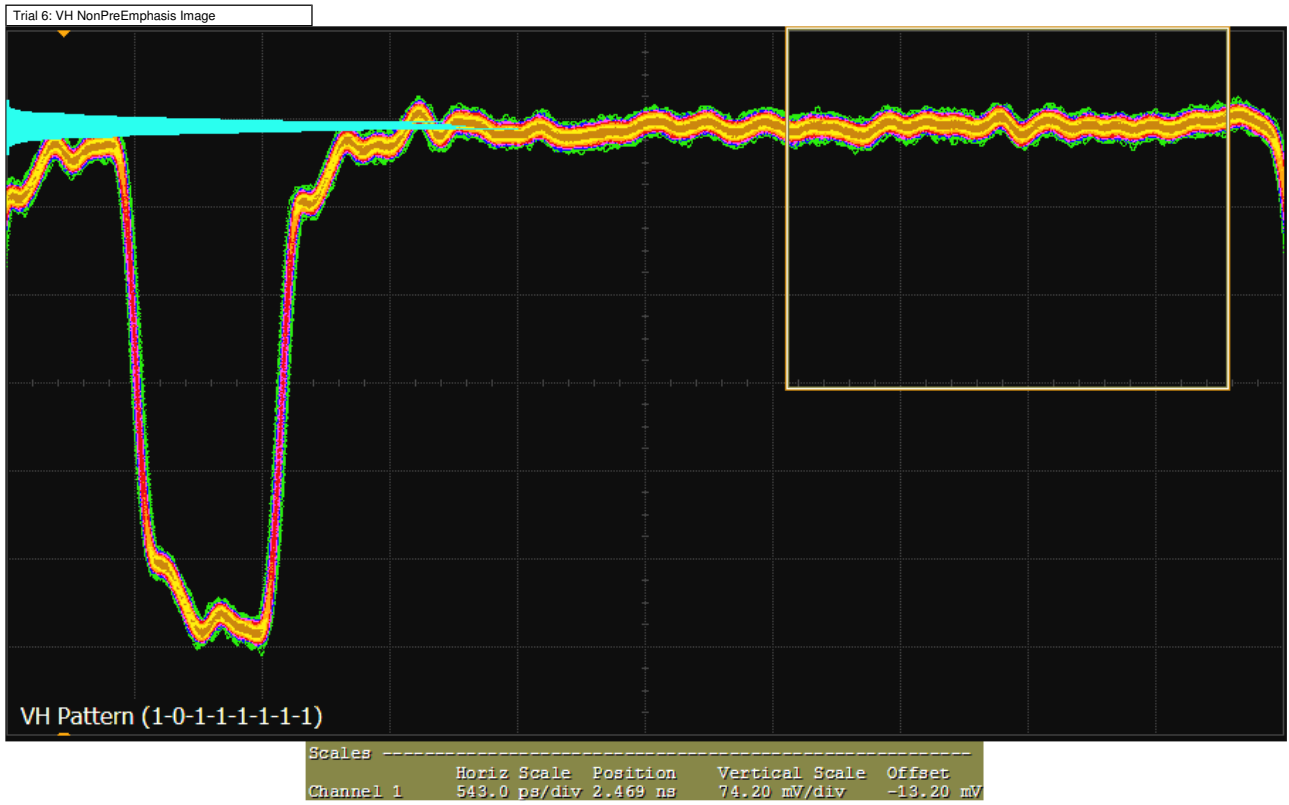


Trial 5



Trial 6





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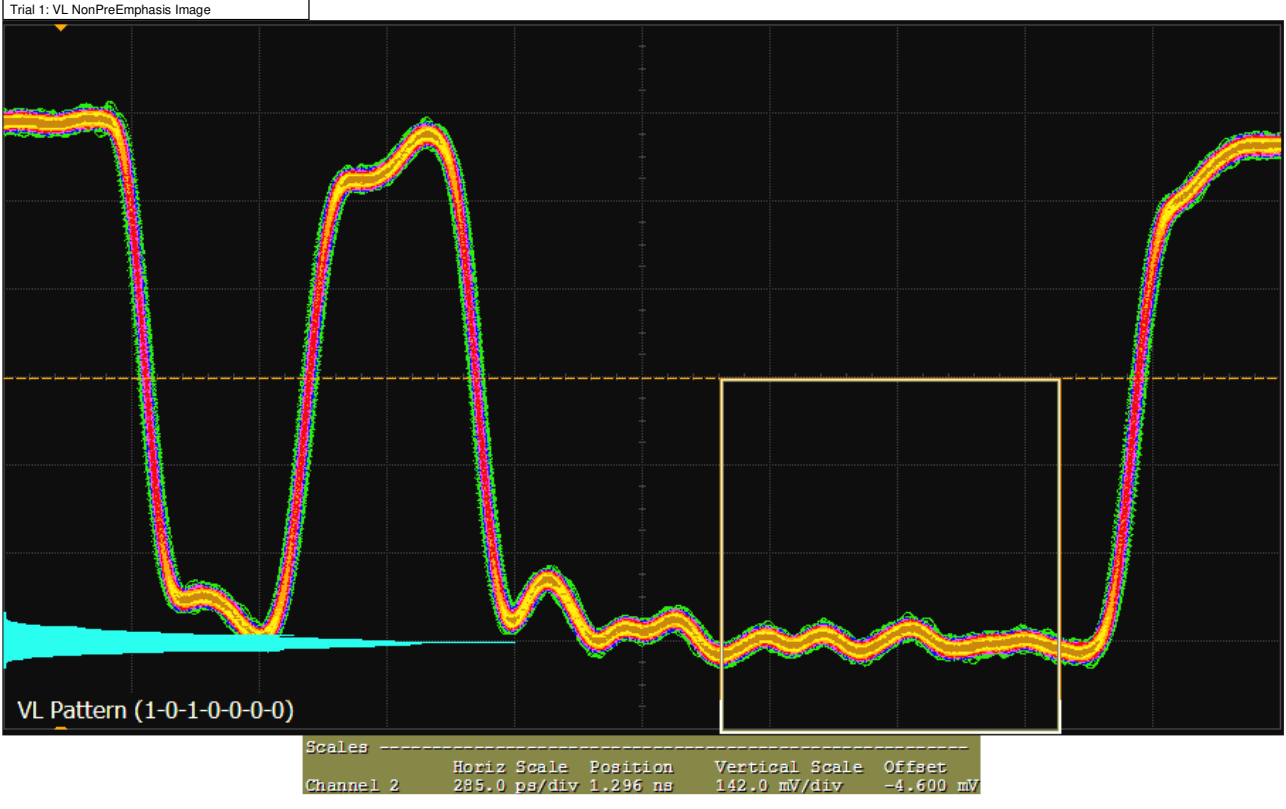
**X Lane 1 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

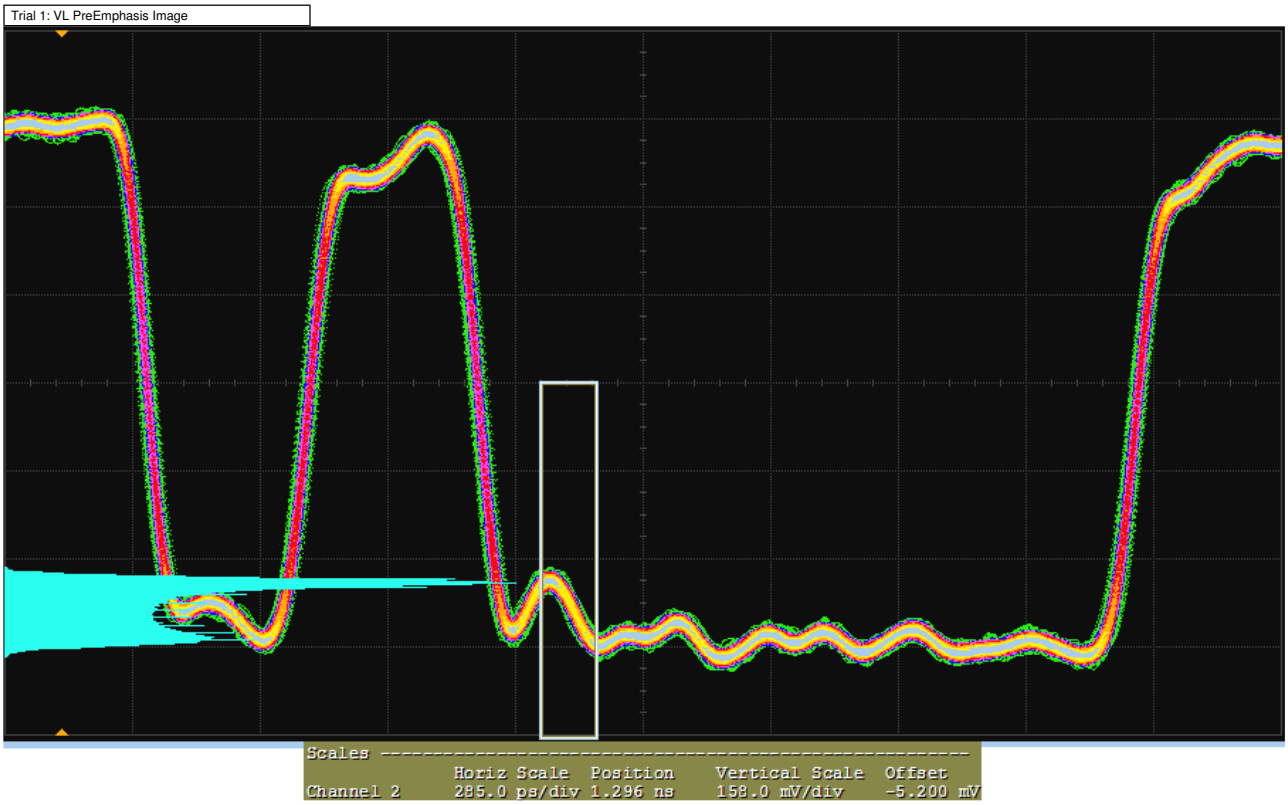
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 2.000 dB** | **PreEmphasis(Pre-emphasis 1) (Worst of 6 Trials) 15 mdB** | **# Trials Run: 6** | **Worst Trial: Trial 1**

Overall Summary + details of 6 worst trials

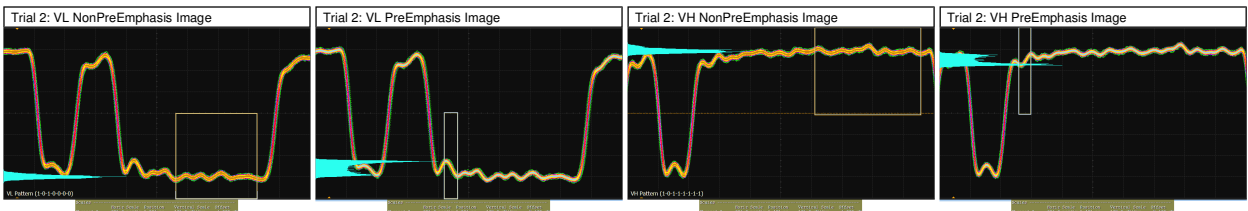
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	44.35 mdB	-97.78 %													
	StdDev	17.80 mdB	895.4 m%													
	Range	51.73 mdB	2.600 %													
	Min	15.16 mdB	-99.25 %													
	Max	66.88 mdB	-96.65 %													
	Sum	266.1 mdB	-586.7 %													
<b>X</b>	Trial 1 (Worst)	15 mdB	-99.3% (See image)	(See image)	(See image)	(See image)	(See image)	1000	775.392 mV	912.128 mV	-1.411 dB	2.7 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
<b>X</b>	Trial 2	67 mdB	-96.7% (See image)	(See image)	(See image)	(See image)	(See image)	1000	626.012 mV	740.331 mV	-1.457 dB	2.7 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
<b>X</b>	Trial 3	36 mdB	-98.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	433.699 mV	519.236 mV	-1.564 dB	2.7 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0
<b>X</b>	Trial 4	43 mdB	-97.9% (See image)	(See image)	(See image)	(See image)	(See image)	1000	853.063 mV	911.391 mV	-574 mdB	1.62 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
<b>X</b>	Trial 5	56 mdB	-97.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	684.714 mV	735.223 mV	-618 mdB	1.62 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
<b>X</b>	Trial 6	49 mdB	-97.6% (See image)	(See image)	(See image)	(See image)	(See image)	1000	475.384 mV	515.472 mV	-703 mdB	1.62 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0

Trial 1

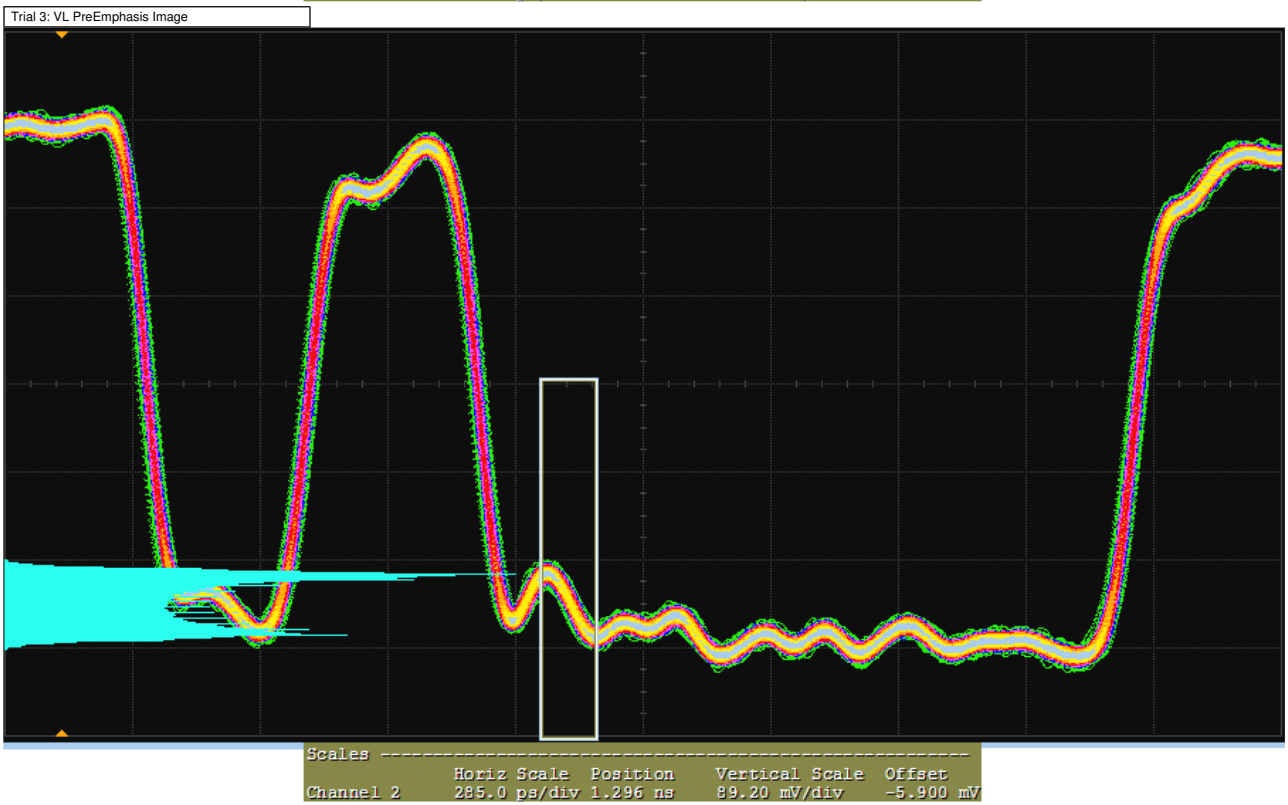
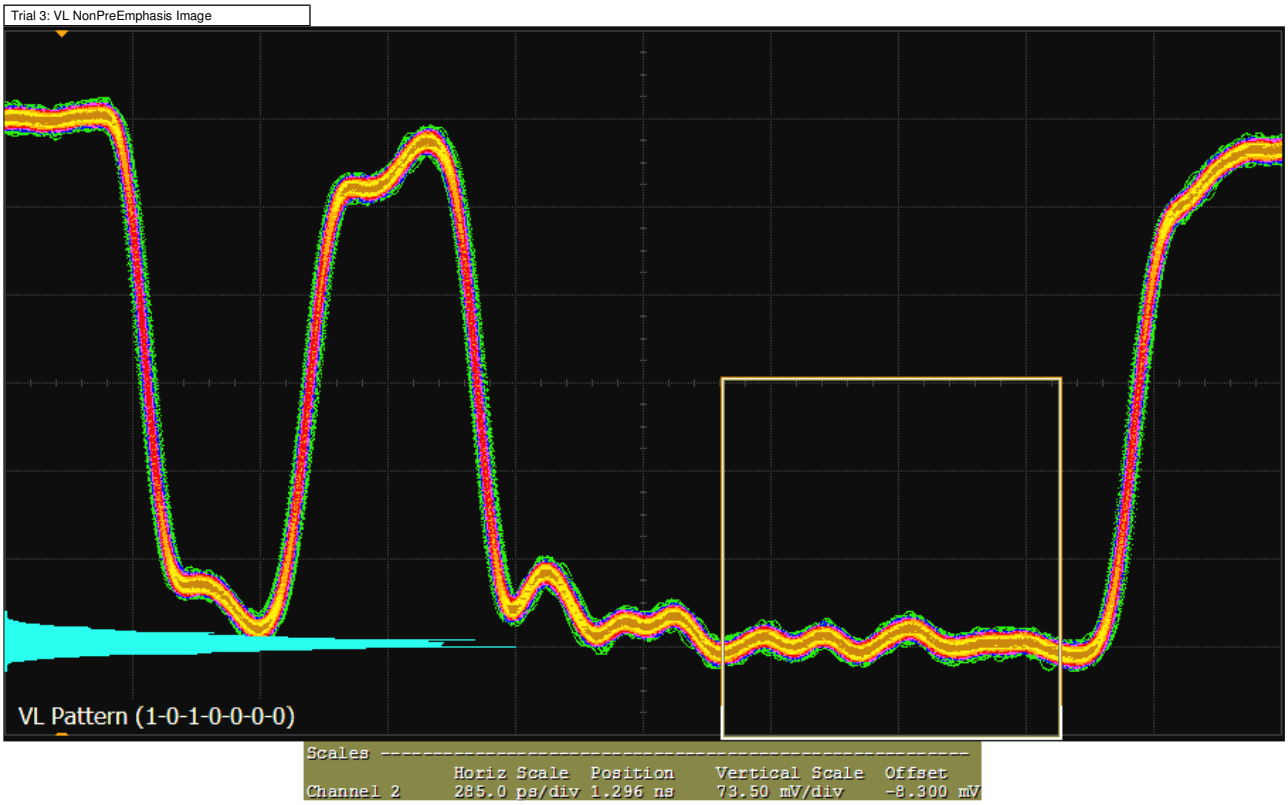


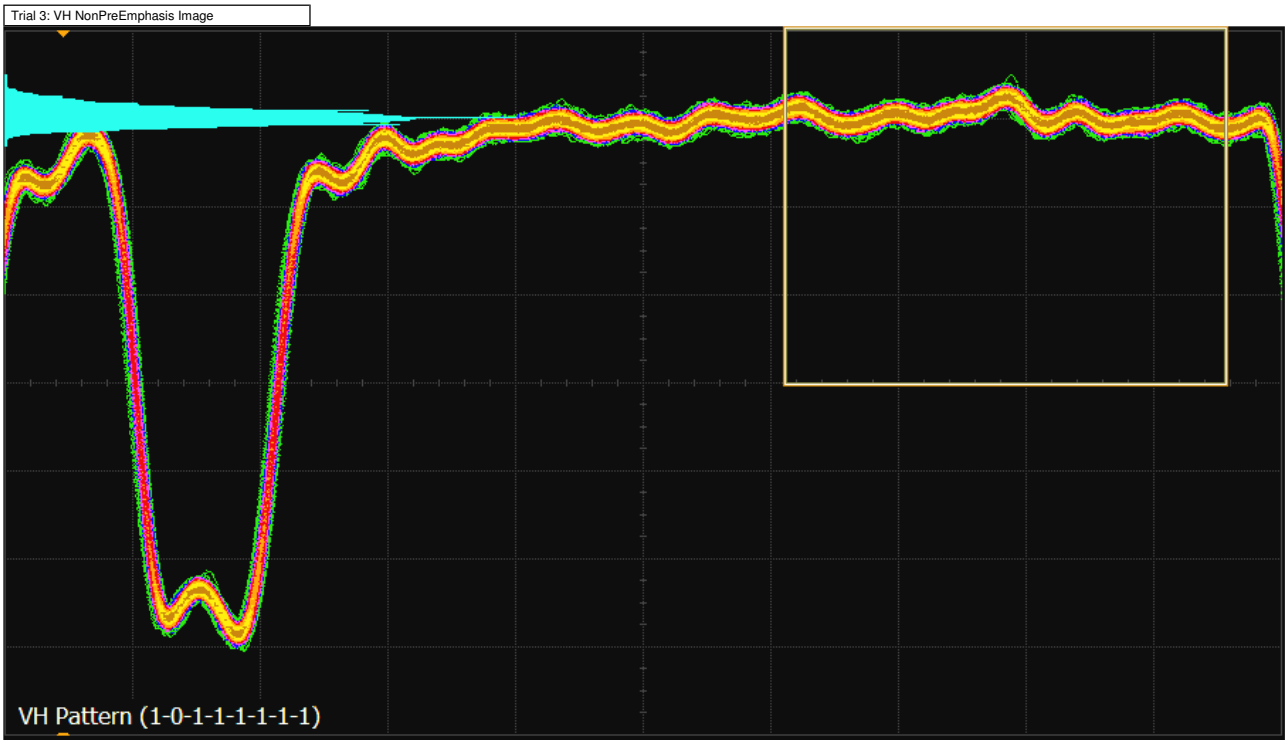


Trial 2



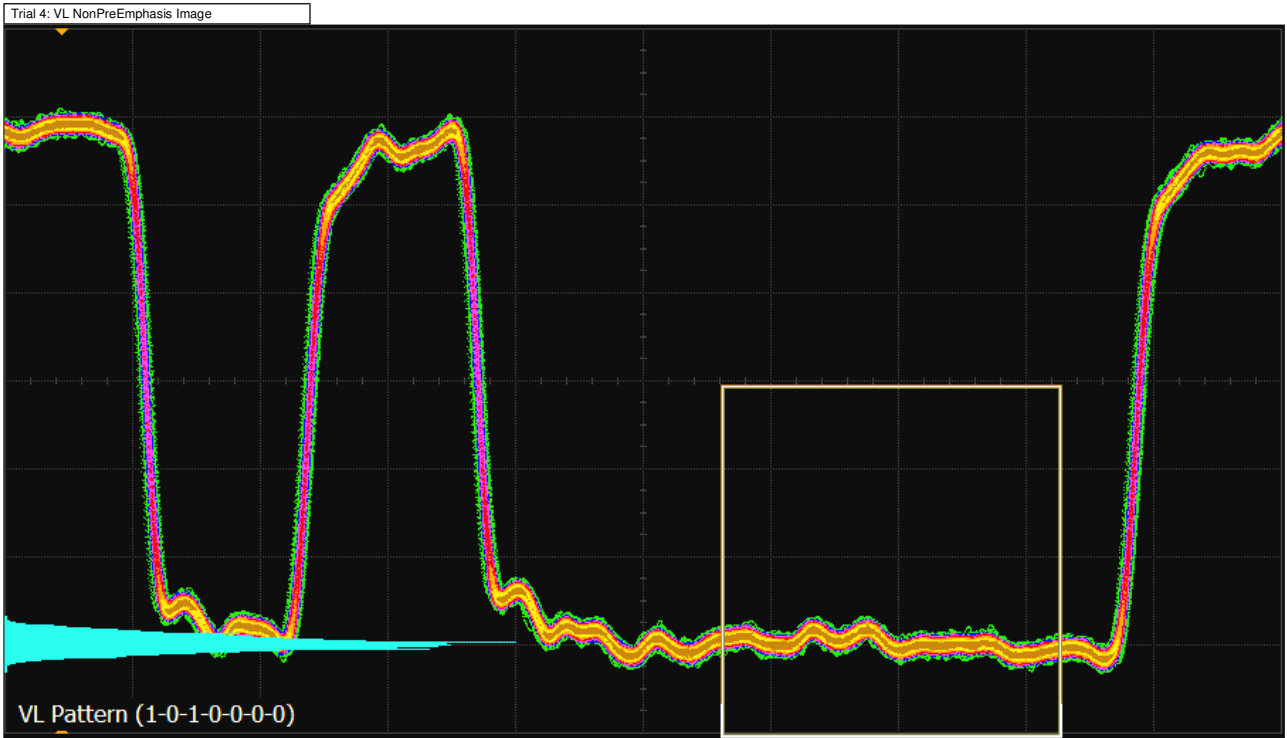
Trial 3





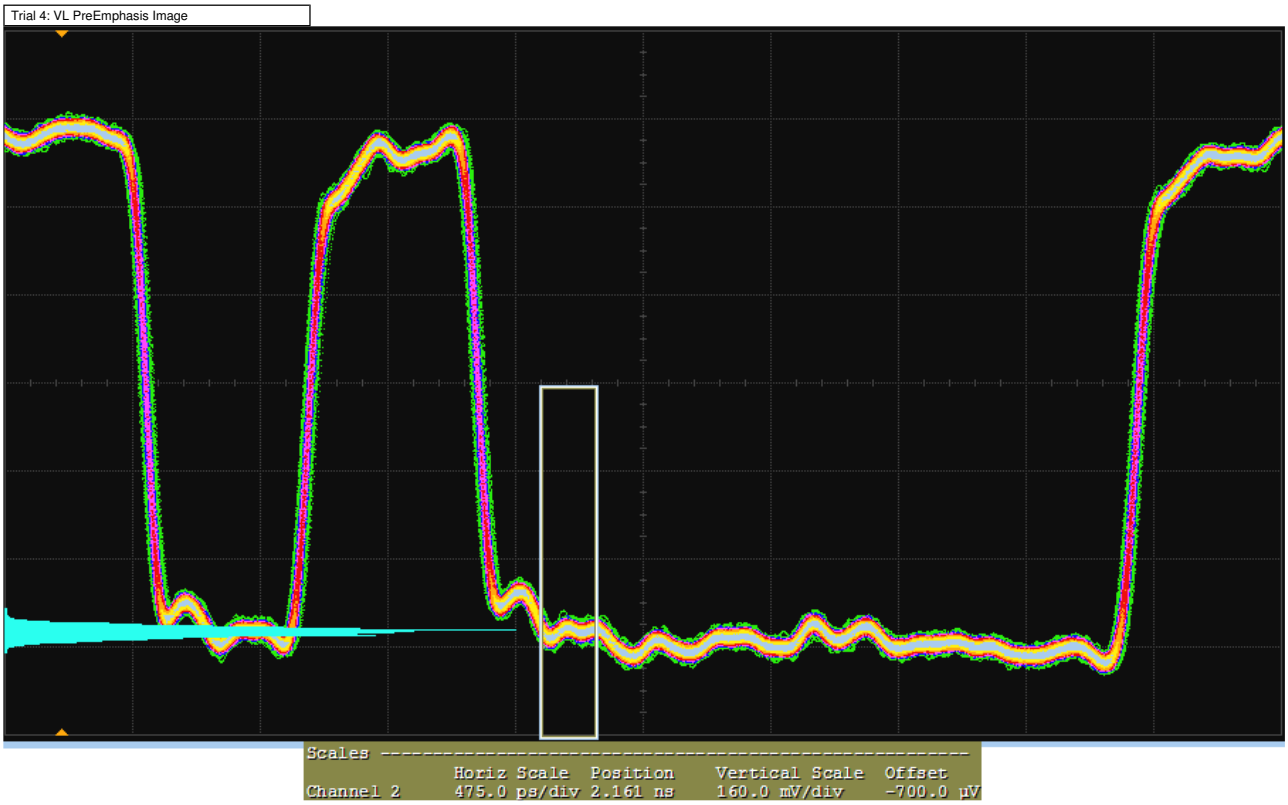
Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	326.0 ps/div	1.481 ns	73.50 mV/div	-8.300 mV

Trial 4

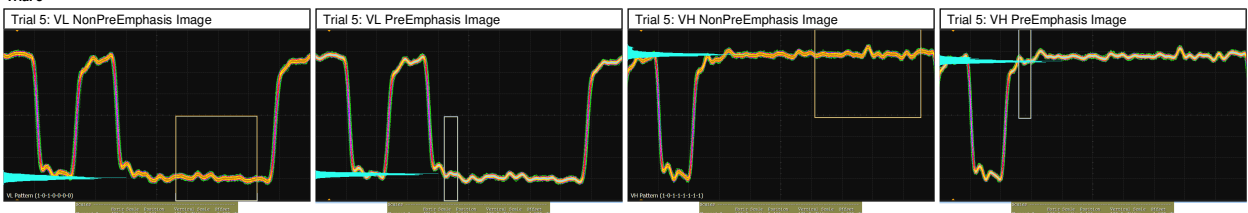


Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	143.0 mV/div	1.000 mV

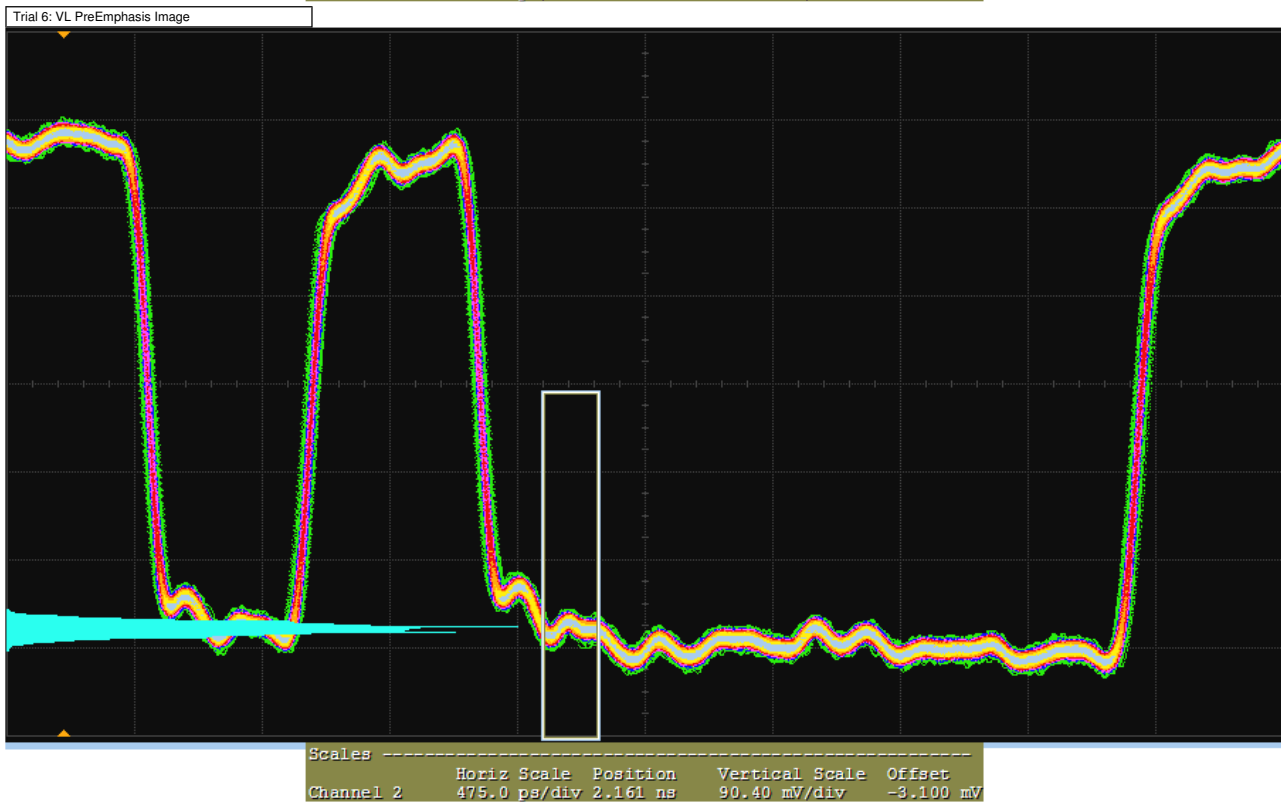
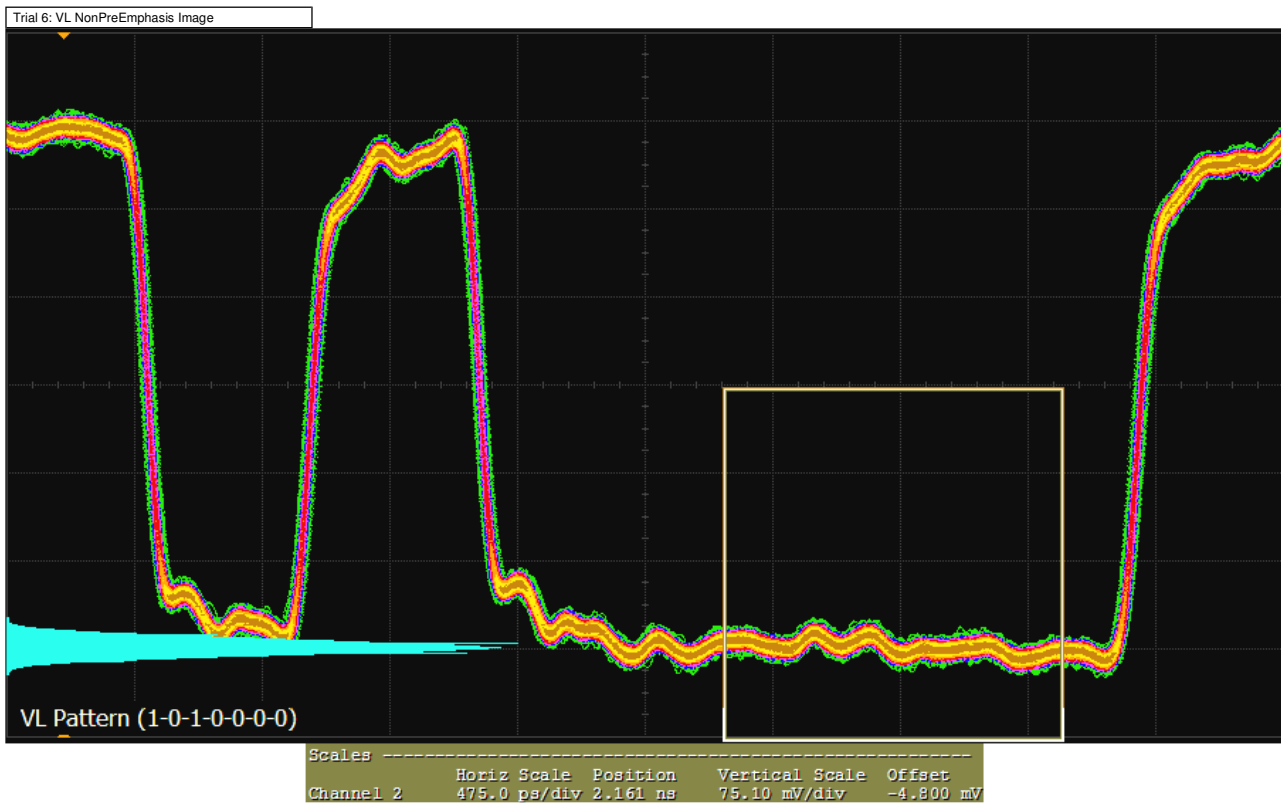


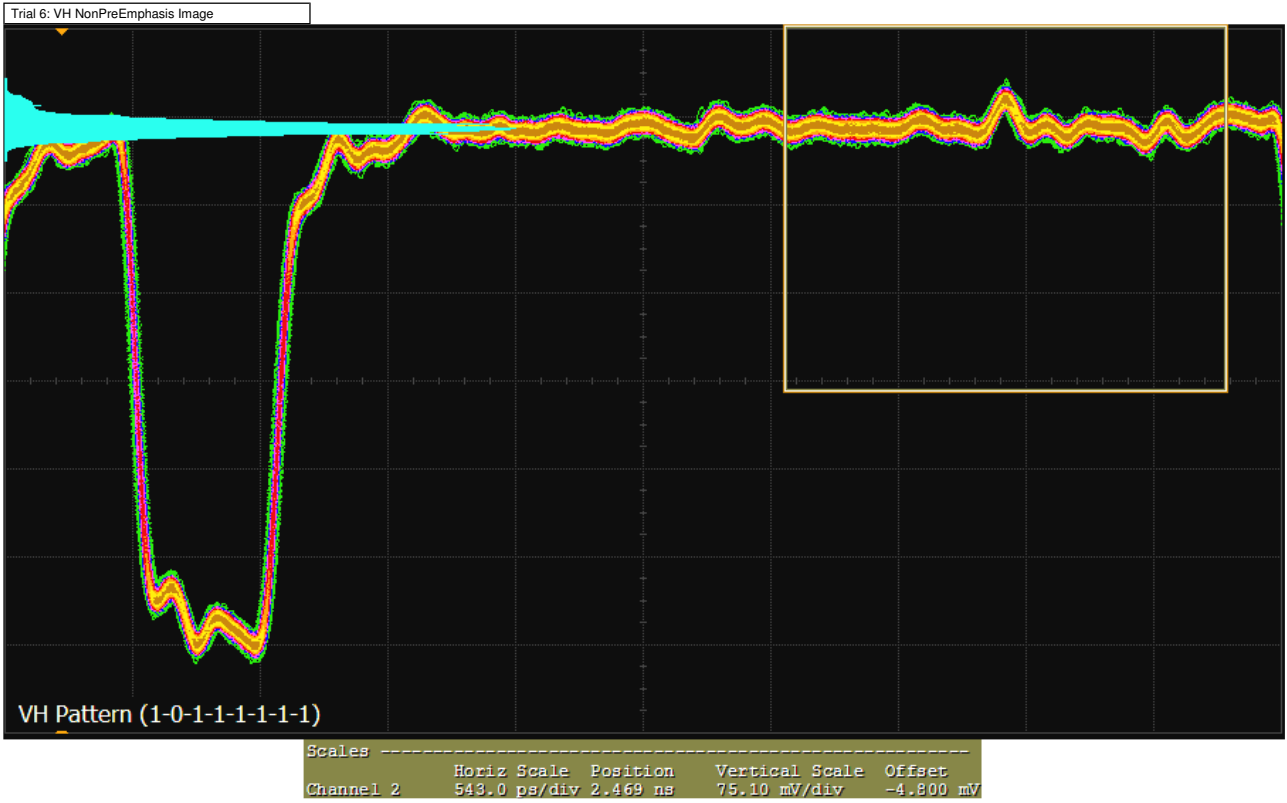


Trial 5



Trial 6





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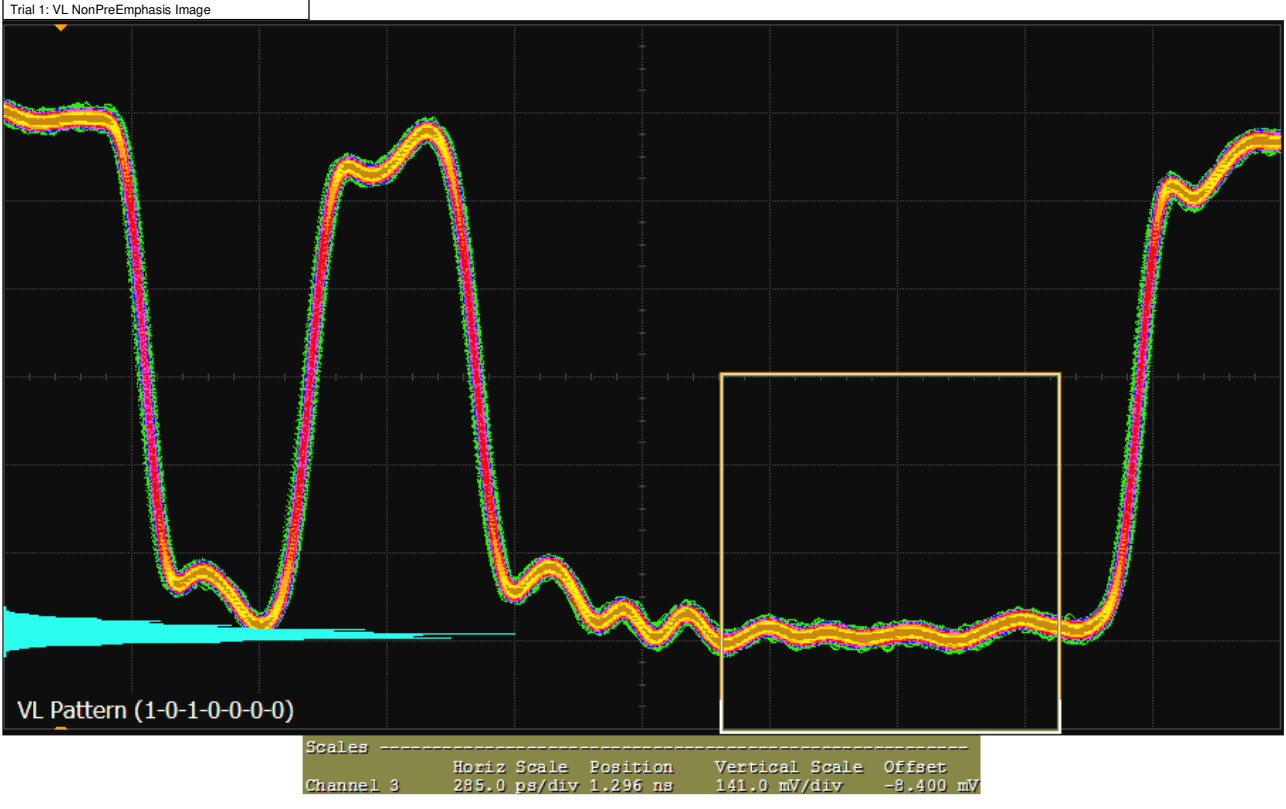
✓ Lane 2 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

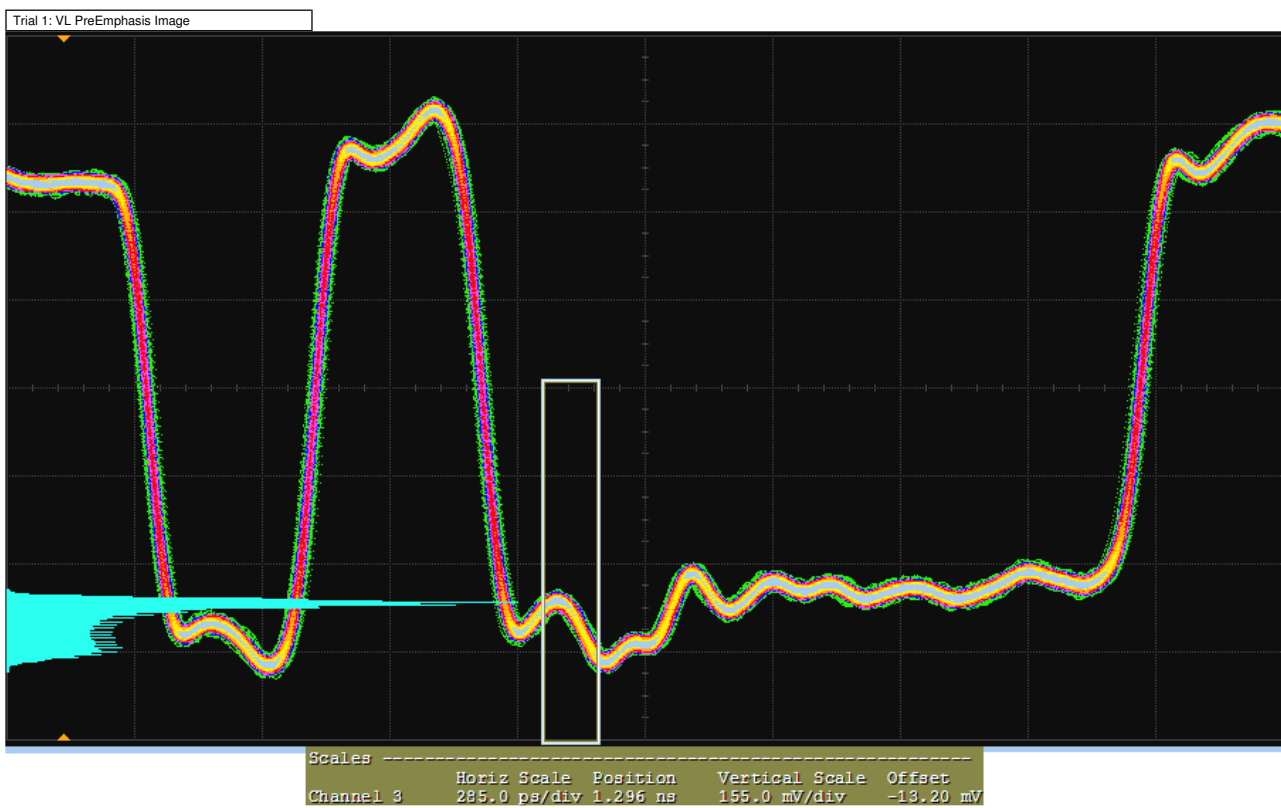
Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 2.000 dB | PreEmphasis(Pre-emphasis 1) (Worst of 6 Trials) 3.021 dB | # Trials Run: 6 | Worst Trial: Trial 1

Overall Summary + details of 6 worst trials

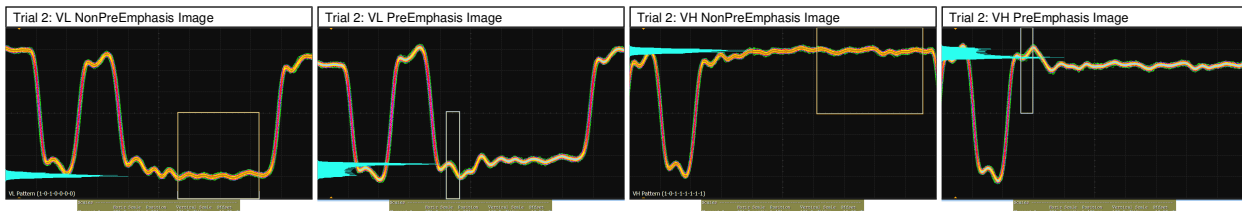
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	3.219 dB	60.95 %													
	StdDev	139.3 mdB	6.977 %													
	Range	334.5 mdB	16.75 %													
	Min	3.021 dB	51.05 %													
	Max	3.356 dB	67.80 %													
	Sum	19.31 dB	365.7 %													
✓	Trial 1 (Worst)	3.021 dB	51.1%	(See image)	(See image)	(See image)	(See image)	1000	871.690 mV	733.983 mV	1.494 dB	2.7 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 2	3.251 dB	62.6%	(See image)	(See image)	(See image)	(See image)	1000	727.948 mV	604.781 mV	1.610 dB	2.7 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 3	3.332 dB	66.6%	(See image)	(See image)	(See image)	(See image)	1000	515.858 mV	429.295 mV	1.595 dB	2.7 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 4	3.072 dB	53.6%	(See image)	(See image)	(See image)	(See image)	1000	941.217 mV	721.783 mV	2.306 dB	1.62 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 5	3.356 dB	67.8%	(See image)	(See image)	(See image)	(See image)	1000	777.791 mV	583.037 mV	2.503 dB	1.62 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 6	3.282 dB	64.1%	(See image)	(See image)	(See image)	(See image)	1000	553.754 mV	416.393 mV	2.476 dB	1.62 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0

Trial 1

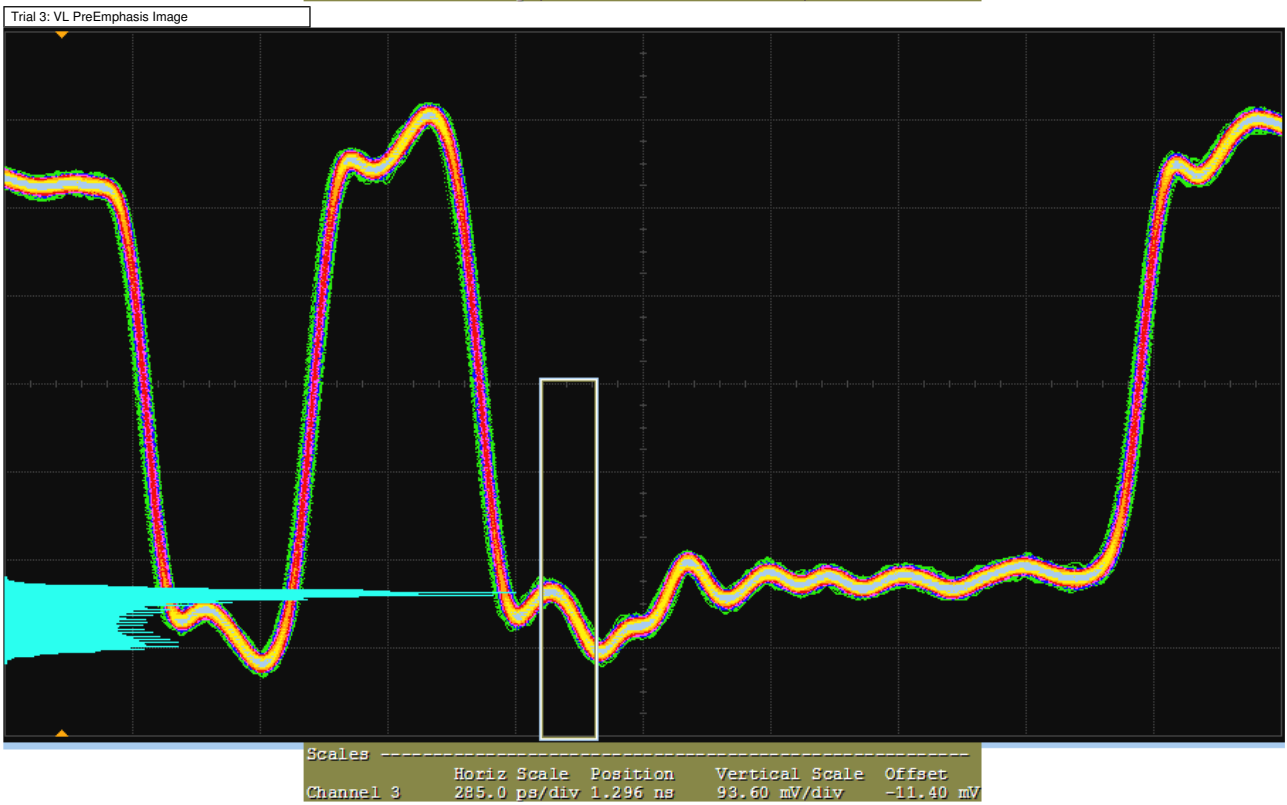
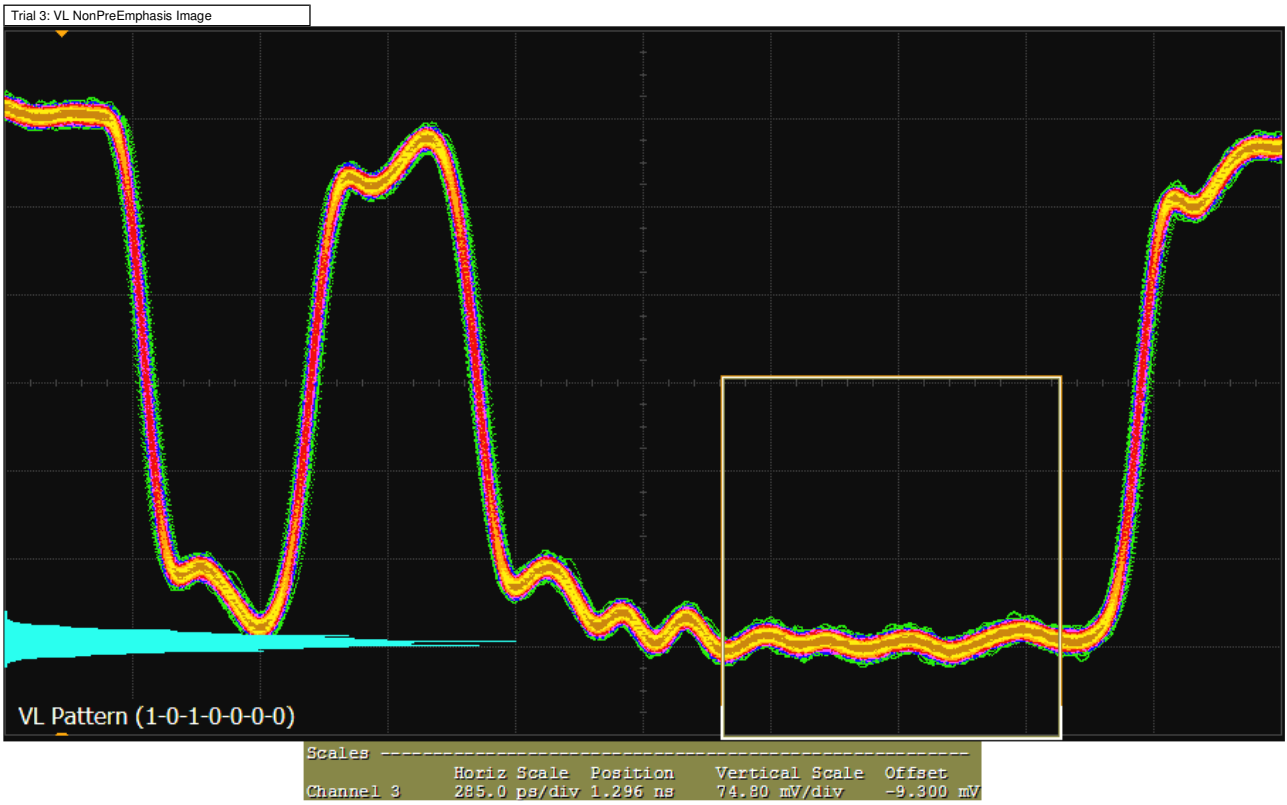




Trial 2



Trial 3



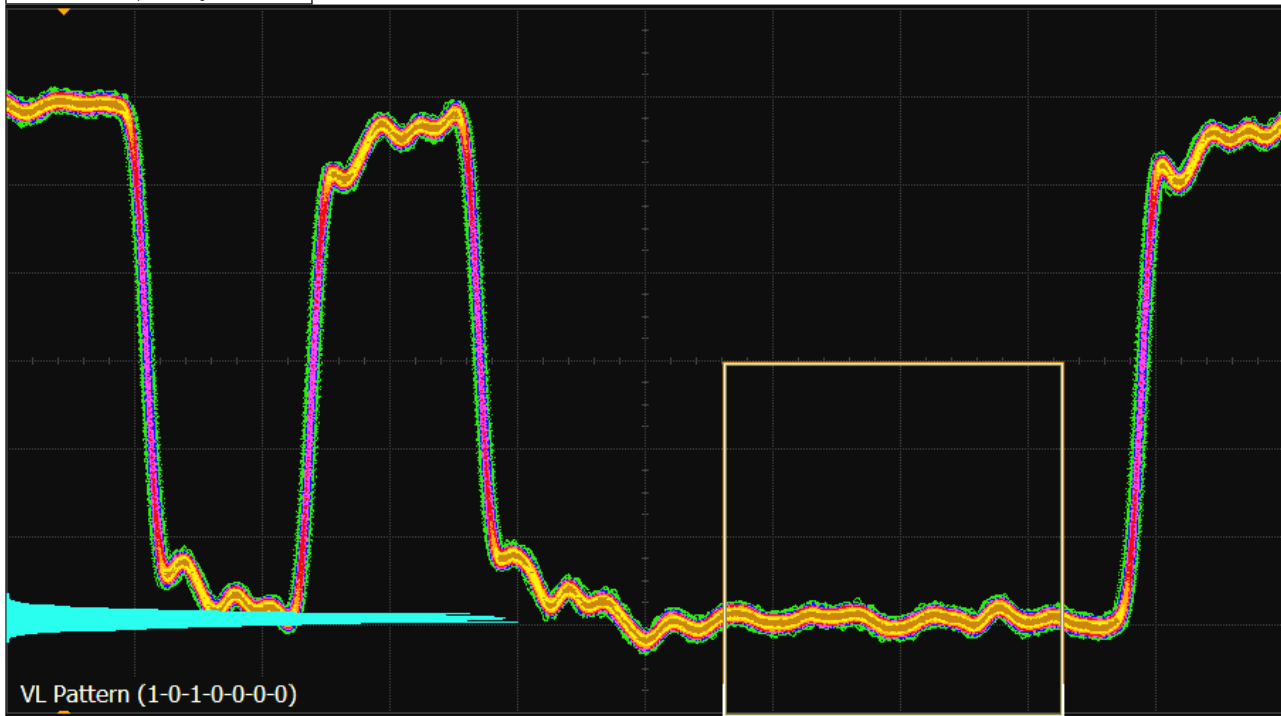
Trial 3: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	326.0 ps/div	1.482 ns	74.80 mV/div	-9.300 mV

Trial 4

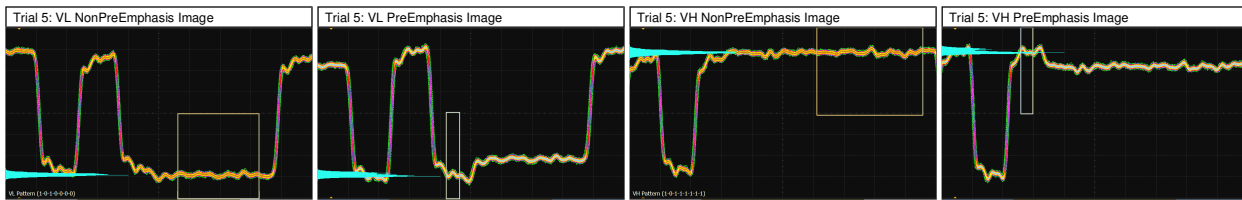
Trial 4: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	145.0 mV/div	-700.0 $\mu$ V



Trial 5



Trial 6



Trial 6: VL NonPreEmphasis Image

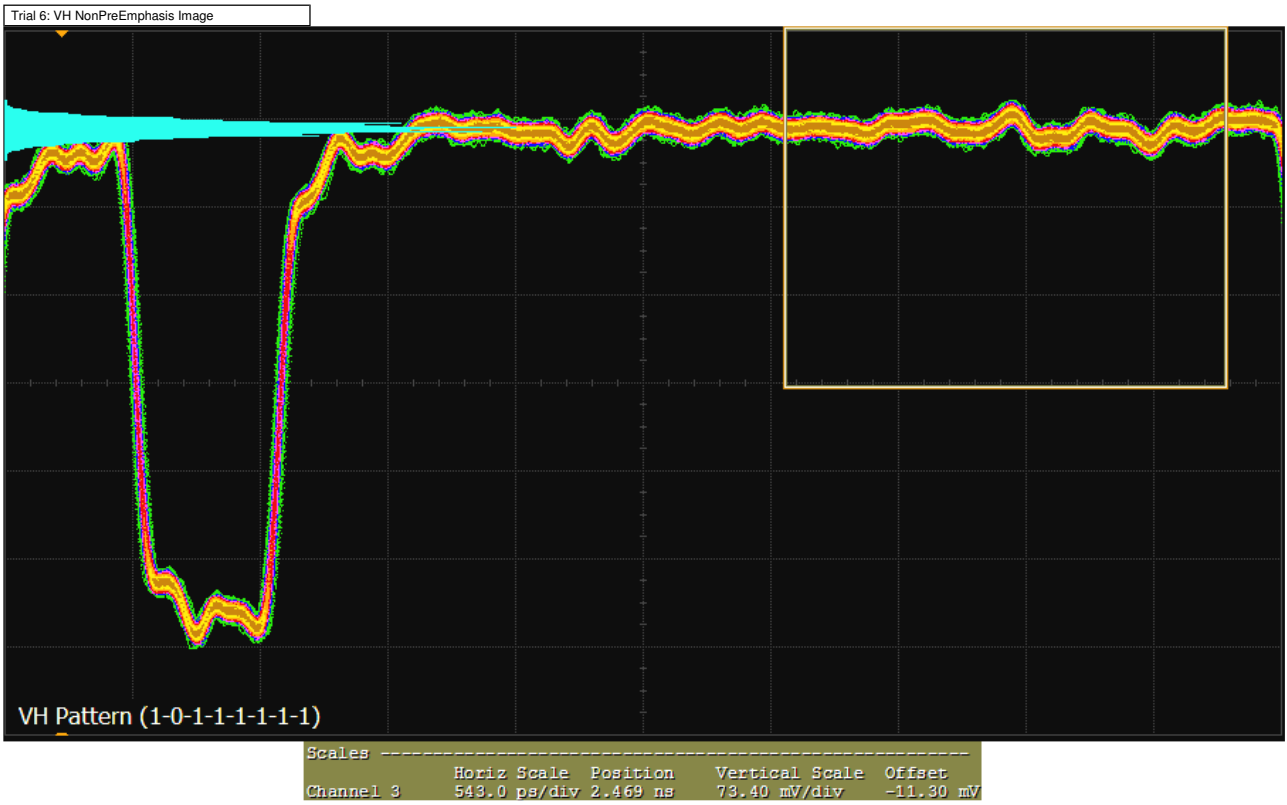


Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	73.40 mV/div	-11.30 mV

Trial 6: VL PreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	96.50 mV/div	-8.600 mV



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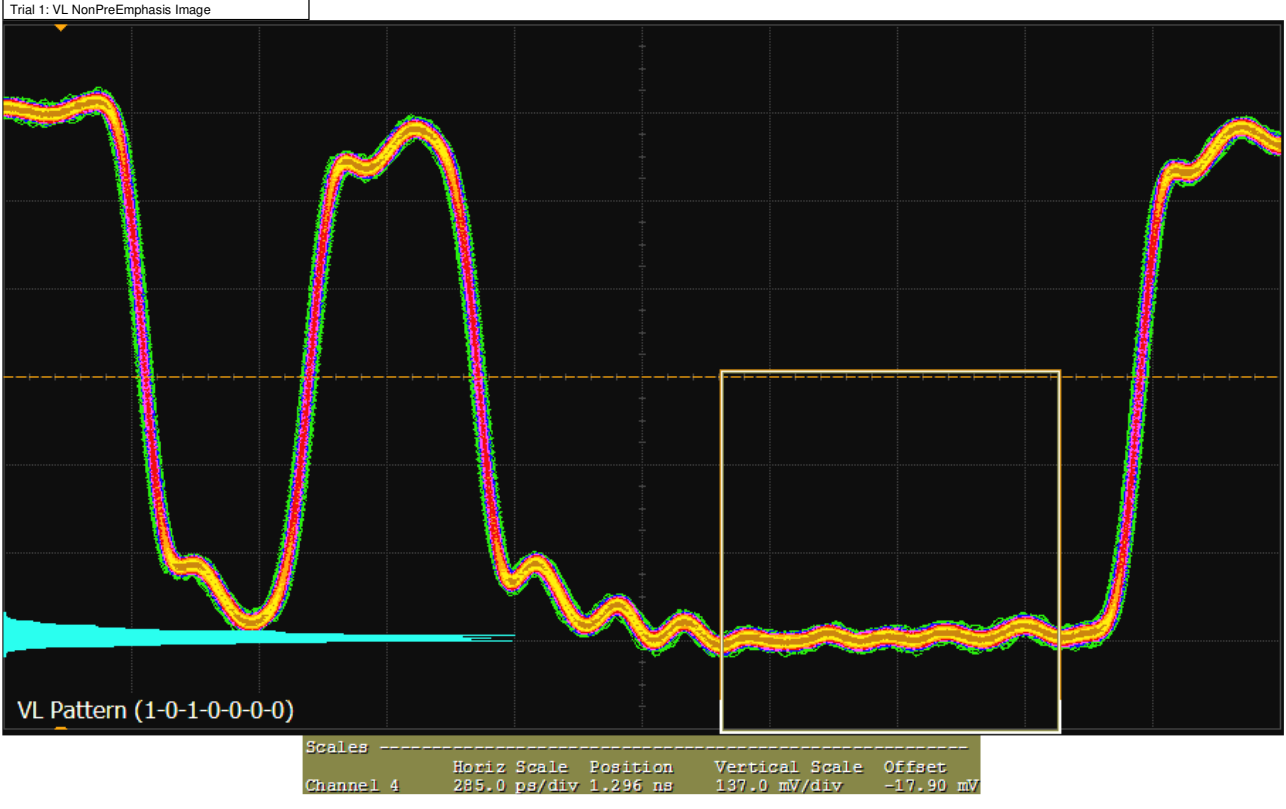
**✘ Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

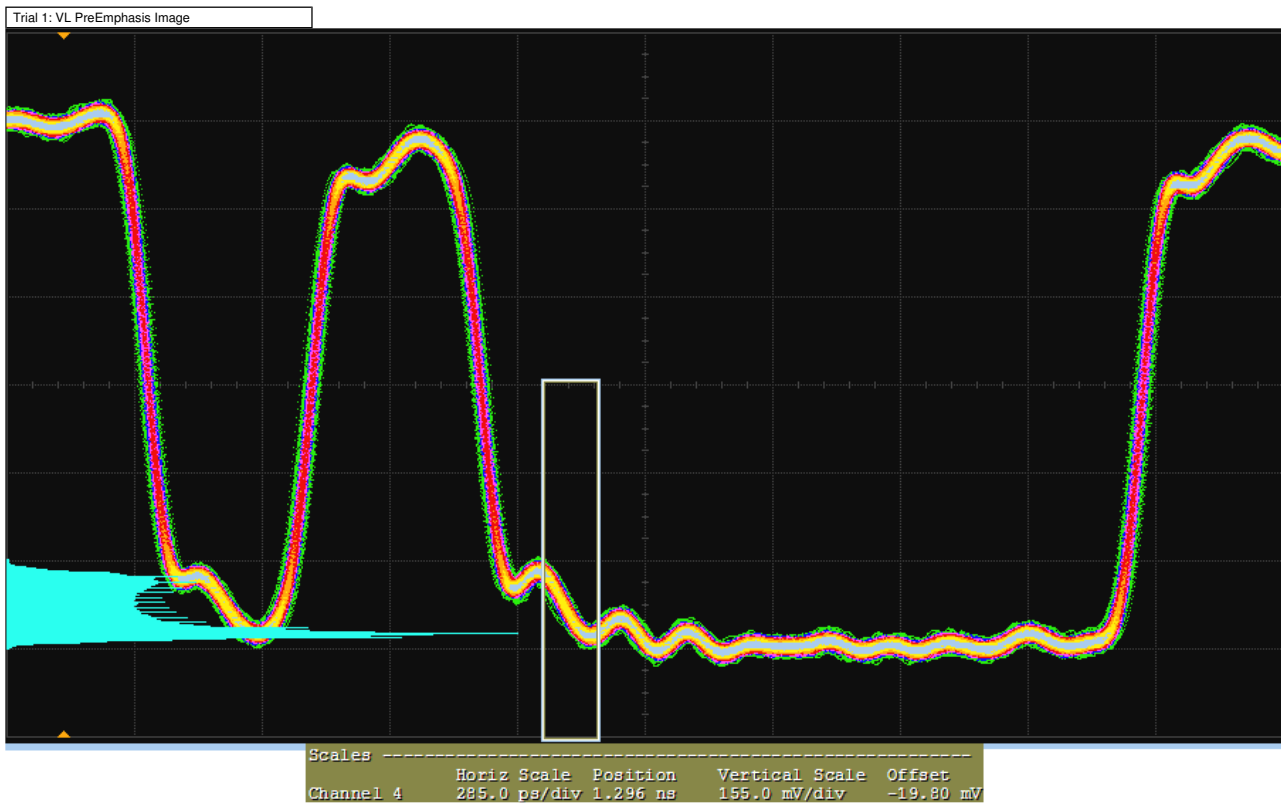
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 2.000 dB** | **PreEmphasis(Pre-emphasis 1) (Worst of 6 Trials) -600 µdB** | **# Trials Run: 6** | **Worst Trial: Trial 3**

Overall Summary + details of 6 worst trials

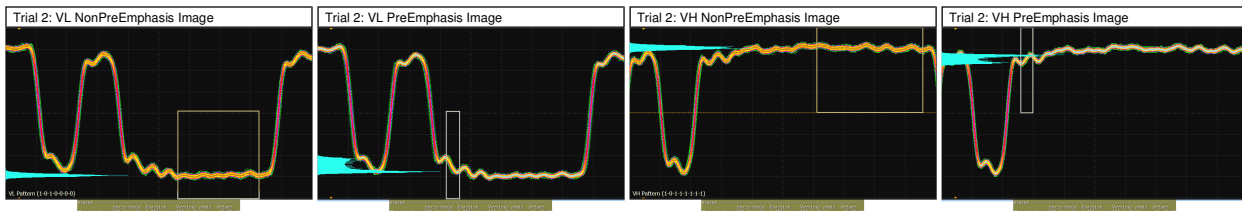
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	32.83 mdB	-98.36 %													
	StdDev	27.63 mdB	1.385 %													
	Range	64.58 mdB	3.250 %													
	Min	-624.2 µdB	-100.1 %													
	Max	63.96 mdB	-96.80 %													
	Sum	197.0 mdB	-590.2 %													
✘	Trial 1	29 mdB	-98.6% (See image)	(See image)	(See image)	(See image)	(See image)	1000	795.480 mV	916.042 mV	-1.226 dB	2.7 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 2	64 mdB	-96.8% (See image)	(See image)	(See image)	(See image)	(See image)	1000	628.990 mV	733.522 mV	-1.335 dB	2.7 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 3 (Worst)	-600 µdB	100.1% (See image)	(See image)	(See image)	(See image)	(See image)	1000	435.656 mV	514.278 mV	-1.441 dB	2.7 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 4	46 mdB	-97.7% (See image)	(See image)	(See image)	(See image)	(See image)	1000	835.247 mV	917.565 mV	-816 mdB	1.62 Gbps	2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 5	57 mdB	-97.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	660.137 mV	732.199 mV	-900 mdB	1.62 Gbps	1	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 6	2 mdB	-99.9% (See image)	(See image)	(See image)	(See image)	(See image)	1000	457.570 mV	512.476 mV	-984 mdB	1.62 Gbps	0	Swing Pre-emphasis	SSC Disabled	Level 0

Trial 1

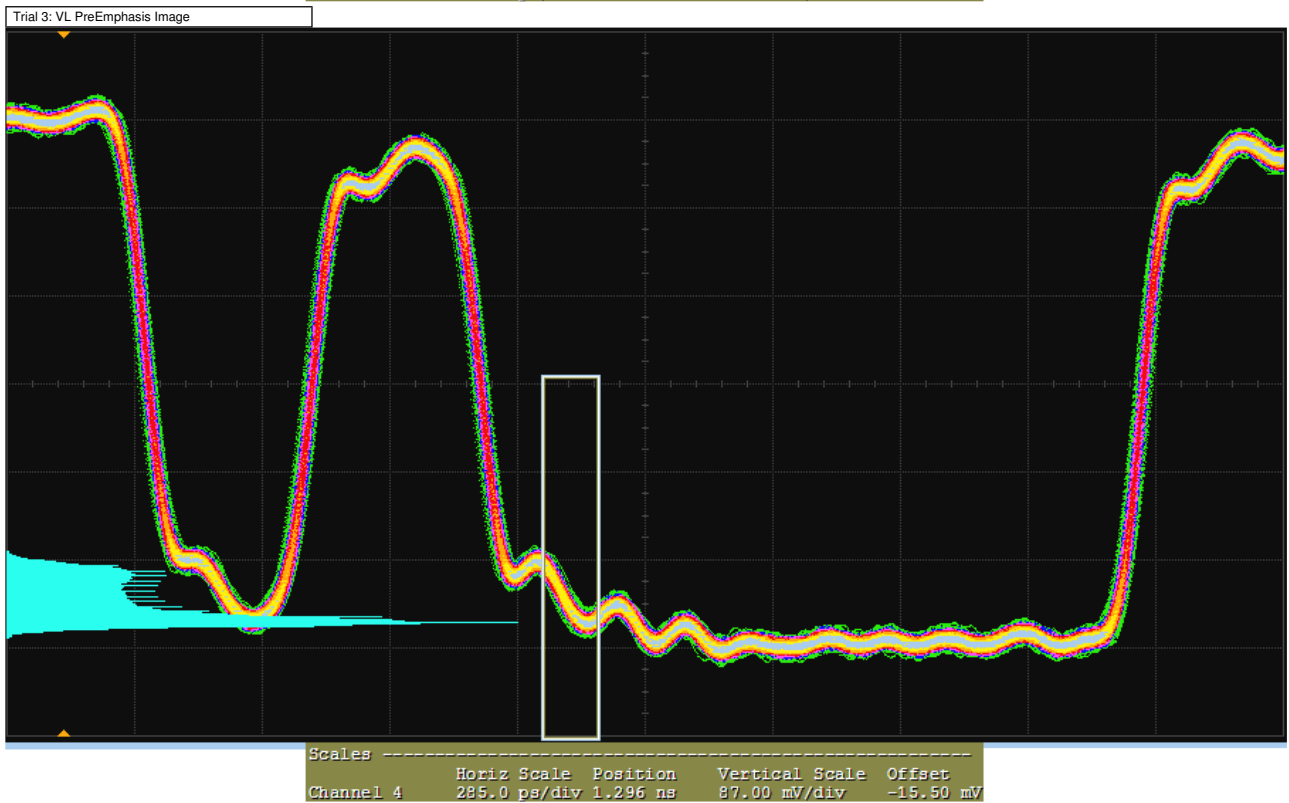
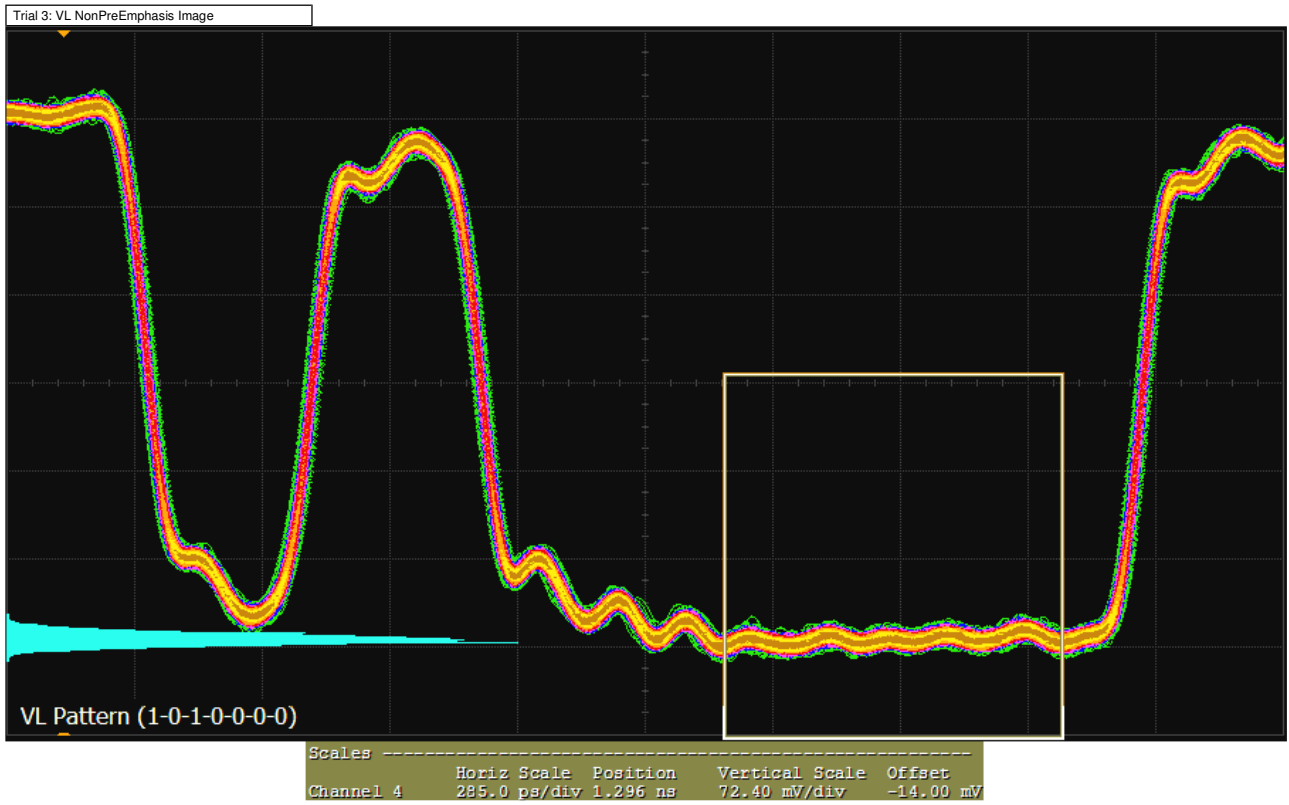


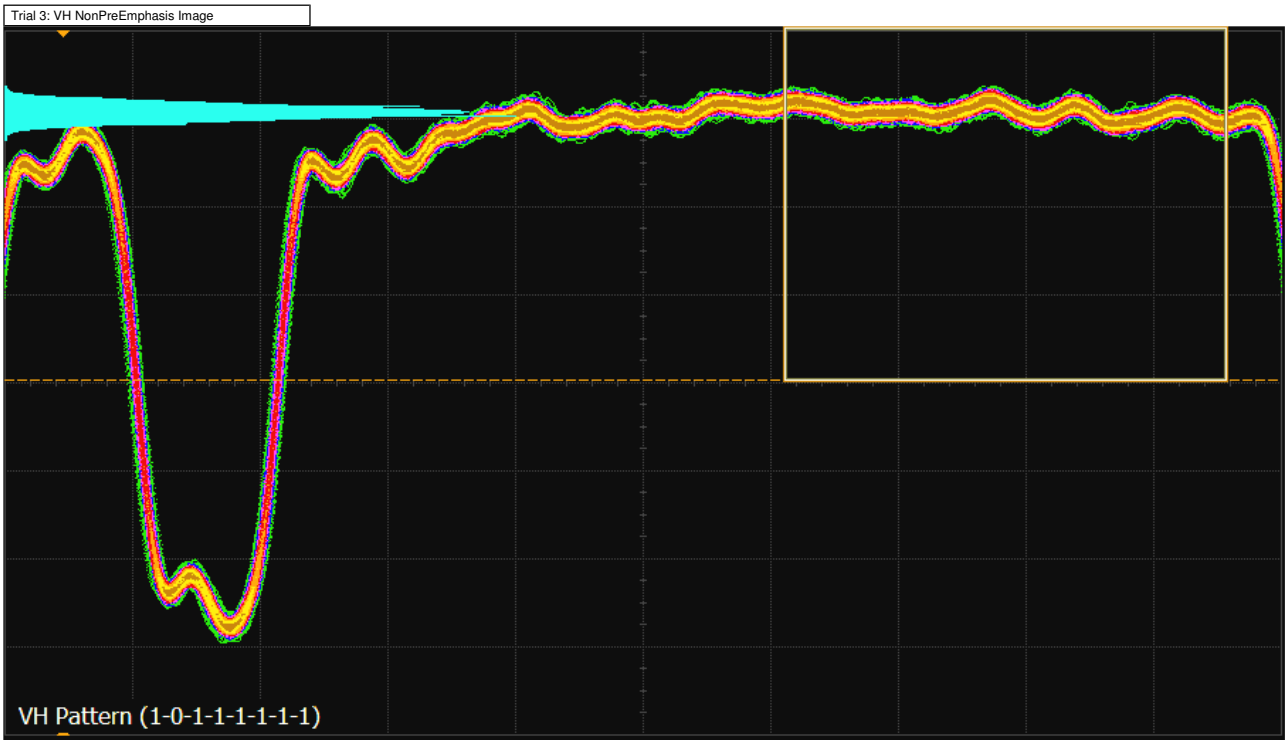


Trial 2

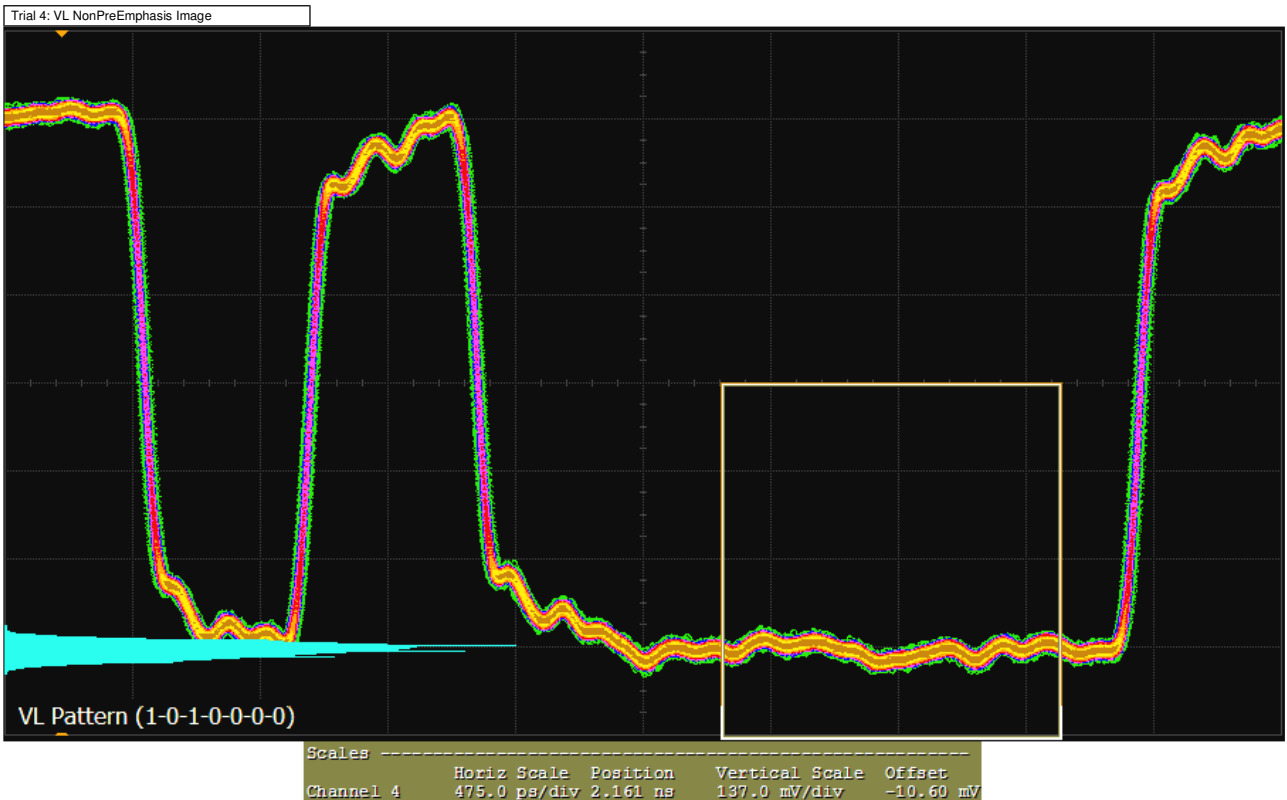


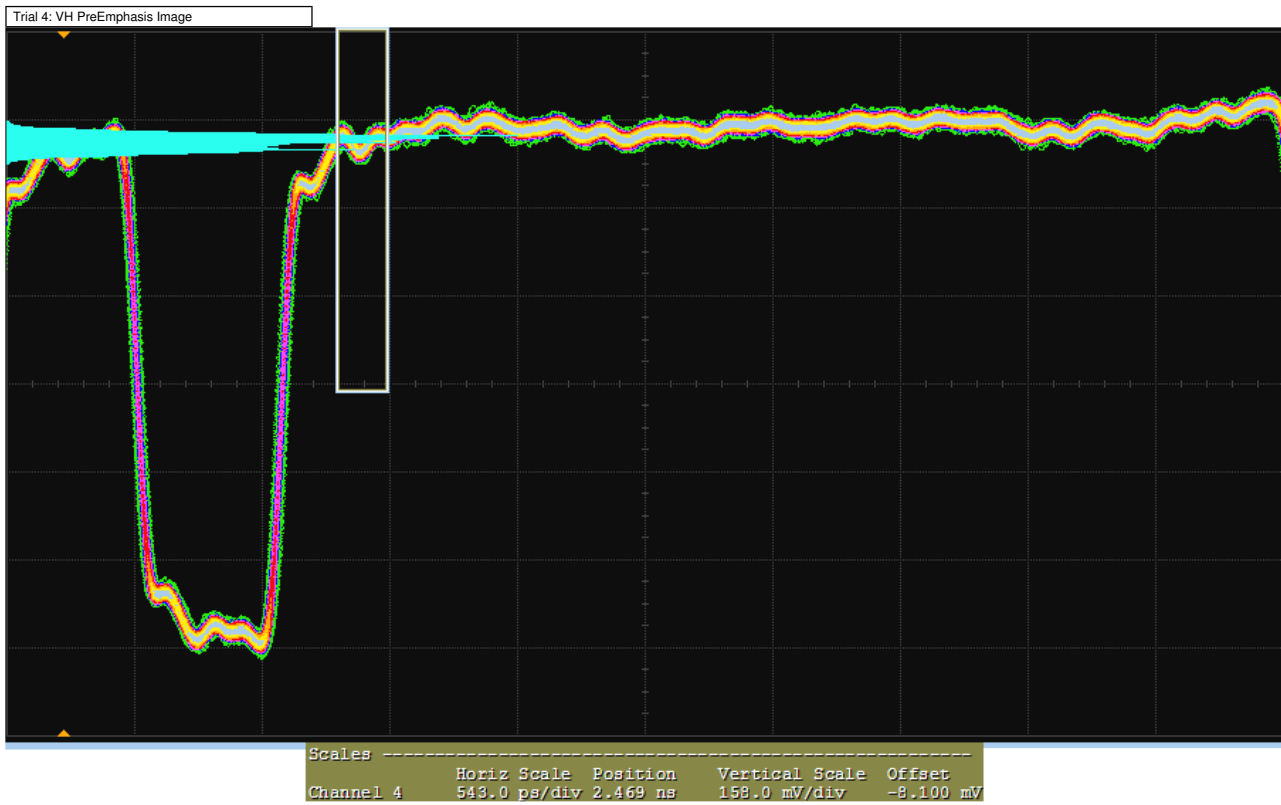
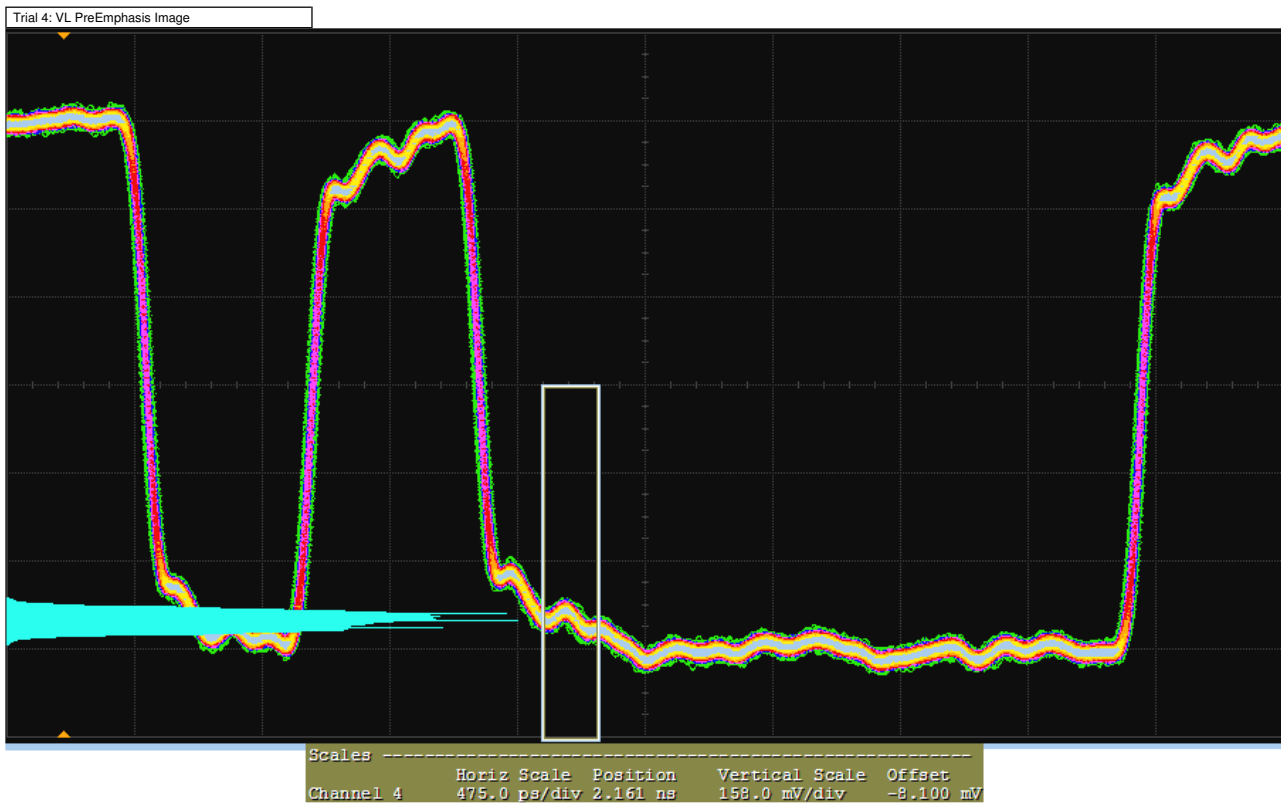
Trial 3



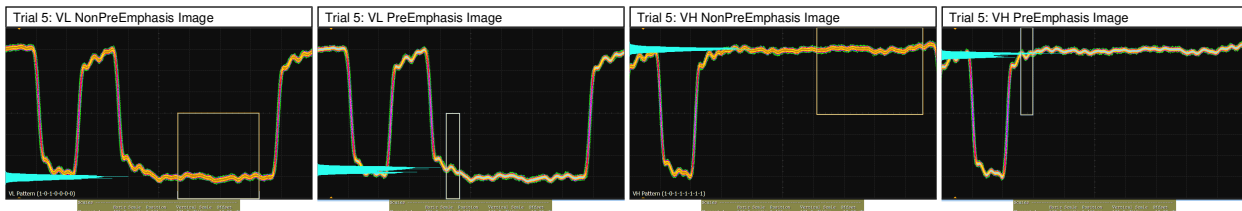


Trial 4

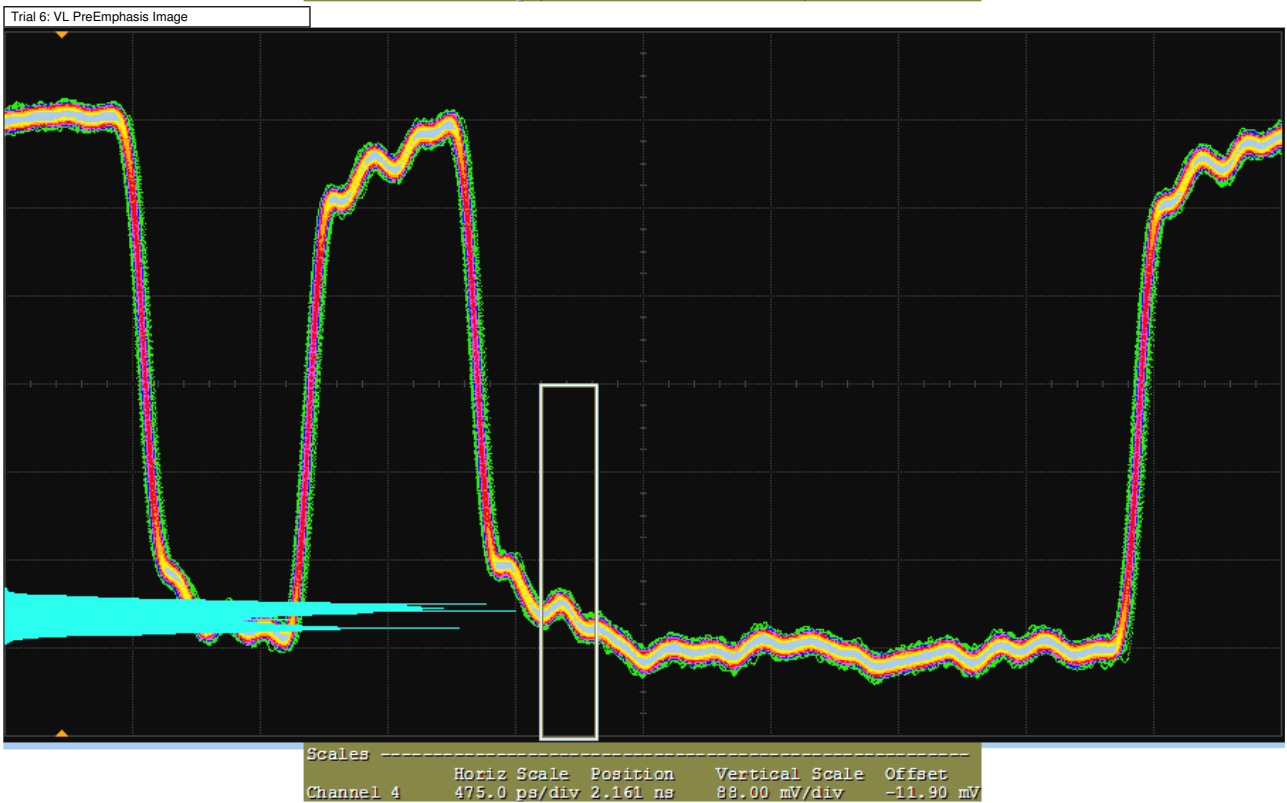
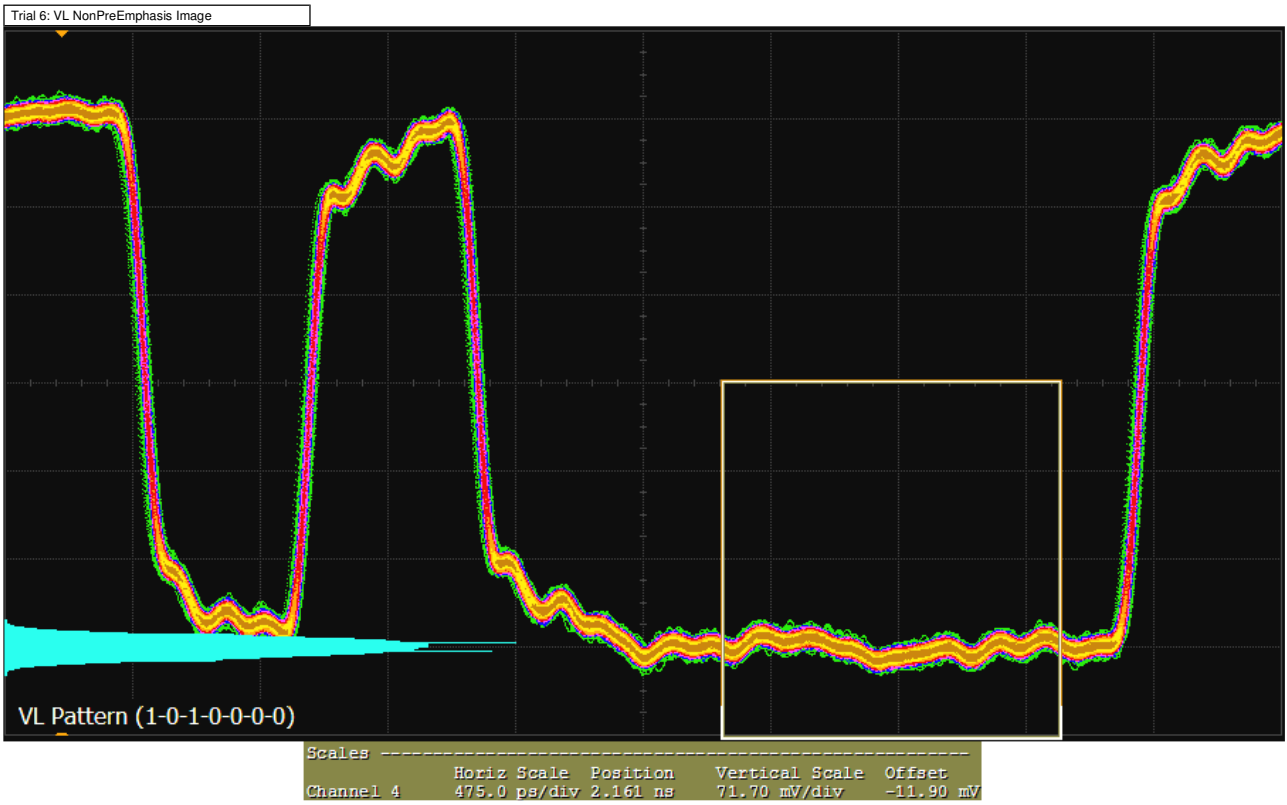




Trial 5



Trial 6







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✓ Lane 0 - Non-Transition Voltage Range Measurement (Swing 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m | **Non-Transition Voltage Range (Worst of 2 Trials)** 726 m | # Trials Run: 2 | Worst Trial: Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 2) (V)	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	727.1 m	2.684 %	NaN V	NaN V									
	StdDev	1.304 m	199.7 m%	NaN V	NaN V									
	Range	1.844 m	282.5 m%	-Infinity V	-Infinity V									
	Min	726.2 m	2.542 %	Infinity V	Infinity V									
	Max	728.0 m	2.825 %	-Infinity V	-Infinity V									
	Sum	1.454	5.367 %	0.000 V	0.000 V									
✓	Trial 1	728 m	2.8%	(no value)	(no value)	819.850 mV	596.851 mV	596.851 mV	596.851 mV	2.7 Gbps	2	1	Pre-emphasis	SSC Disabled Level 0
✓	Trial 2 (Worst)	726 m	2.5%	(no value)	(no value)	814.202 mV	591.239 mV	591.239 mV	591.239 mV	1.62 Gbps	2	1	Pre-emphasis	SSC Disabled Level 0

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✓ Lane 1 - Non-Transition Voltage Range Measurement (Swing 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range (Worst of 2 Trials) 1.113 # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 2) (V)	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	1.116	57.63 %	NaN V	NaN V									
	StdDev	4.379 m	599.2 m%	NaN V	NaN V									
	Range	6.193 m	847.5 m%	-Infinity V	-Infinity V									
	Min	1.113	57.20 %	Infinity V	Infinity V									
	Max	1.119	58.05 %	-Infinity V	-Infinity V									
	Sum	2.232	115.3 %	0.000 V	0.000 V									
✓	Trial 1 (Worst)	1.113	57.2%	(no value)	(no value)	819.768 mV	912.128 mV	912.128 mV	912.128 mV	2.7 Gbps	2	1	Pre-emphasis Disabled	Level 0
✓	Trial 2	1.119	58.1%	(no value)	(no value)	814.571 mV	911.391 mV	911.391 mV	911.391 mV	1.62 Gbps	2	1	Pre-emphasis Disabled	Level 0

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✓ Lane 2 - Non-Transition Voltage Range Measurement (Swing 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m | **Non-Transition Voltage Range (Worst of 2 Trials)** 885 m | # Trials Run: 2 | Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 2) (V)	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	885.4 m	25.07 %	NaN V	NaN V									
	StdDev	385.1 μ	99.87 m%	NaN V	NaN V									
	Range	544.6 μ	141.2 m%	-Infinity V	-Infinity V									
	Min	885.1 m	25.00 %	Infinity V	Infinity V									
	Max	885.7 m	25.14 %	-Infinity V	-Infinity V									
	Sum	1.771	50.14 %	0.000 V	0.000 V									
✓	Trial 1 (Worst)	885 m	25.0%	(no value)	(no value)	829.219 mV	733.983 mV	733.983 mV	733.983 mV	2.7 Gbps	2	1	Pre-emphasis Disabled	Level 0
✓	Trial 2	886 m	25.1%	(no value)	(no value)	814.935 mV	721.783 mV	721.783 mV	721.783 mV	1.62 Gbps	2	1	Pre-emphasis Disabled	Level 0

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✓ Lane 3 - Non-Transition Voltage Range Measurement (Swing 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range (Worst of 2 Trials) 1.123 # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 2) (V)	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	1.125	58.90 %	NaN V	NaN V									
	StdDev	2.423 m	399.5 m%	NaN V	NaN V									
	Range	3.427 m	565.0 m%	-Infinity V	-Infinity V									
	Min	1.123	58.62 %	Infinity V	Infinity V									
	Max	1.127	59.18 %	-Infinity V	-Infinity V									
	Sum	2.250	117.8 %	0.000 V	0.000 V									
✓	Trial 1 (Worst)	1.123	58.6%	(no value)	(no value)	815.375 mV	916.042 mV	916.042 mV	916.042 mV	2.7 Gbps	2	Swing	Pre-emphasis 1	SSC Disabled Level 0
✓	Trial 2	1.127	59.2%	(no value)	(no value)	814.248 mV	917.565 mV	917.565 mV	917.565 mV	1.62 Gbps	2	Swing	Pre-emphasis 1	SSC Disabled Level 0

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✓ Lane 0 - Non-PreEmphasis Level Test (Swing 1/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
 Pass Limits: [800.0 mdB to 6.0000 dB] Lane 0 Non-PreEmphasis Level Test (Swing 1/Swing 0) (Worst of 2 Trials) 3.0355 dB # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

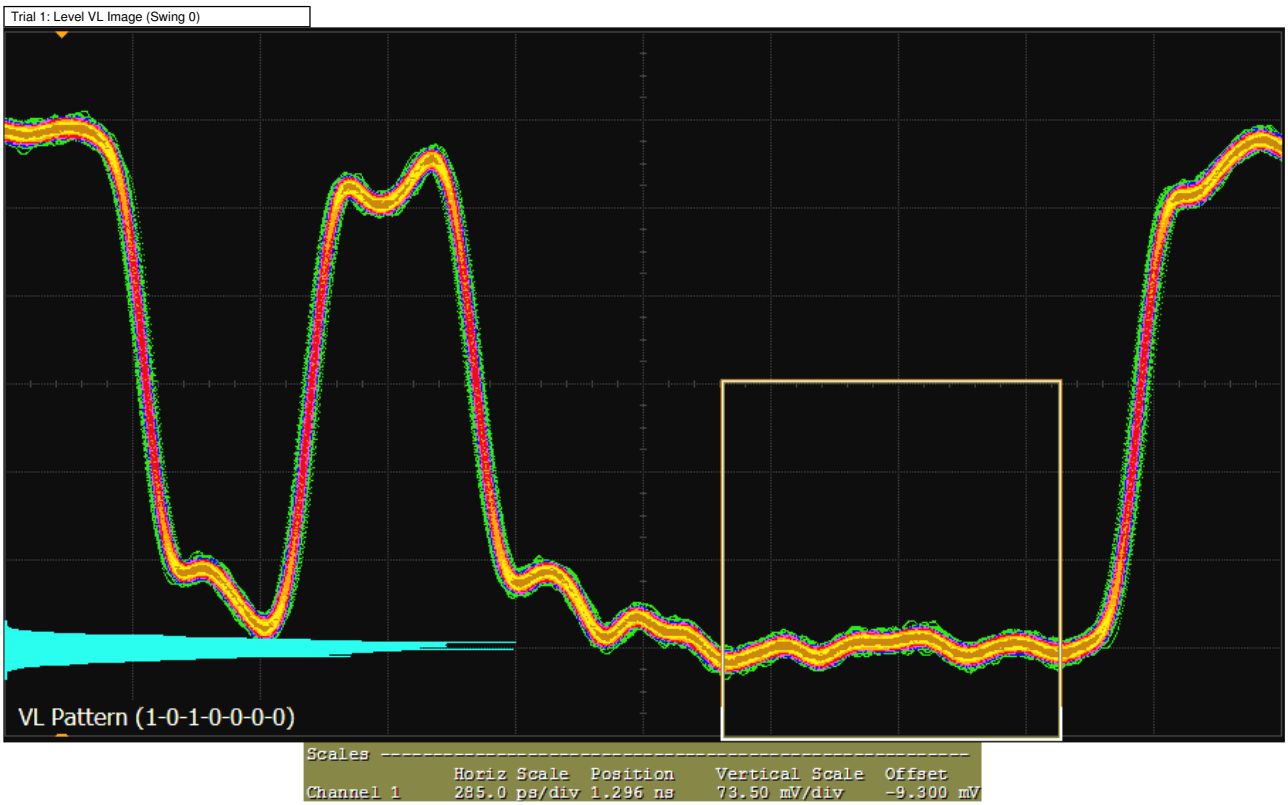
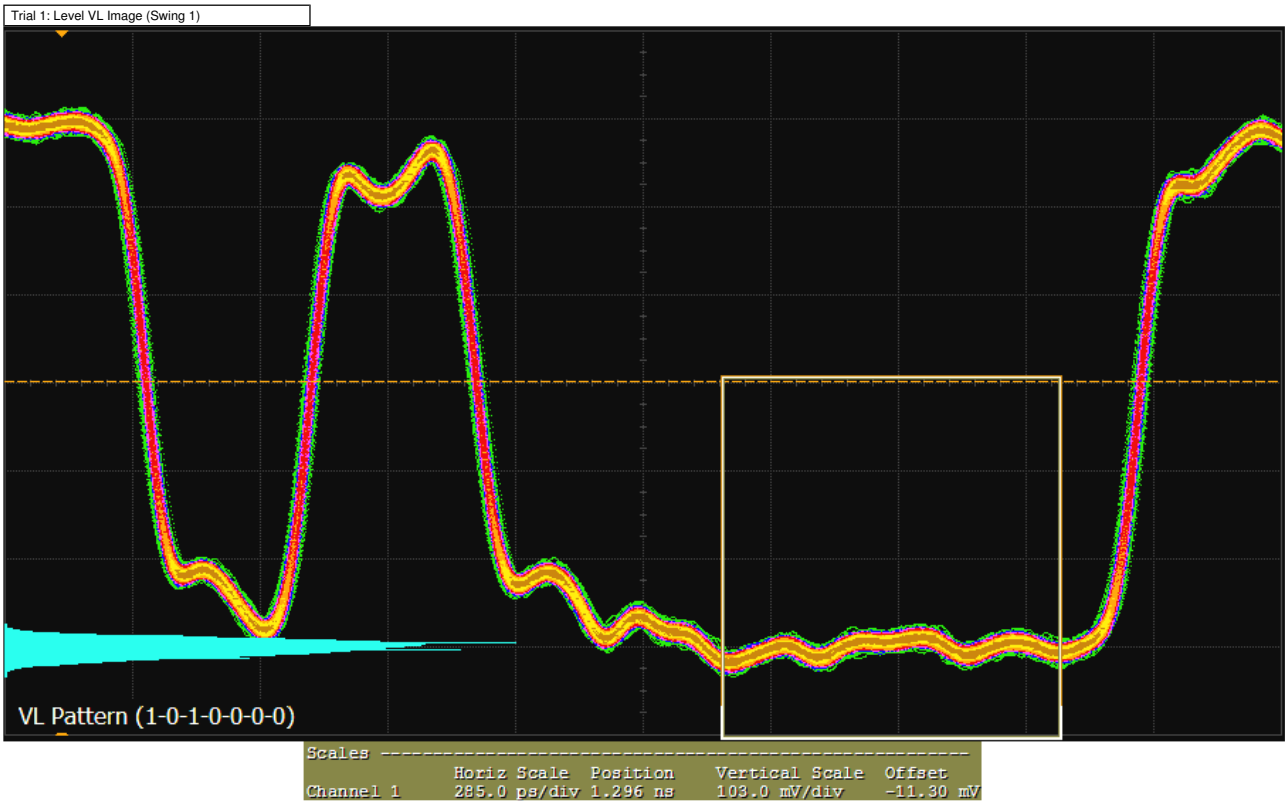
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 1)	Level VL Image (Swing 0)	Level VH Image (Swing 0)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	VTop (Swing 0)	VBase (Swing 0)	VSwing (Swing 0)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitF
	Avg	3.056 dB	43.39 %																				
	StdDev	29.43 mdB	565.7 m%																				
	Range	41.62 mdB	800.0 m%																				
	Min	3.035 dB	42.99 %																				
	Max	3.077 dB	43.79 %																				
	Sum	6.113 dB	86.78 %																				
✓	Trial 1 (Worst)	3.0355 dB	43.0%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	291.842 mV	316.701 mV	608.543 mV	203.674 mV	225.385 mV	429.059 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2	3.0771 dB	43.8%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	290.671 mV	311.993 mV	602.664 mV	201.265 mV	221.618 mV	422.883 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

Trial 1

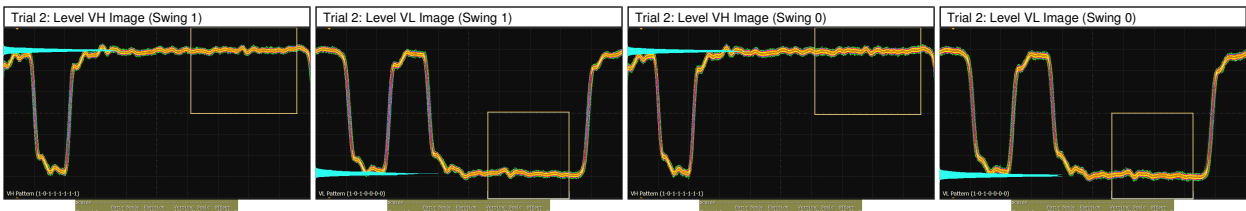
Trial 1: Level VH Image (Swing 1)



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	326.0 ps/div	1.481 ns	103.0 mV/div	-11.30 mV



Trial 2



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✓ Lane 1 - Non-PreEmphasis Level Test (Swing 1/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

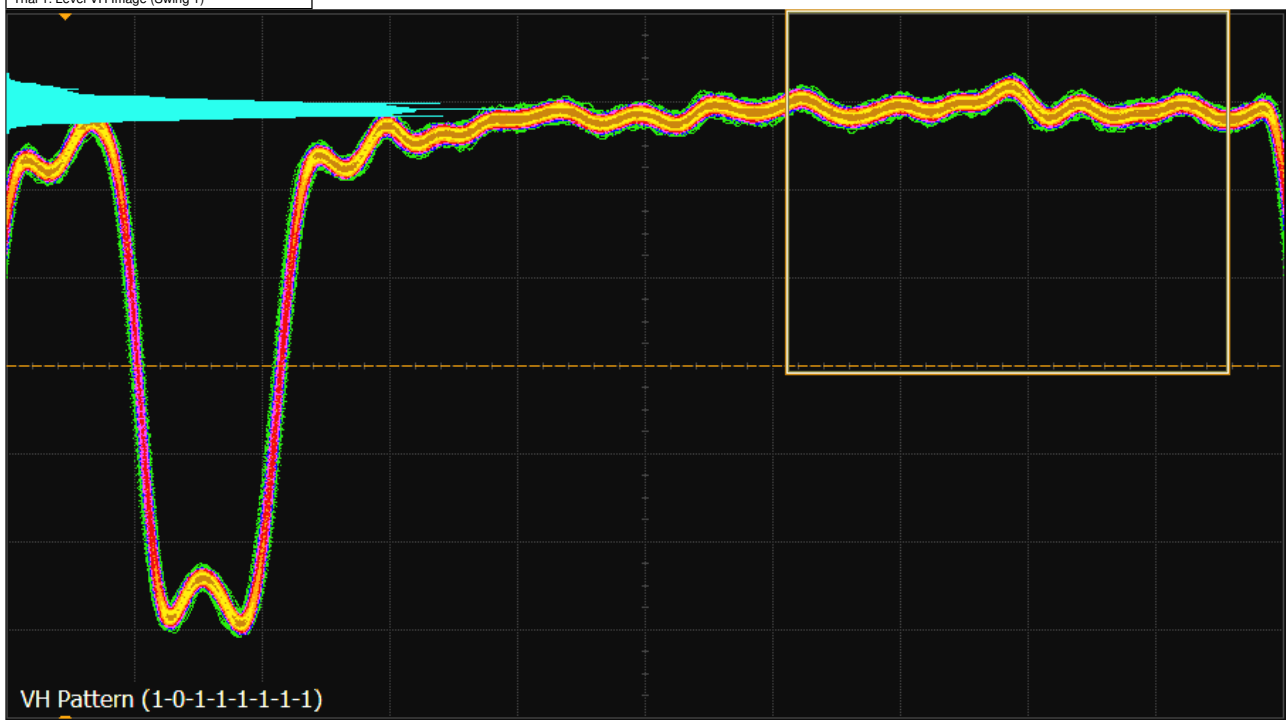
Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [800.0 mdB to 6.0000 dB] **Lane 1 Non-PreEmphasis Level Test (Swing 1/Swing 0) (Worst of 2 Trials)** 3.0377 dB **# Trials Run:** 2 **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Level VH Image (Swing 1)	Level VL Image (Swing 0)	Level VH Image (Swing 0)	Level VL Image (Swing 0)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	VTop (Swing 0)	VBase (Swing 0)	VSwing (Swing 0)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitR
	Avg	3.045 dB	43.18 %																				
	StdDev	10.56 mdB	204.0 m%																				
	Range	14.94 mdB	288.5 m%																				
	Min	3.038 dB	43.03 %																				
	Max	3.053 dB	43.32 %																				
	Sum	6.090 dB	86.35 %																				
✓	Trial 1 (Worst)	3.0377 dB	43.0%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	296.202 mV	313.953 mV	610.155 mV	206.583 mV	223.501 mV	430.084 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2	3.0527 dB	43.3%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	293.032 mV	311.452 mV	604.484 mV	203.201 mV	222.154 mV	425.355 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

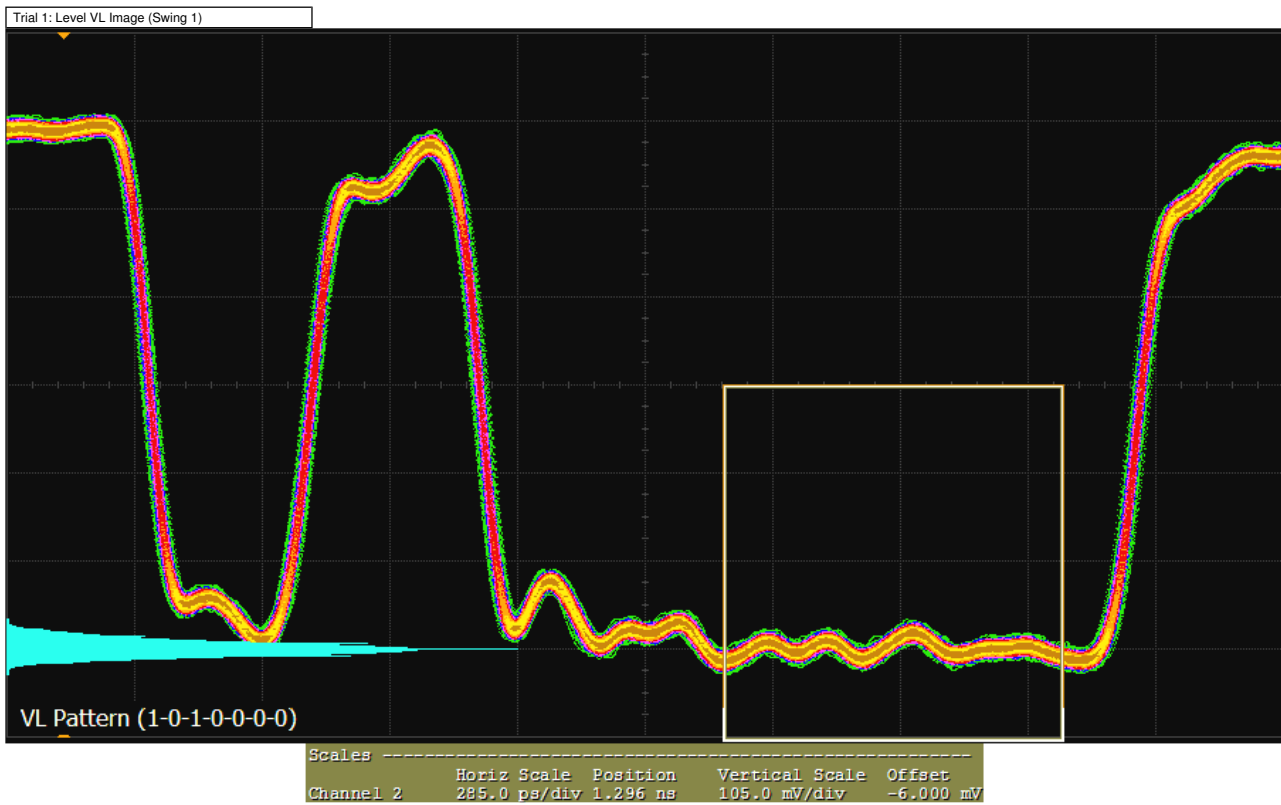
Trial 1

Trial 1: Level VH Image (Swing 1)

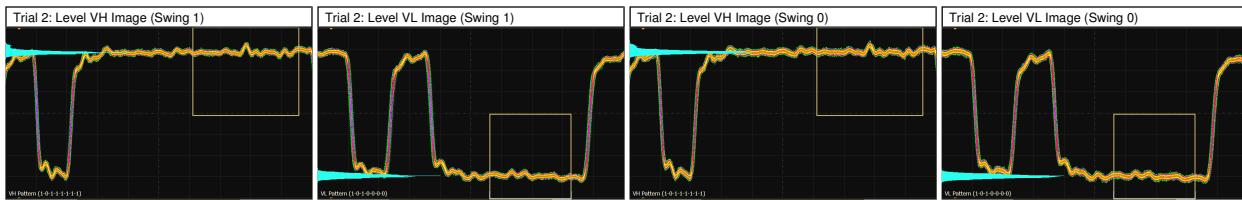


Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 2		326.0 ps/div	1.481 ns	105.0 mV/div	-6.000 mV





Trial 2



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✓ Lane 2 - Non-PreEmphasis Level Test (Swing 1/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [800.0 mdB to 6.0000 dB] **Lane 2 Non-PreEmphasis Level Test (Swing 1/Swing 0) (Worst of 2 Trials)** 2.9466 dB **# Trials Run:** 2 **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

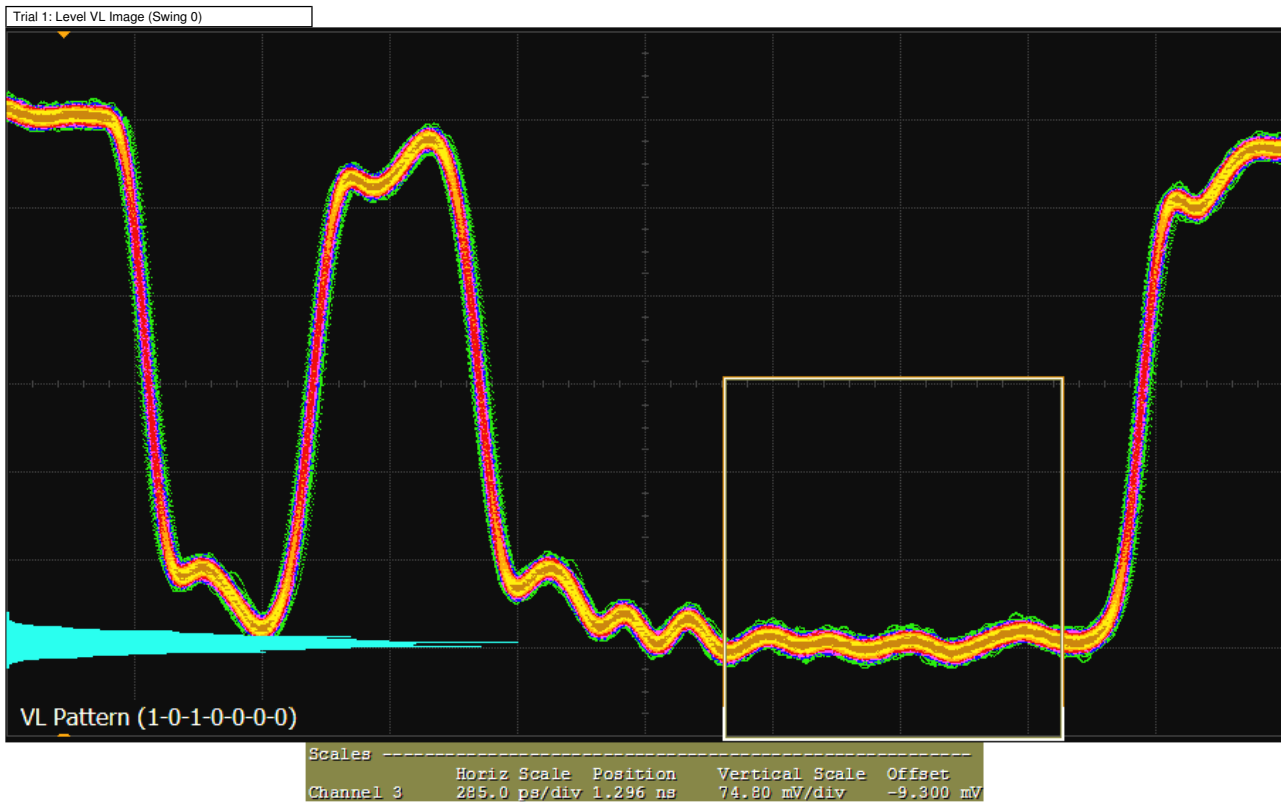
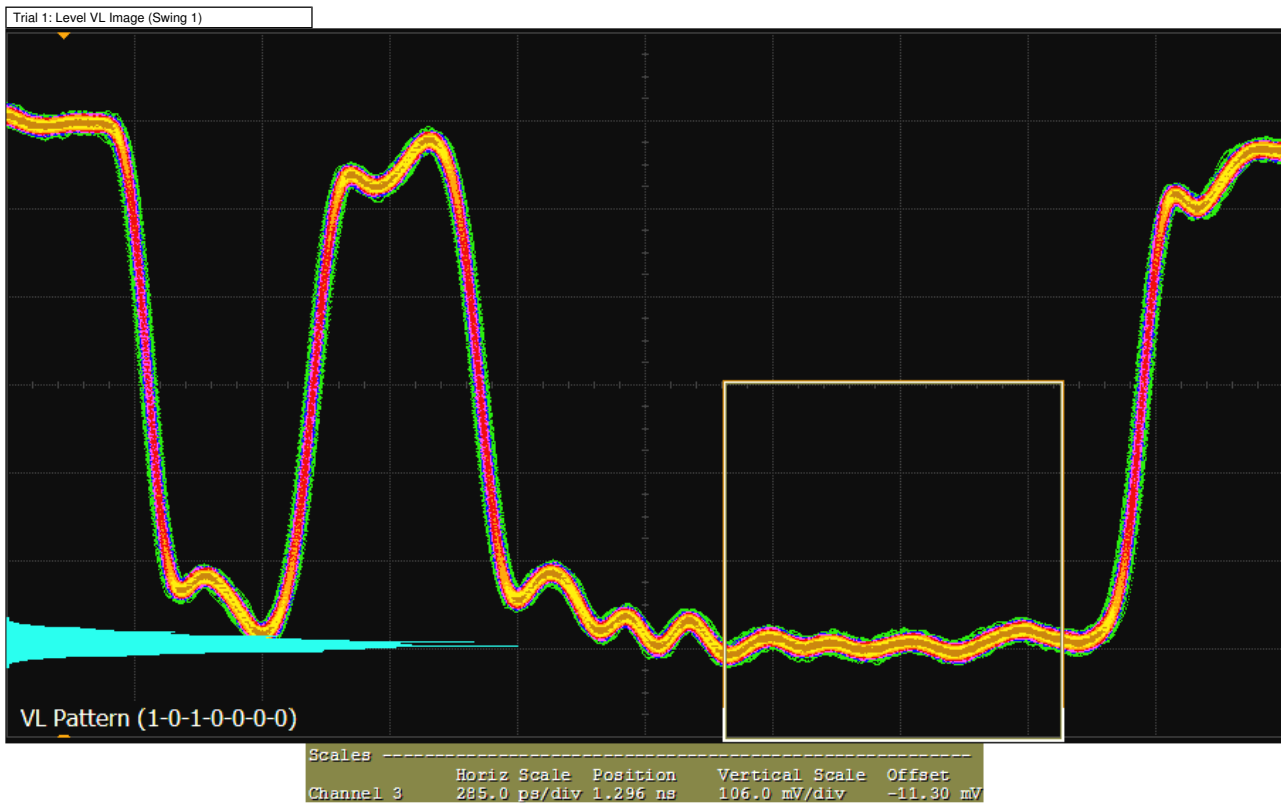
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 1)	Level VL Image (Swing 0)	Level VH Image (Swing 0)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	VTop (Swing 0)	VBase (Swing 0)	VSwing (Swing 0)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitF
	Avg	3.062 dB	43.50 %																				
	StdDev	163.4 mdB	3.143 %																				
	Range	231.0 mdB	4.444 %																				
	Min	2.947 dB	41.28 %																				
	Max	3.178 dB	45.73 %																				
	Sum	6.124 dB	87.01 %																				
✓	Trial 1 (Worst)	2.9466 dB	41.3%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	298.874 mV	322.942 mV	621.816 mV	210.916 mV	232.009 mV	442.925 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2	3.1777 dB	45.7%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	296.021 mV	313.957 mV	609.977 mV	202.957 mV	220.131 mV	423.088 mV	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

Trial 1

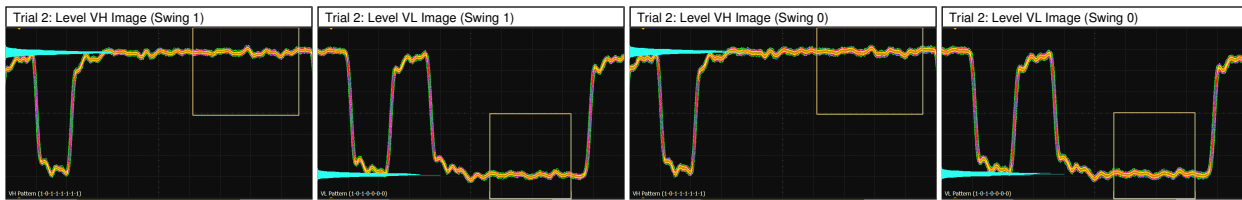
Trial 1: Level VH Image (Swing 1)



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	326.0 ps/div	1.481 ns	106.0 mV/div	-11.30 mV	



Trial 2



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✓ Lane 3 - Non-PreEmphasis Level Test (Swing 1/ Swing 0) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

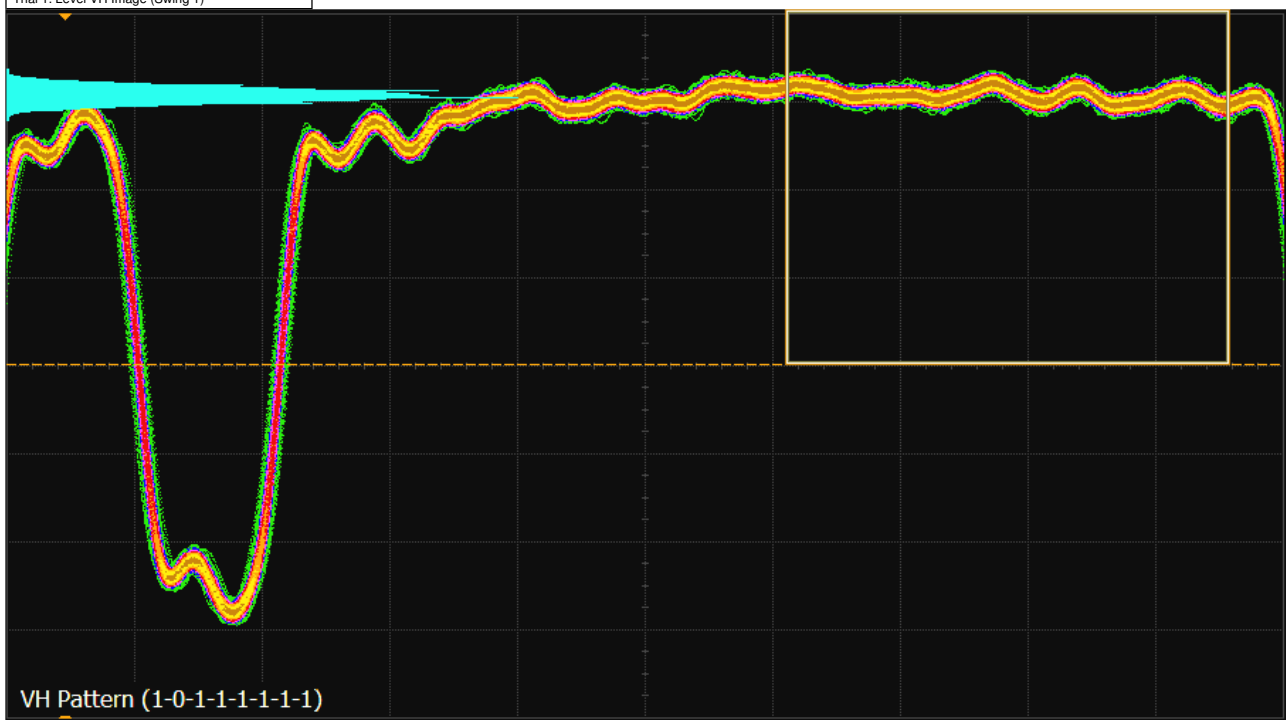
Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [800.0 mdB to 6.0000 dB] **Lane 3 Non-PreEmphasis Level Test (Swing 1/Swing 0) (Worst of 2 Trials)** 3.1453 dB **# Trials Run:** 2 **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

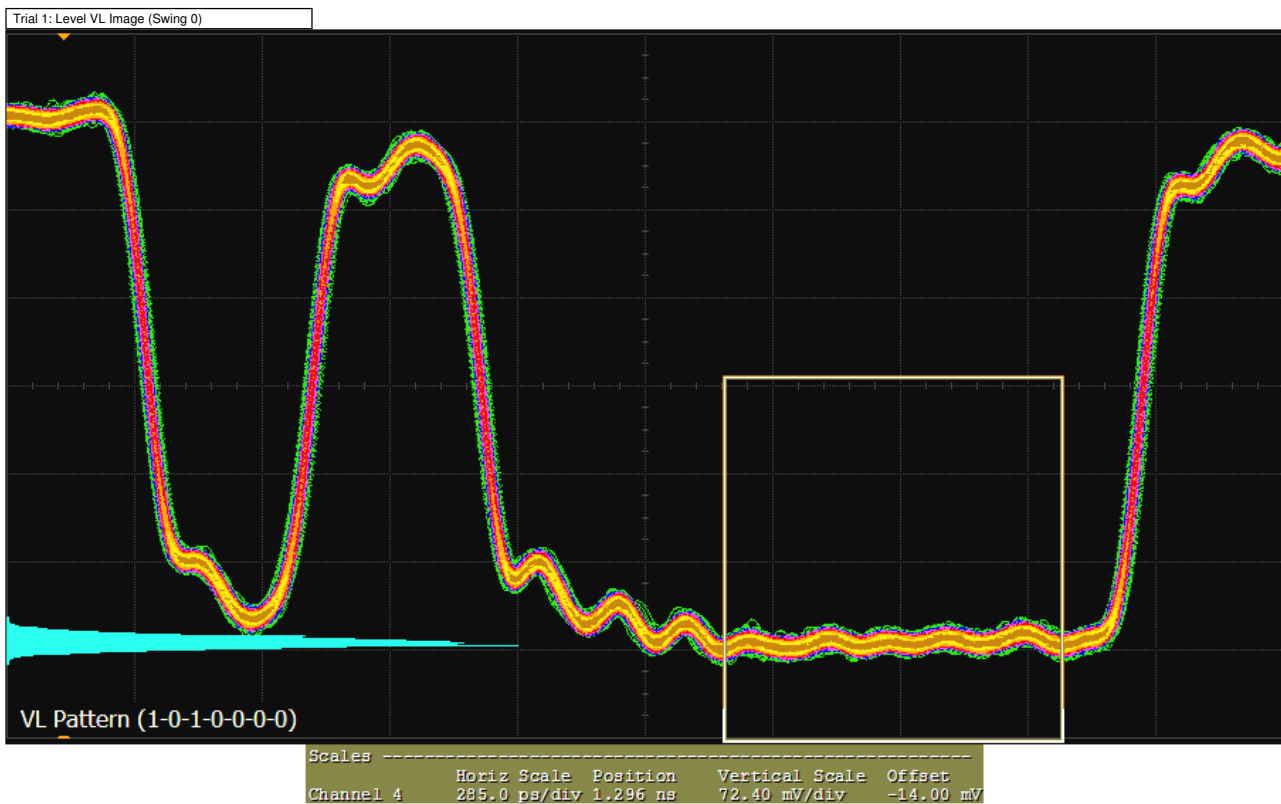
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 1)	Level VL Image (Swing 0)	Level VH Image (Swing 0)	Level VL Image (Swing 1)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 1)	VBase (Swing 1)	VSwing (Swing 1)	VTop (Swing 0)	VBase (Swing 0)	VSwing (Swing 0)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitR
	<b>Avg</b>	3.151 dB	45.21 %																				
	<b>StdDev</b>	7.915 mdB	152.3 m%																				
	<b>Range</b>	11.19 mdB	215.4 m%																				
	<b>Min</b>	3.145 dB	45.10 %																				
	<b>Max</b>	3.157 dB	45.32 %																				
	<b>Sum</b>	6.302 dB	90.42 %																				
✓	Trial 1 (Worst)	3.1453 dB	45.1%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	288.867 mV	311.442 mV	600.309 mV	198.768 mV	219.168 mV	417.935 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gbp
✓	Trial 2	3.1565 dB	45.3%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	286.992 mV	309.957 mV	596.950 mV	196.925 mV	218.137 mV	415.061 mV	Compliance Layer Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbp

Trial 1

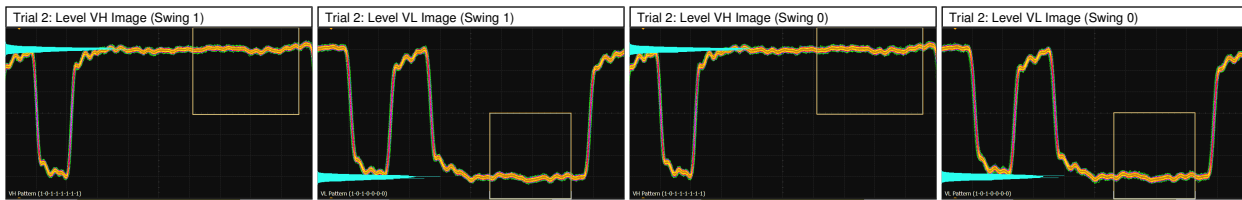
Trial 1: Level VH Image (Swing 1)



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	326.0 ps/div	1.482 ns	102.0 mV/div	-17.30 mV



Trial 2



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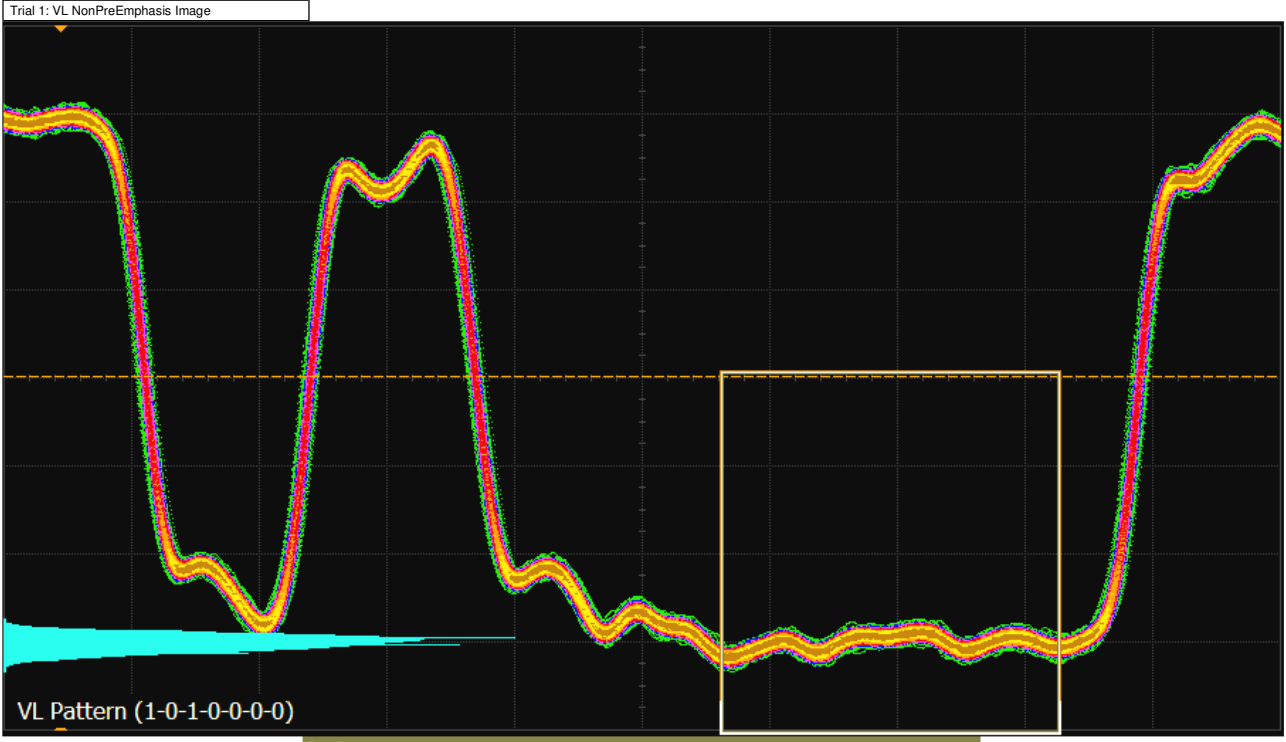
**✘ Lane 0 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 4 Trials) -2.424 dB** | **# Trials Run: 4** | **Worst Trial: Trial 3**

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-2.375 dB	-248.5 %													
	StdDev	47.35 mdB	2.943 %													
	Range	104.7 mdB	6.500 %													
	Min	-2.424 dB	-251.5 %													
	Max	-2.320 dB	-245.0 %													
	Sum	-9.501 dB	-993.8 %													
✘	Trial 1	-2.320 dB	-	(See image)	(See image)	(See image)	(See image)	1000	790.553 mV	689.765 mV	1.185 dB	2.7 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 2	-2.354 dB	-	(See image)	(See image)	(See image)	(See image)	1000	563.304 mV	491.273 mV	1.188 dB	2.7 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 3 (Worst)	-2.424 dB	-	(See image)	(See image)	(See image)	(See image)	1000	915.695 mV	683.712 mV	2.538 dB	1.62 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 4	-2.403 dB	-	(See image)	(See image)	(See image)	(See image)	1000	660.318 mV	483.965 mV	2.699 dB	1.62 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0

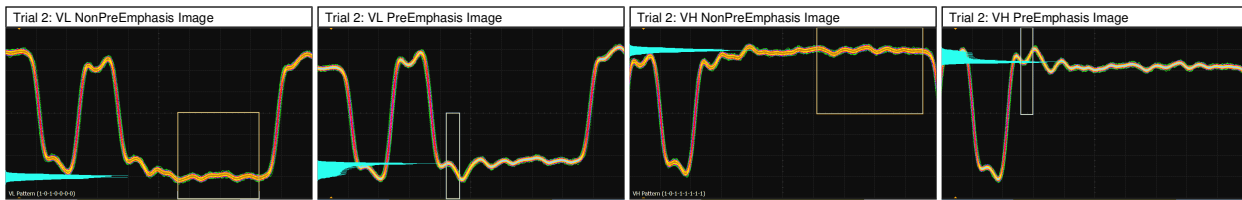
Trial 1



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	285.0 ps/div	1.296 ns	103.0 mV/div	-11.30 mV

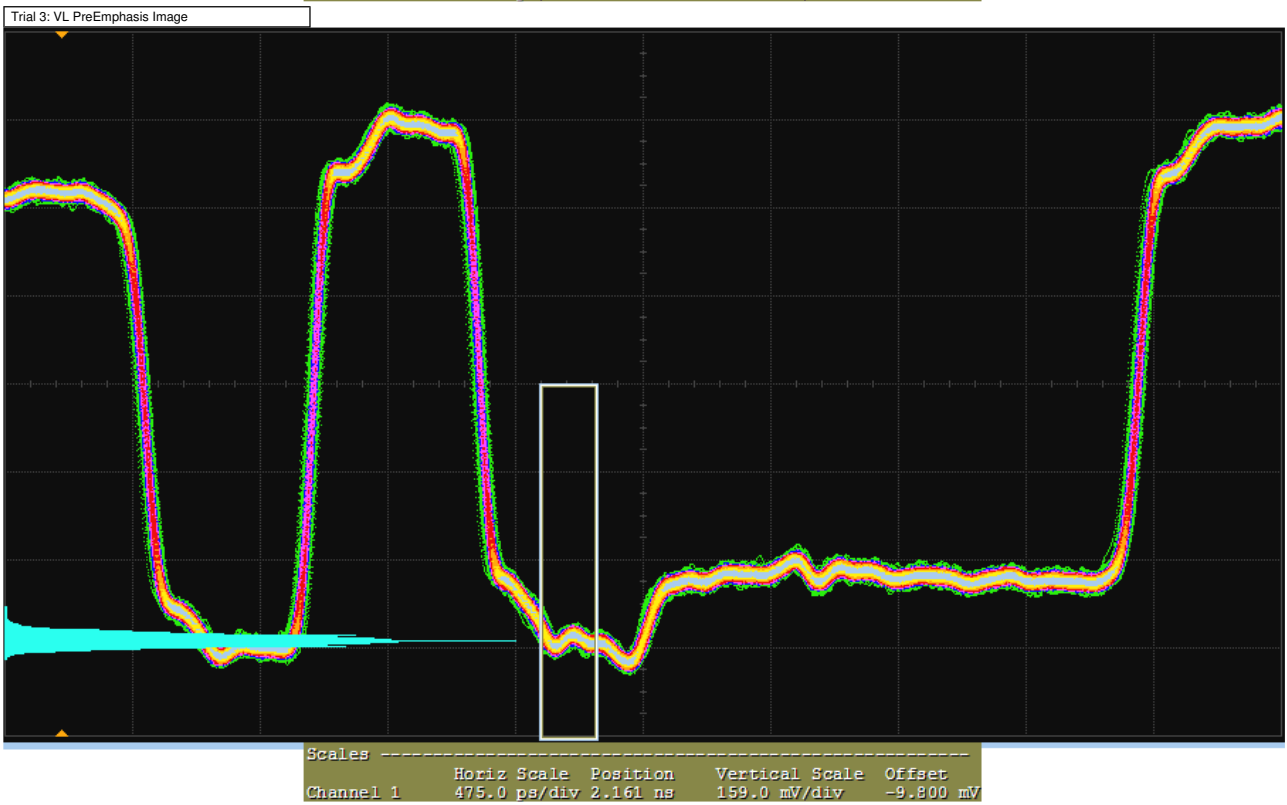
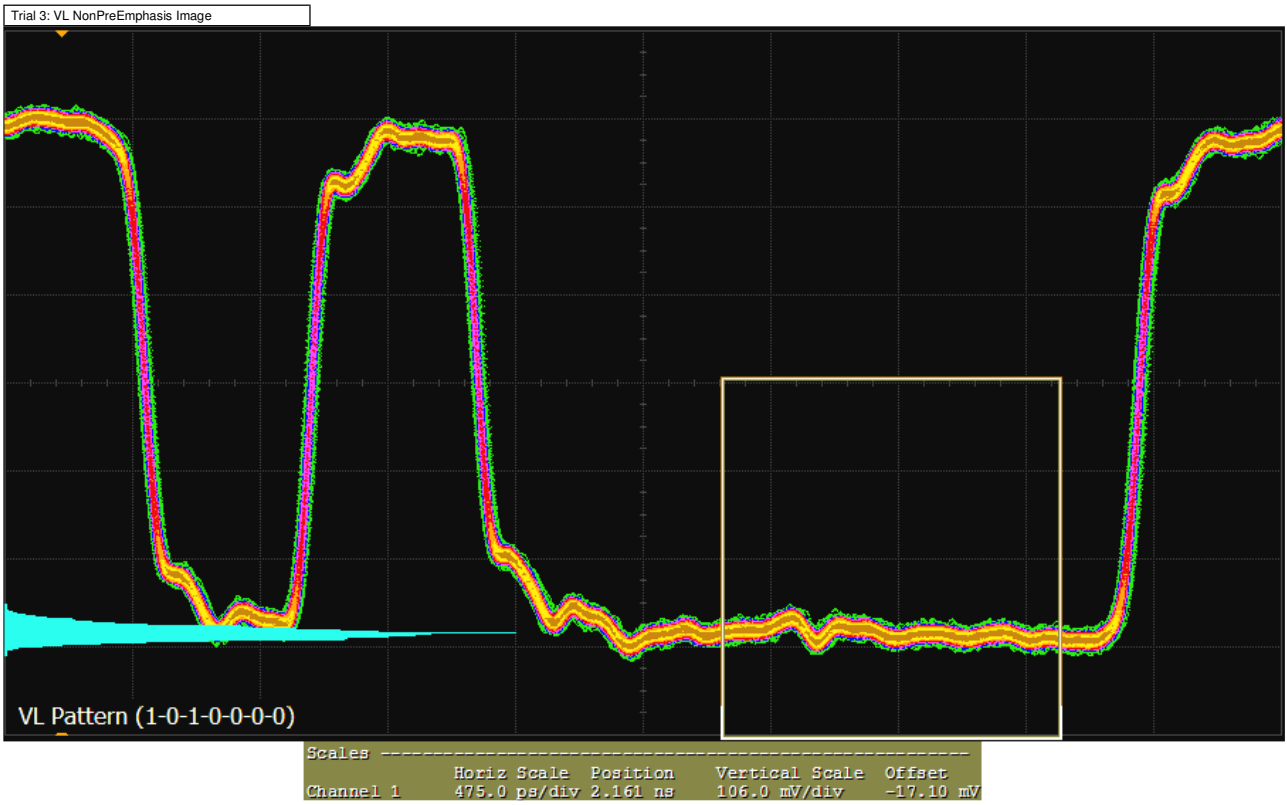


Trial 2

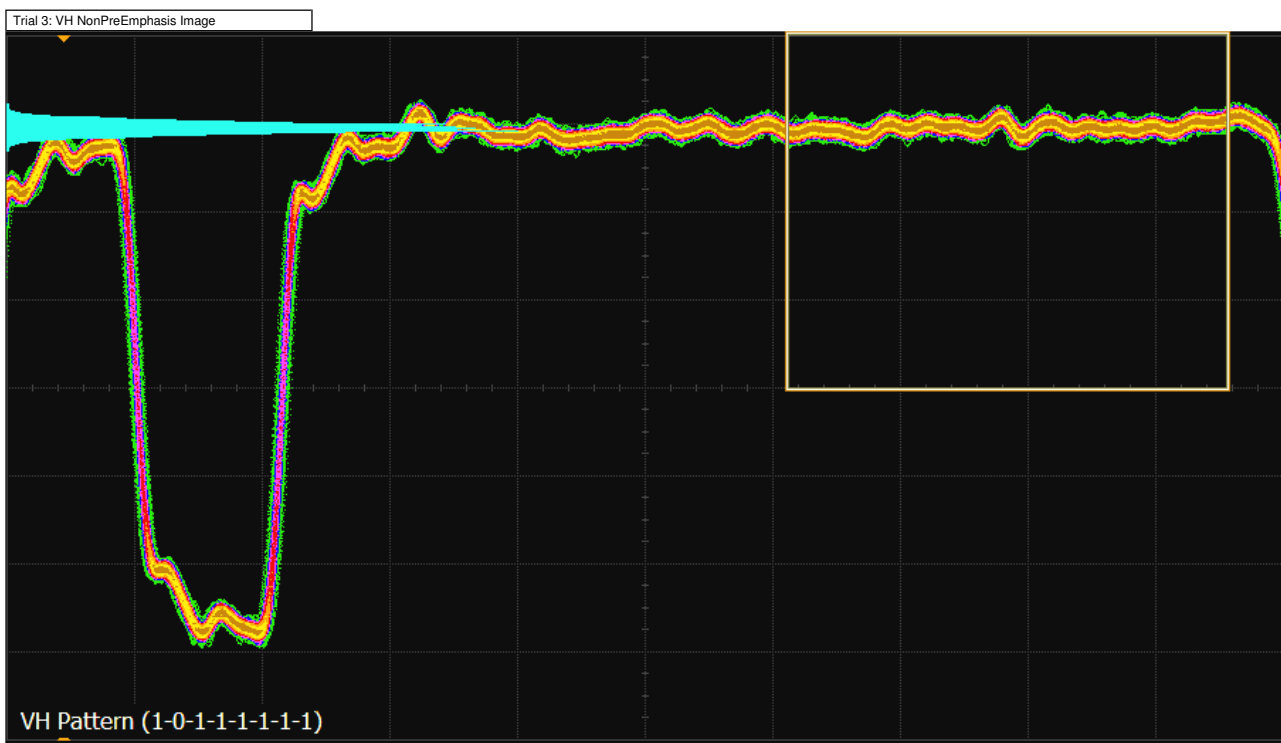


Trial 3

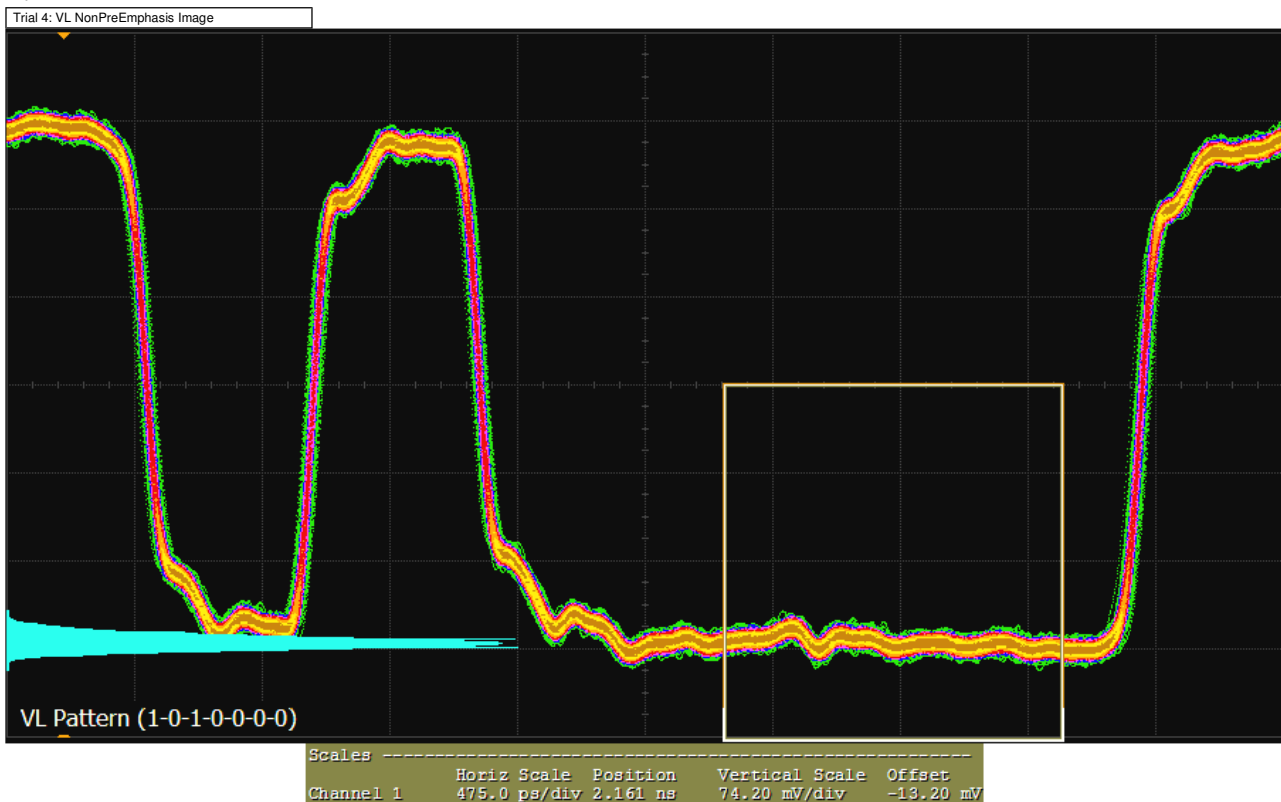








Trial 4



Trial 4: VL PreEmphasis Image



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	117.0 mV/div	-10.10 mV

Trial 4: VH PreEmphasis Image



Scales				
Channel 1	Horiz Scale	Position	Vertical Scale	Offset
	543.0 ps/div	2.469 ns	117.0 mV/div	-10.10 mV

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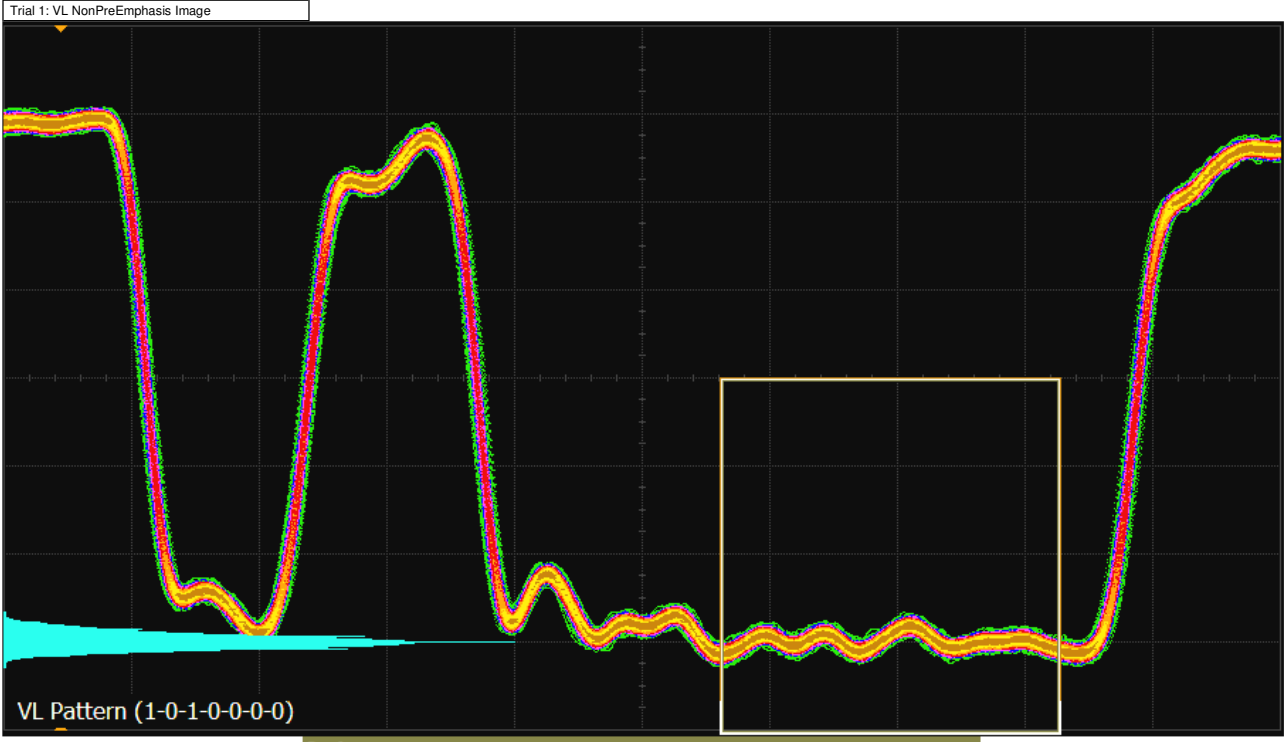
✓ Lane 1 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 1.600 dB | PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 4 Trials) 3.026 dB | # Trials Run: 4 | Worst Trial: Trial 1

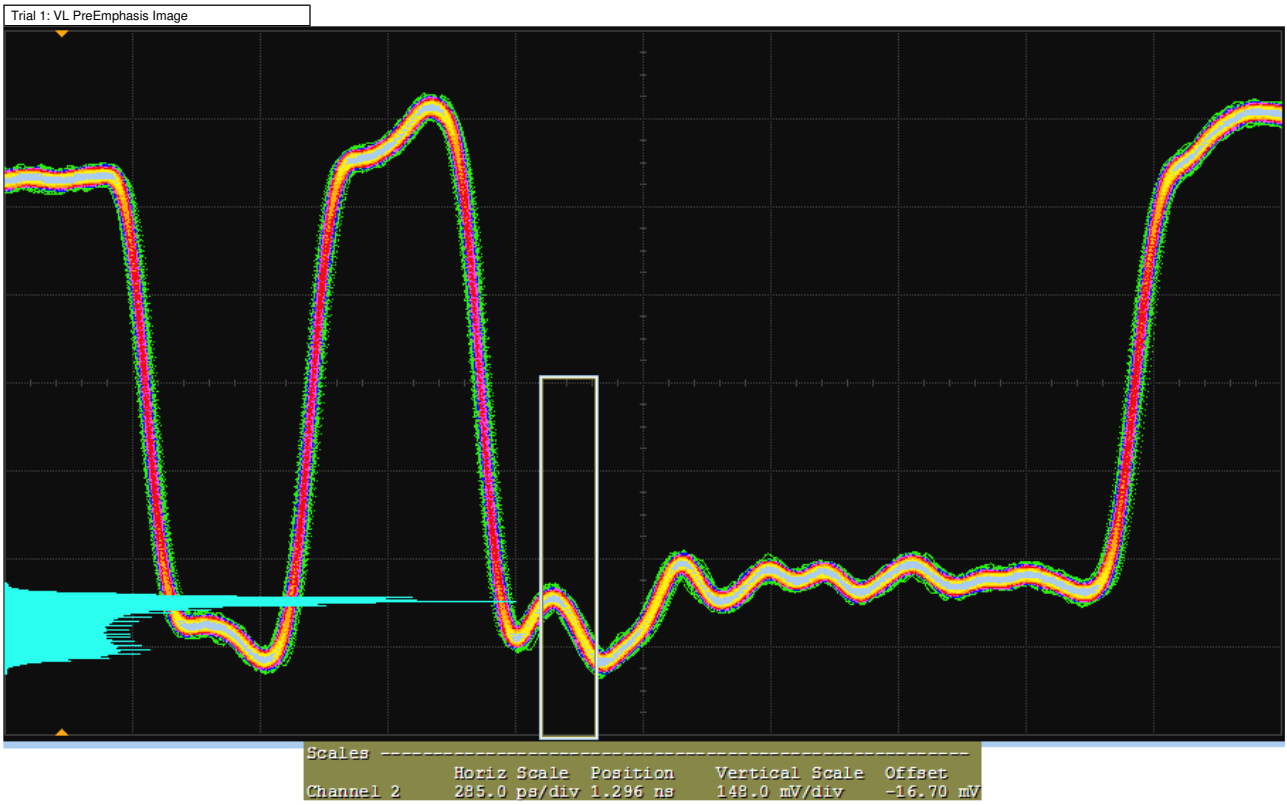
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	3.181 dB	98.80 %													
	StdDev	123.5 mdB	7.703 %													
	Range	300.6 mdB	18.75 %													
	Min	3.026 dB	89.13 %													
	Max	3.326 dB	107.9 %													
	Sum	12.72 dB	395.2 %													
✓	Trial 1 (Worst)	3.026 dB	89.1%	(See image)	(See image)	(See image)	(See image)	1000	823.091 mV	687.069 mV	1.569 dB	2.7 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 2	3.201 dB	100.1%	(See image)	(See image)	(See image)	(See image)	1000	592.110 mV	490.382 mV	1.637 dB	2.7 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 3	3.170 dB	98.1%	(See image)	(See image)	(See image)	(See image)	1000	906.273 mV	675.602 mV	2.551 dB	1.62 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 4	3.326 dB	107.9%	(See image)	(See image)	(See image)	(See image)	1000	658.294 mV	486.701 mV	2.623 dB	1.62 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0

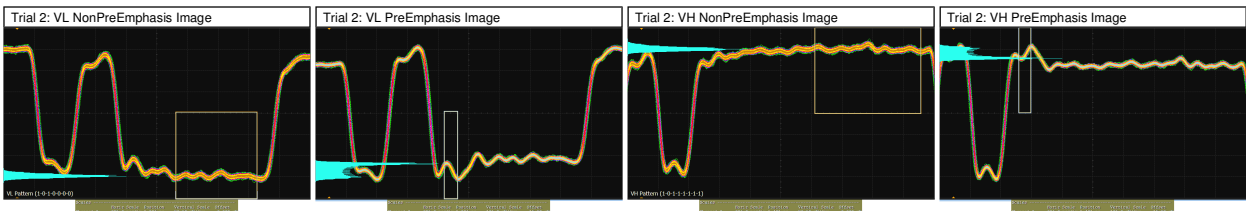
Trial 1



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	285.0 ps/div	1.296 ns	105.0 mV/div	-6.000 mV	



Trial 2



Trial 3

Trial 3: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	475.0 ps/div	2.161 ns	105.0 mV/div	-2.300 mV

Trial 3: VL PreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	475.0 ps/div	2.161 ns	161.0 mV/div	-7.500 mV

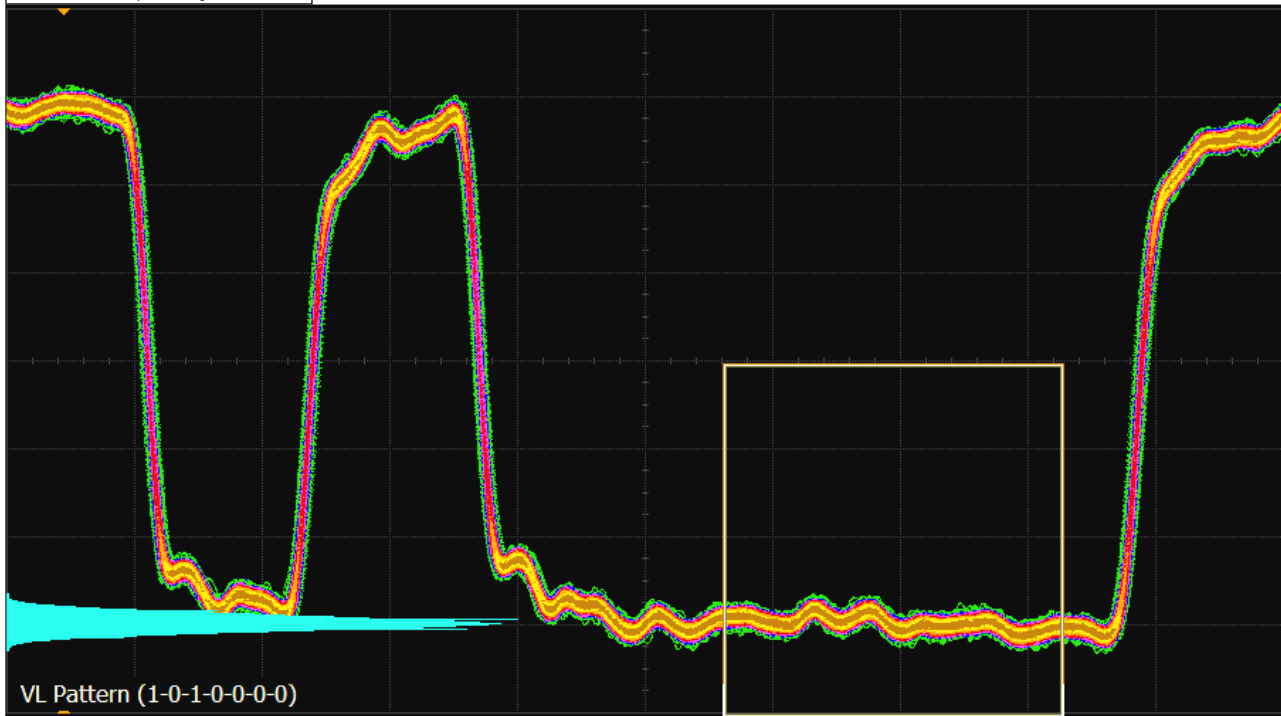
Trial 3: VH NonPreEmphasis Image



Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	543.0 ps/div	2.469 ns	105.0 mV/div	-2.300 mV

Trial 4

Trial 4: VL NonPreEmphasis Image



Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	75.10 mV/div	-4.800 mV

Trial 4: VL PreEmphasis Image



Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	115.0 mV/div	-8.100 mV

Trial 4: VH PreEmphasis Image



Scales				
Channel 2	Horiz Scale	Position	Vertical Scale	Offset
	543.0 ps/div	2.469 ns	115.0 mV/div	-8.100 mV

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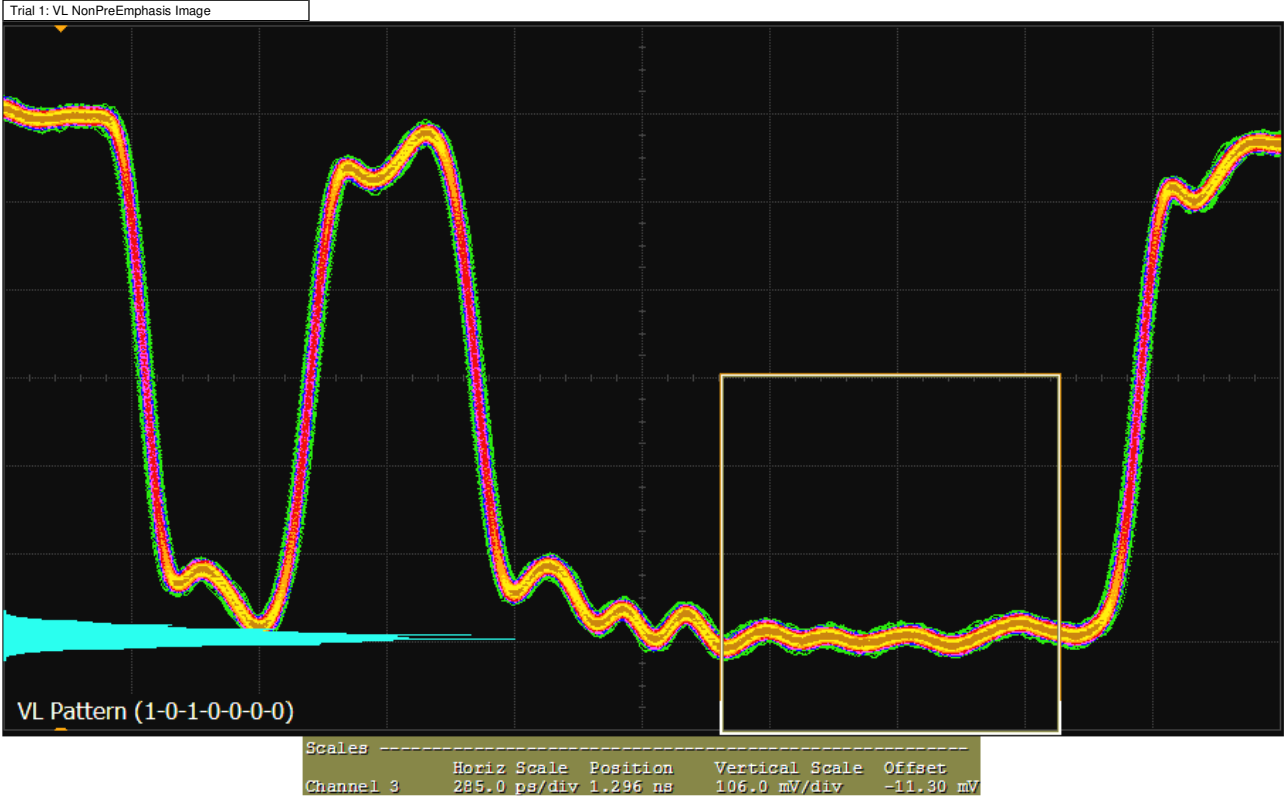
✓ Lane 2 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: >= 1.600 dB | PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 4 Trials) 2.133 dB | # Trials Run: 4 | Worst Trial: Trial 1

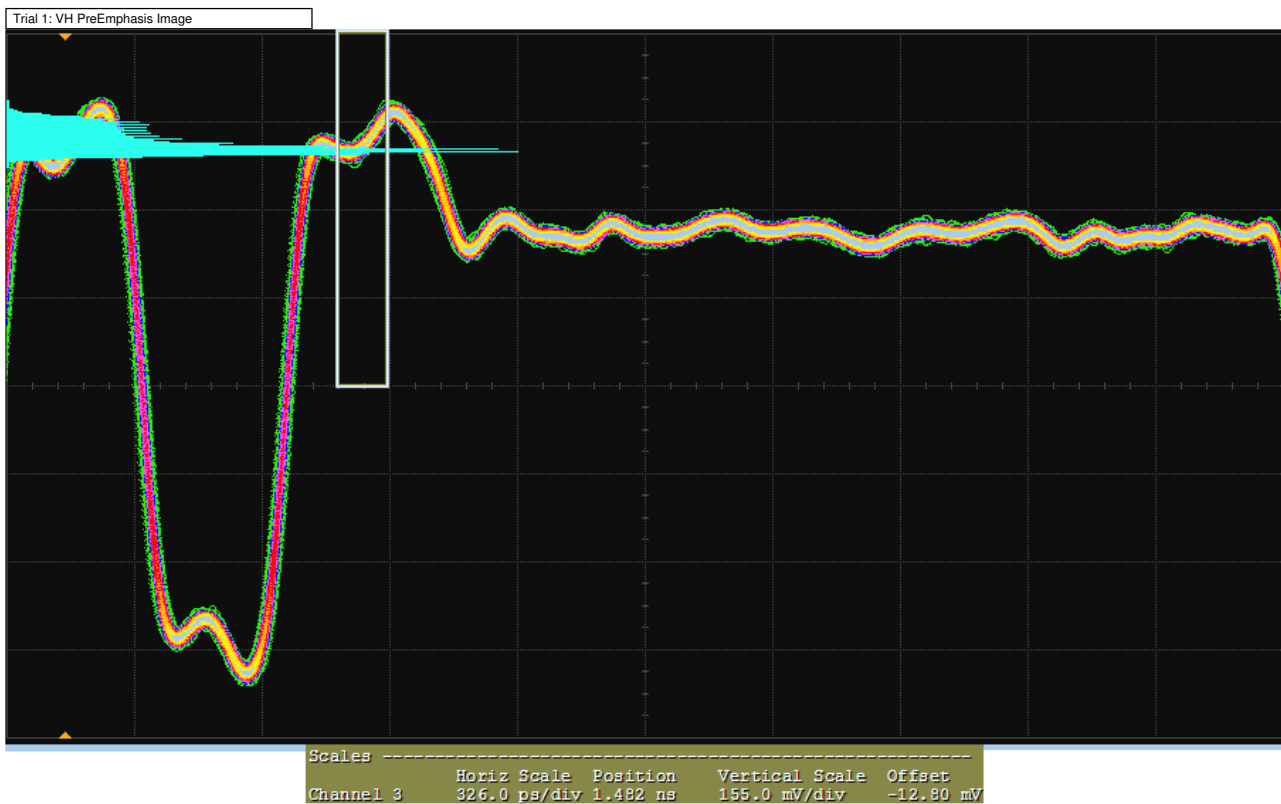
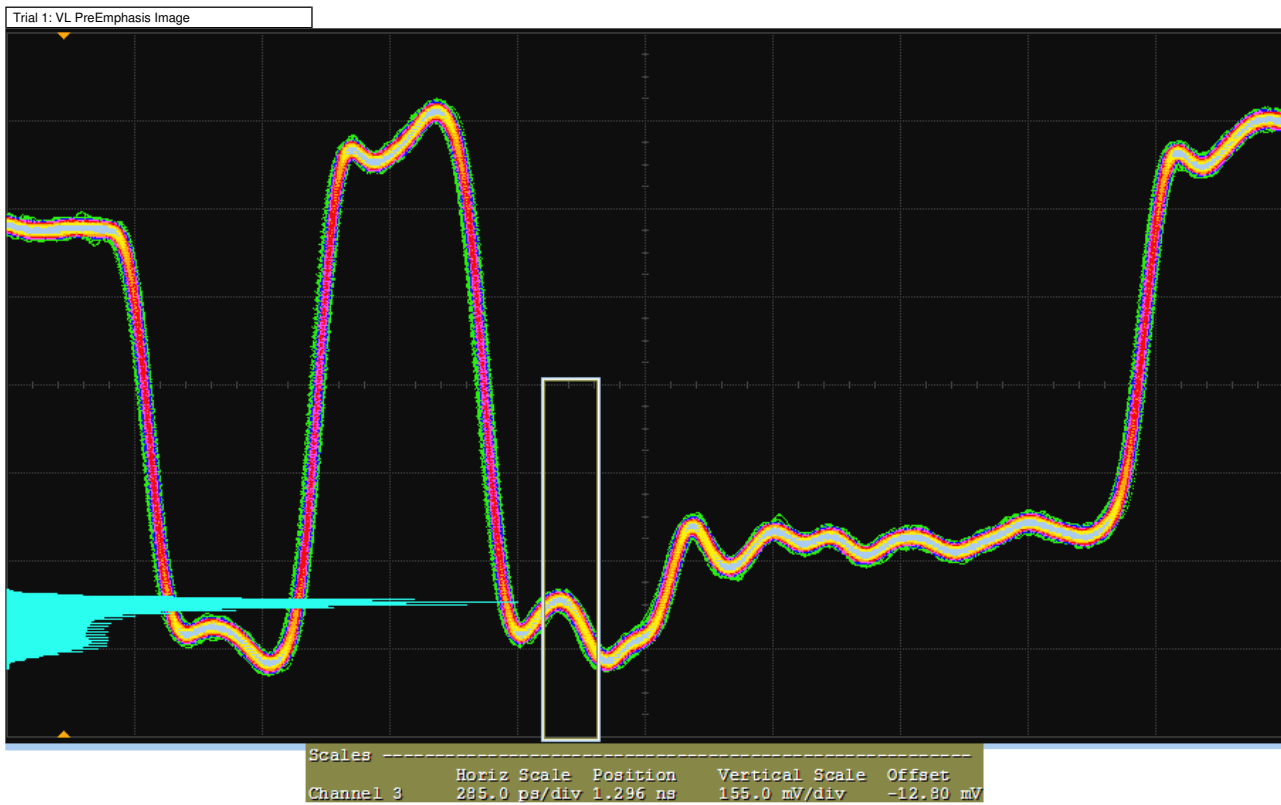
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	2.293 dB	43.31 %													
	StdDev	145.1 mdB	9.066 %													
	Range	305.2 mdB	19.06 %													
	Min	2.133 dB	33.31 %													
	Max	2.438 dB	52.38 %													
	Sum	9.171 dB	173.3 %													
✓	Trial 1 (Worst)	2.133 dB	33.3%	(See image)	(See image)	(See image)	(See image)	1000	874.309 mV	568.237 mV	3.743 dB	2.7 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 2	2.391 dB	49.4%	(See image)	(See image)	(See image)	(See image)	1000	662.205 mV	418.478 mV	3.986 dB	2.7 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 3	2.210 dB	38.1%	(See image)	(See image)	(See image)	(See image)	1000	944.908 mV	549.198 mV	4.713 dB	1.62 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 4	2.438 dB	52.4%	(See image)	(See image)	(See image)	(See image)	1000	713.911 mV	405.453 mV	4.914 dB	1.62 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0

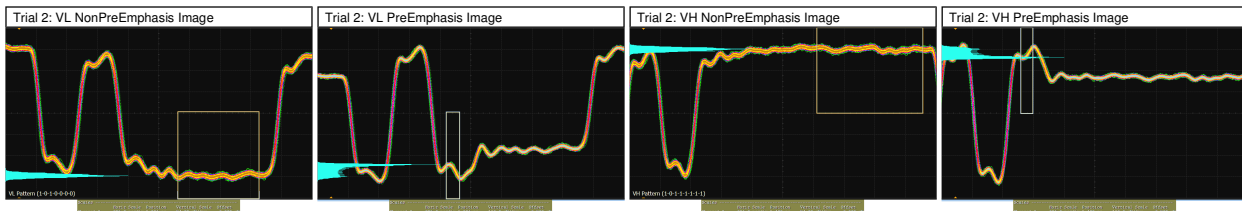
Trial 1



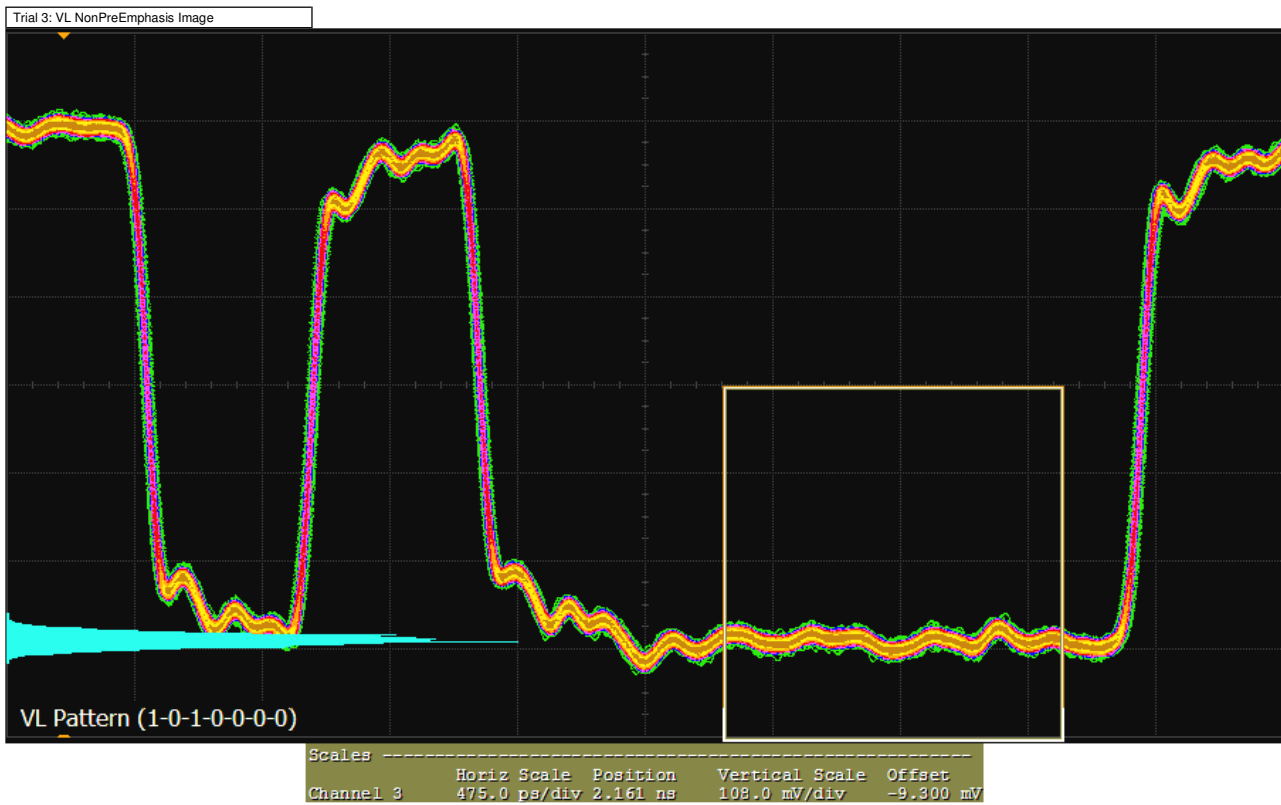




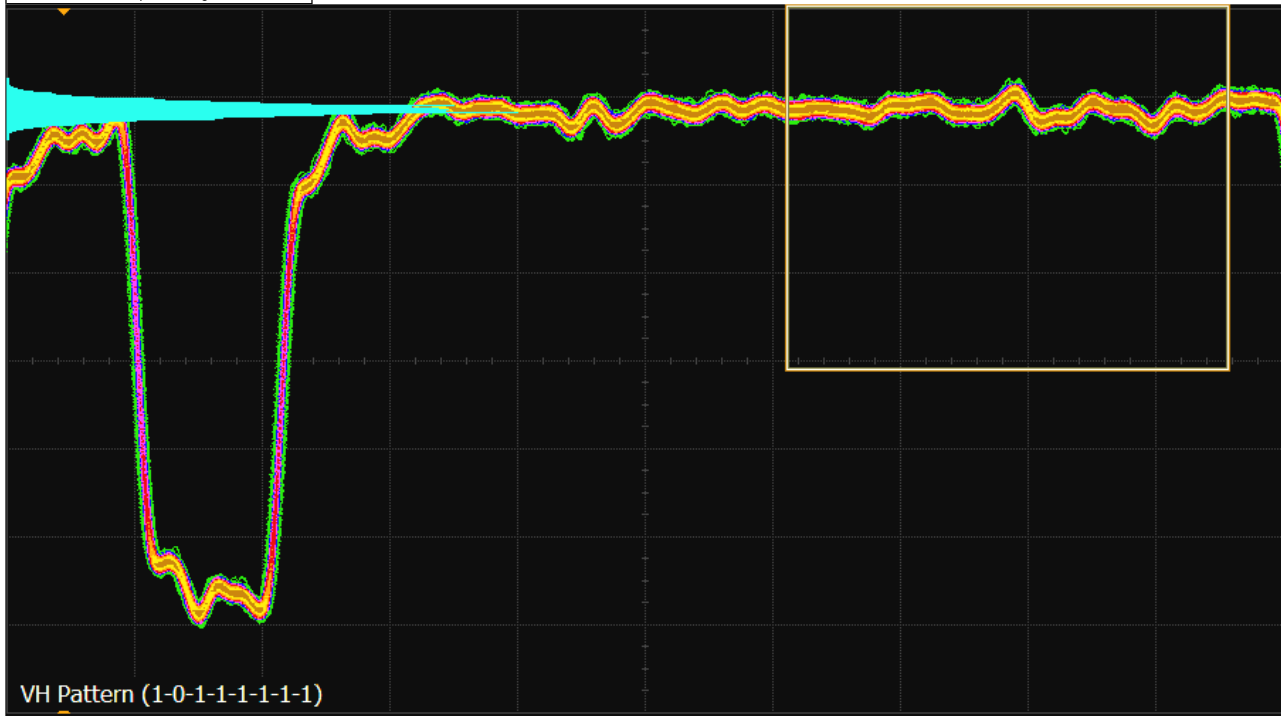
Trial 2



Trial 3



Trial 3: VH NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	543.0 ps/div	2.469 ns	108.0 mV/div	-9.300 mV

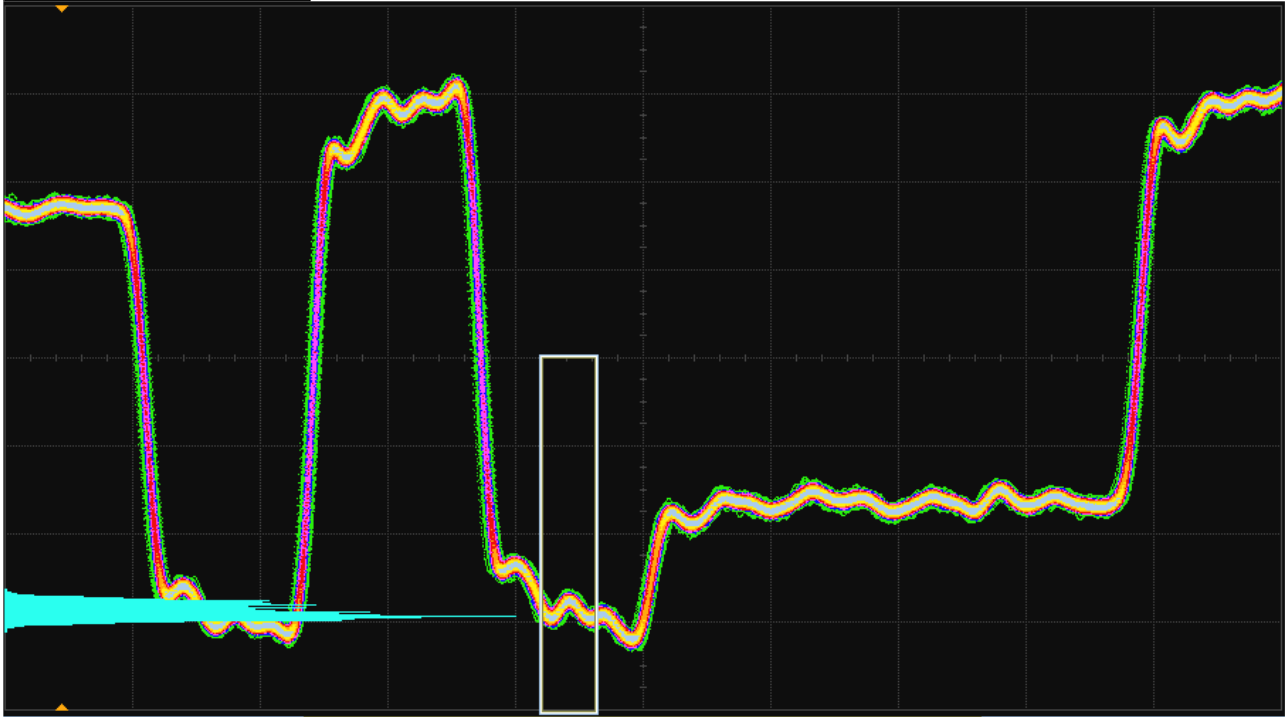
Trial 4

Trial 4: VL NonPreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	73.40 mV/div	-11.30 mV

Trial 4: VL PreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	475.0 ps/div	2.161 ns	122.0 mV/div	-11.60 mV

Trial 4: VH PreEmphasis Image



Scales	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	543.0 ps/div	2.469 ns	122.0 mV/div	-11.60 mV

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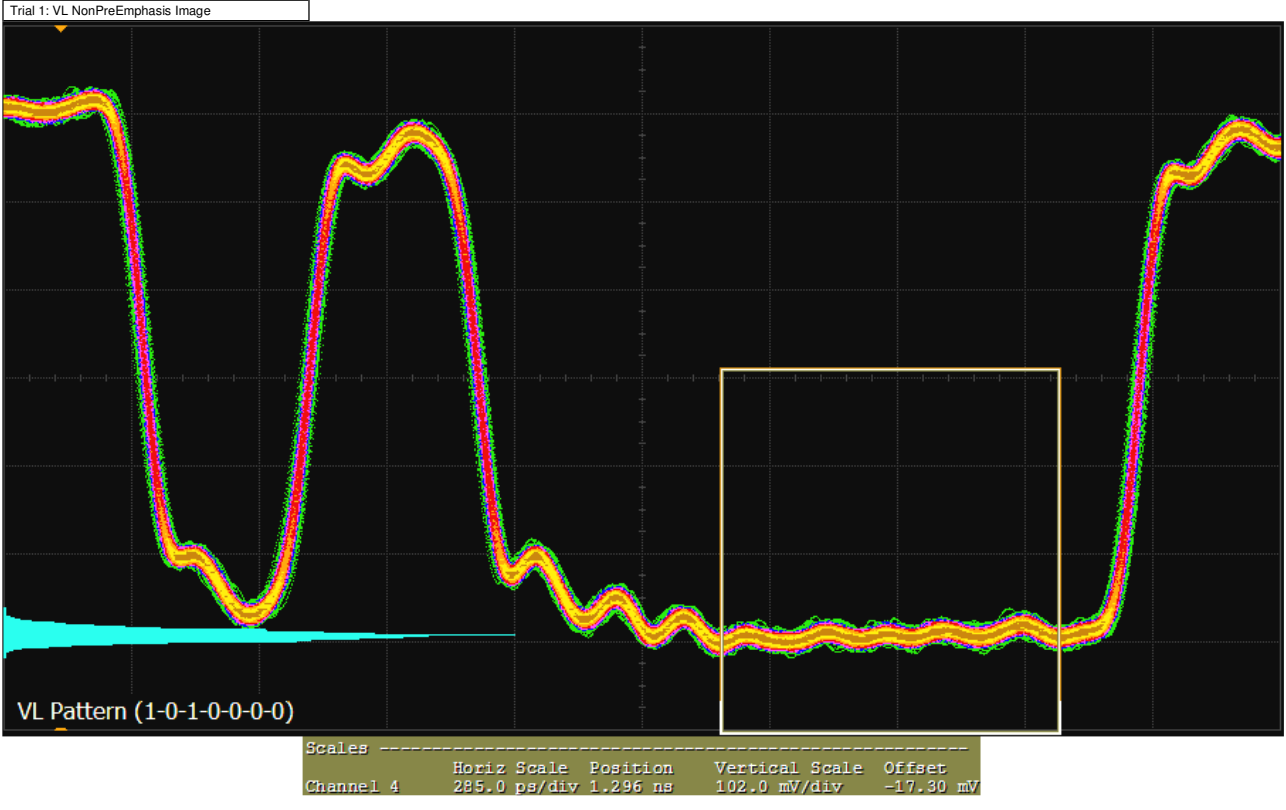
**✘ Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

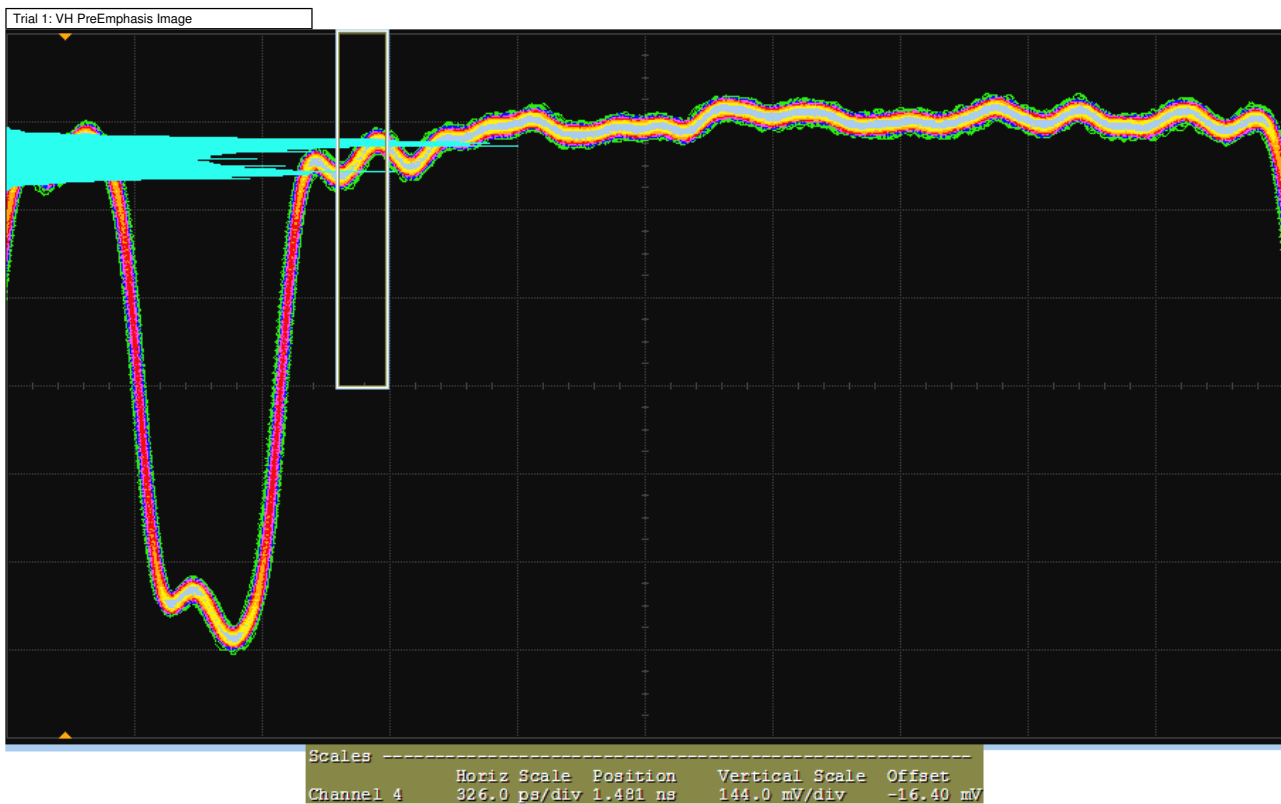
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 2) - PreEmphasis(Pre-emphasis 1) (Worst of 4 Trials) 25 mdB** | **# Trials Run: 4** | **Worst Trial: Trial 4**

Overall Summary + details of 4 worst trials

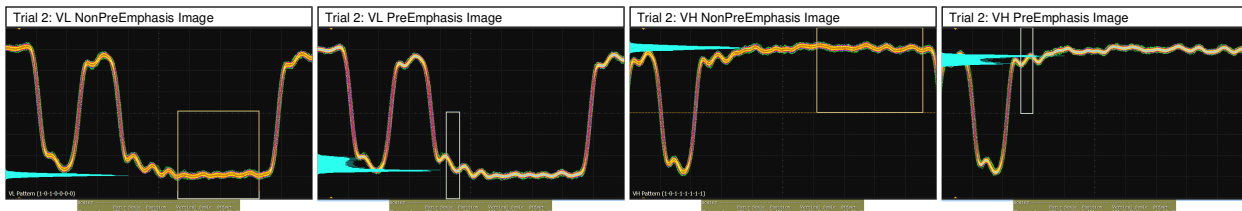
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	51.05 mdB	-96.81 %													
	StdDev	29.76 mdB	1.869 %													
	Range	68.59 mdB	4.313 %													
	Min	25.23 mdB	-98.44 %													
	Max	93.82 mdB	-94.13 %													
	Sum	204.2 mdB	-387.3 %													
✘	Trial 1	94 mdB	-94.1% (See image)	(See image)	(See image)	(See image)	(See image)	1000	731.738 mV	844.177 mV	-1.242 dB	2.7 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 2	45 mdB	-97.2% (See image)	(See image)	(See image)	(See image)	(See image)	1000	508.781 mV	597.463 mV	-1.396 dB	2.7 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 3	40 mdB	-97.5% (See image)	(See image)	(See image)	(See image)	(See image)	1000	765.131 mV	844.786 mV	-860 mdB	1.62 Gbps	1 2	Swing Pre-emphasis	SSC Disabled	Level 0
✘	Trial 4 (Worst)	25 mdB	-98.4% (See image)	(See image)	(See image)	(See image)	(See image)	1000	533.143 mV	595.386 mV	-959 mdB	1.62 Gbps	0 2	Swing Pre-emphasis	SSC Disabled	Level 0

Trial 1

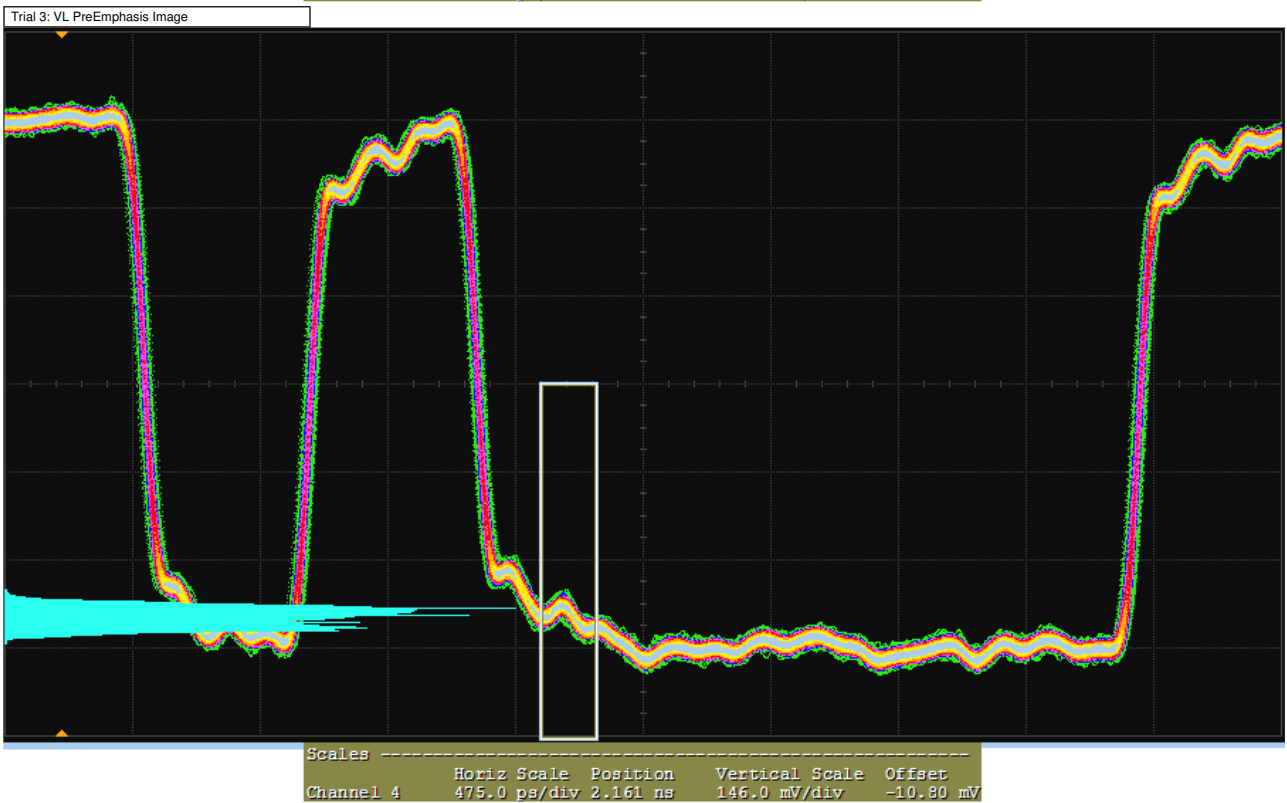
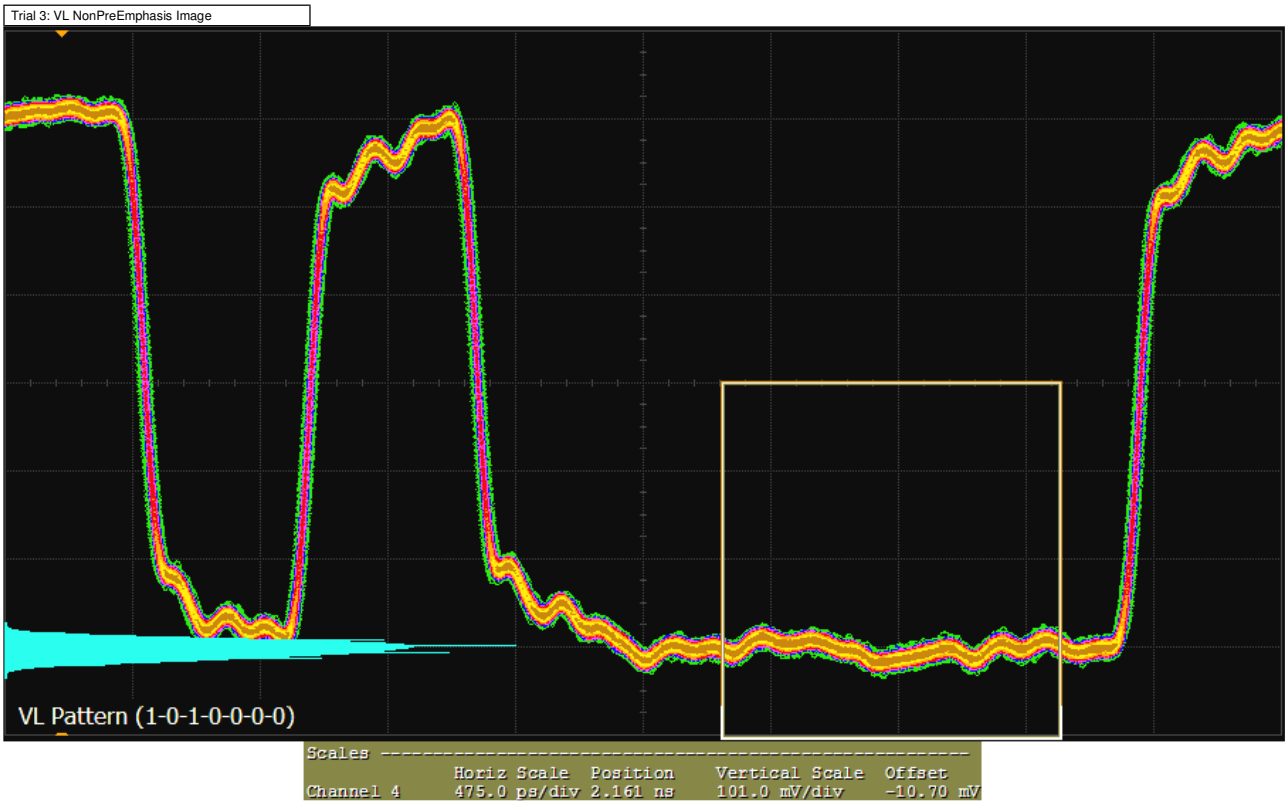




Trial 2



Trial 3



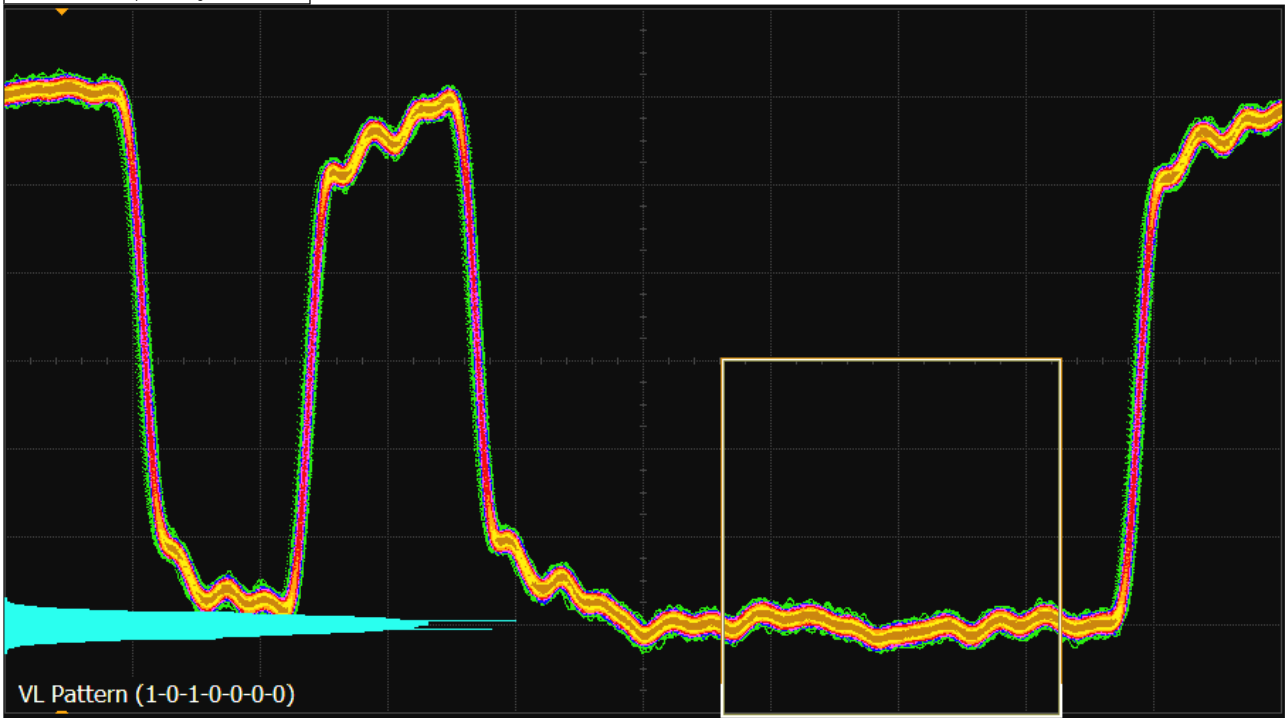
Trial 3: VH NonPreEmphasis Image



Scales				
Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	543.0 ps/div	2.469 ns	101.0 mV/div	-10.70 mV

Trial 4

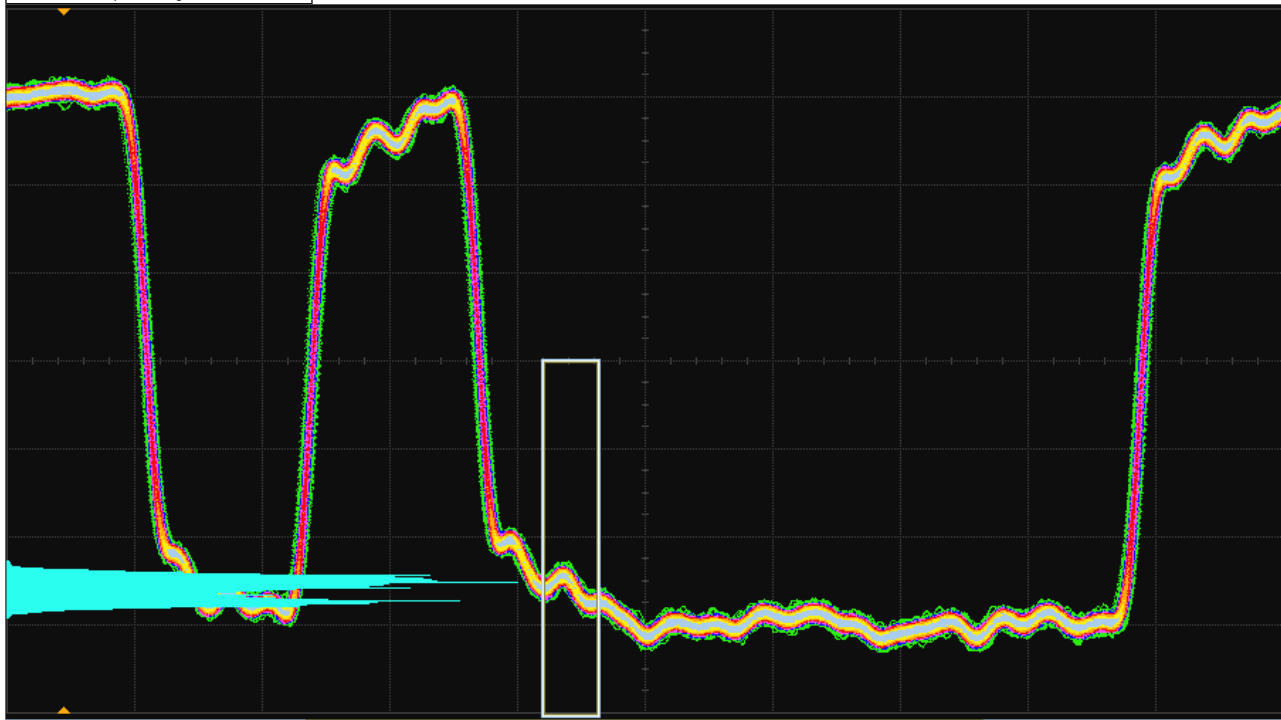
Trial 4: VL NonPreEmphasis Image



Scales				
Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	71.70 mV/div	-11.90 mV



Trial 4: VL PreEmphasis Image



Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	475.0 ps/div	2.161 ns	102.0 mV/div	-10.90 mV

Trial 4: VH PreEmphasis Image



Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	543.0 ps/div	2.469 ns	102.0 mV/div	-10.90 mV

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✓ Lane 0 - Non-Transition Voltage Range Measurement (Swing 1) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m | **Non-Transition Voltage Range (Worst of 2 Trials)** 818 m | # Trials Run: 2 | Worst Trial: Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	819.5 m	15.75 %	NaN V										
	StdDev	1.945 m	299.6 m%	NaN V										
	Range	2.751 m	423.7 m%	-Infinity V										
	Min	818.1 m	15.54 %	Infinity V										
	Max	820.8 m	15.96 %	-Infinity V										
	Sum	1.639	31.50 %	0.000 V										
✓	Trial 1	821 m	16.0%	(no value)	608.543 mV	499.512 mV	689.765 mV	689.765 mV	499.512 mV	2.7 Gbps	Swing 1 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 2 (Worst)	818 m	15.5%	(no value)	602.664 mV	493.028 mV	683.712 mV	683.712 mV	493.028 mV	1.62 Gbps	Swing 1 2	Pre-emphasis 2	SSC Disabled	Level 0

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✓ Lane 1 - Non-Transition Voltage Range Measurement (Swing 1) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m | **Non-Transition Voltage Range (Worst of 2 Trials)** 1.118 | **# Trials Run:** 2 | **Worst Trial:** Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	1.122	58.47 %	NaN V										
	StdDev	5.943 m	799.0 m%	NaN V										
	Range	8.404 m	1.130 %	-Infinity V										
	Min	1.118	57.91 %	-Infinity V										
	Max	1.126	59.04 %	-Infinity V										
	Sum	2.244	116.9 %	0.000 V										
✓	Trial 1	1.126	59.0%	(no value)	610.155 mV	740.331 mV	687.069 mV	740.331 mV	687.069 mV	2.7 Gbps	Swing 1 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 2 (Worst)	1.118	57.9%	(no value)	604.484 mV	735.223 mV	675.602 mV	735.223 mV	675.602 mV	1.62 Gbps	Swing 1 2	Pre-emphasis 2	SSC Disabled	Level 0

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✓ Lane 2 - Non-Transition Voltage Range Measurement (Swing 1) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range (Worst of 2 Trials) 900 m # Trials Run: 2 Worst Trial: Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	<i>907.1 m</i>	<i>28.11 %</i>	<i>NaN V</i>										
	<i>StdDev</i>	<i>9.531 m</i>	<i>1.398 %</i>	<i>NaN V</i>										
	<i>Range</i>	<i>13.48 m</i>	<i>1.977 %</i>	<i>-Infinity V</i>										
	<i>Min</i>	<i>900.4 m</i>	<i>27.12 %</i>	<i>Infinity V</i>										
	<i>Max</i>	<i>913.8 m</i>	<i>29.10 %</i>	<i>-Infinity V</i>										
	<i>Sum</i>	<i>1.814</i>	<i>56.21 %</i>	<i>0.000 V</i>										
✓	Trial 1	914 m	29.1% (no value)		621.816 mV	604.781 mV	568.237 mV	604.781 mV	568.237 mV	2.7 Gbps	Swing 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 2 (Worst)	900 m	27.1% (no value)		609.977 mV	583.037 mV	549.198 mV	583.037 mV	549.198 mV	1.62 Gbps	Swing 1	Pre-emphasis 2	SSC Disabled	Level 0

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✓ Lane 3 - Non-Transition Voltage Range Measurement (Swing 1) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 708 m Non-Transition Voltage Range (Worst of 2 Trials) 1.222 # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 3) (V)	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	1.224	72.95 %	NaN V										
	StdDev	3.296 m	499.4 m%	NaN V										
	Range	4.661 m	706.2 m%	-Infinity V										
	Min	1.222	72.60 %	Infinity V										
	Max	1.227	73.31 %	-Infinity V										
	Sum	2.448	145.9 %	0.000 V										
✓	Trial 1 (Worst)	1.222	72.6%	(no value)	600.309 mV	733.522 mV	844.177 mV	844.177 mV	733.522 mV	2.7 Gbps	Swing 1 2	Pre-emphasis 2	SSC Disabled	Level 0
✓	Trial 2	1.227	73.3%	(no value)	596.950 mV	732.199 mV	844.786 mV	844.786 mV	732.199 mV	1.62 Gbps	Swing 1 2	Pre-emphasis 2	SSC Disabled	Level 0

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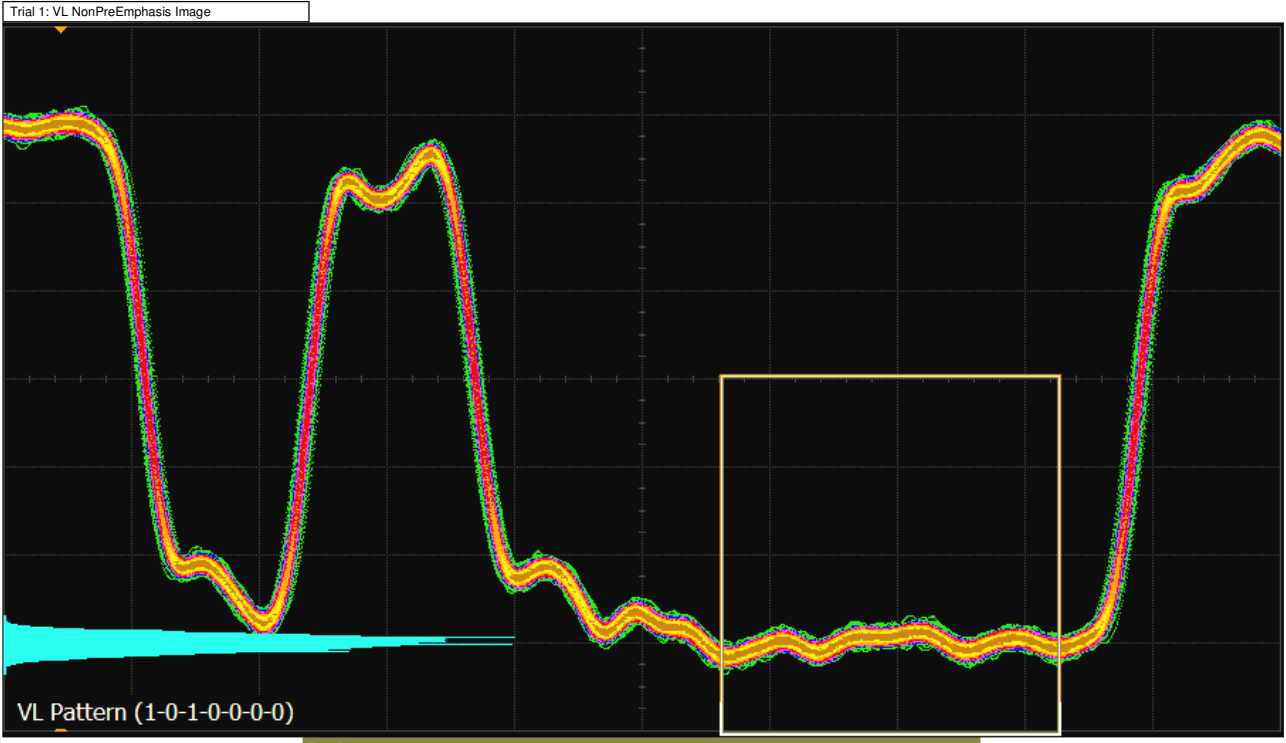
**X Lane 0 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
 Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2) (Worst of 2 Trials) -235 mdB** | **# Trials Run: 2** | **Worst Trial: Trial 2**

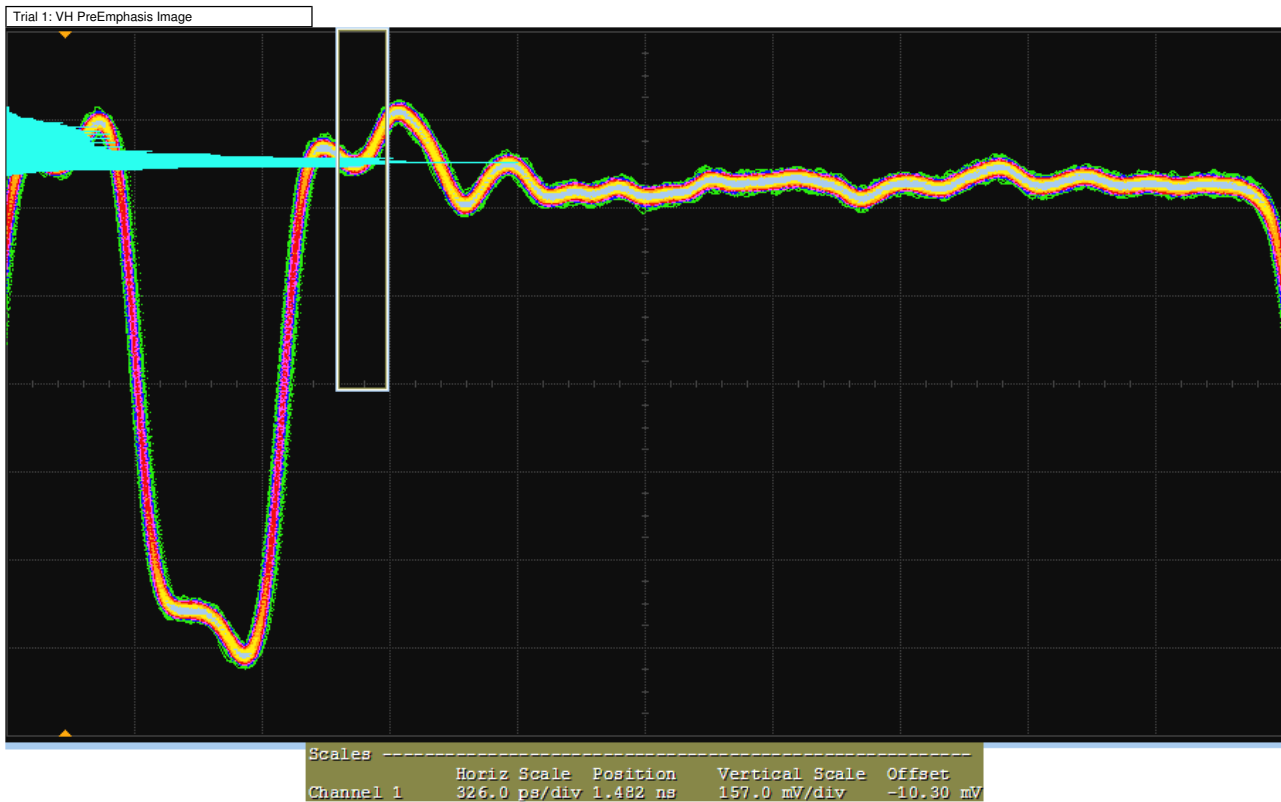
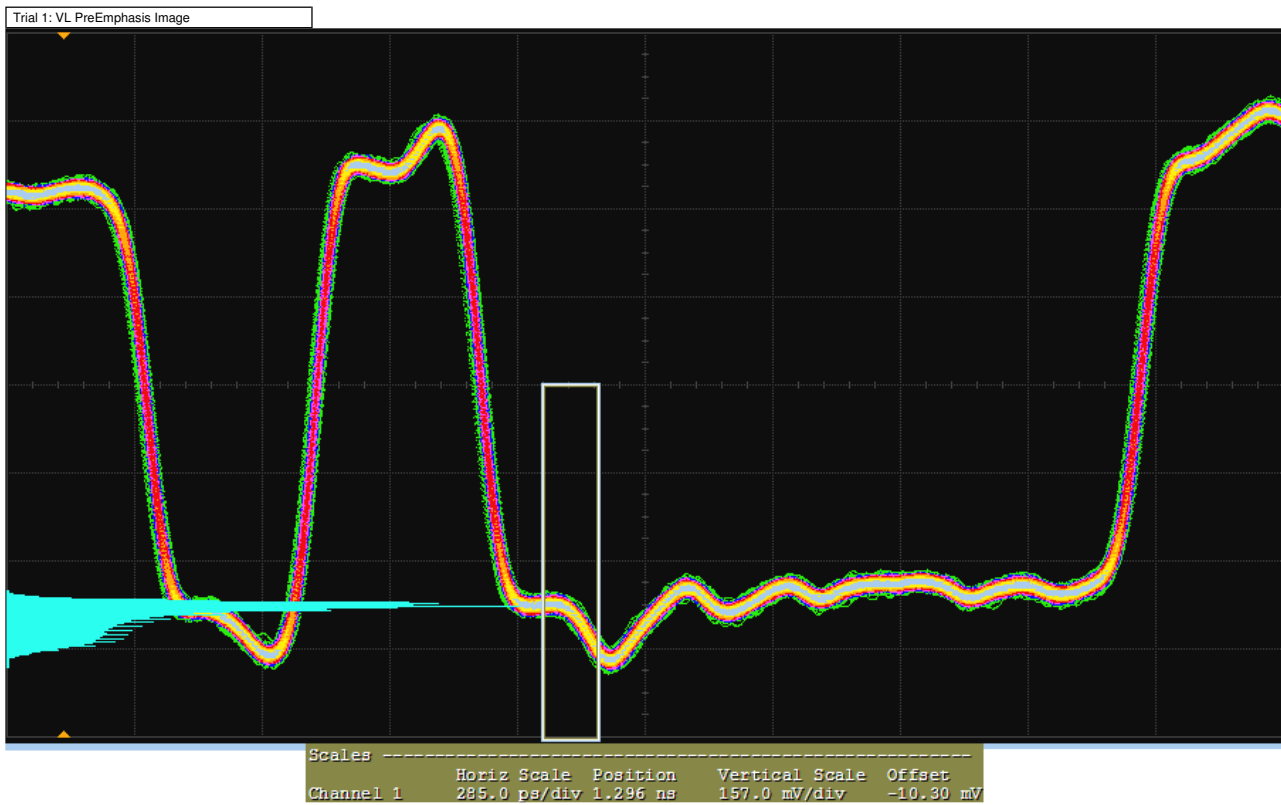
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-154.3 mdB	-109.7 %													
	StdDev	114.0 mdB	7.115 %													
	Range	161.2 mdB	10.06 %													
	Min	-234.9 mdB	-114.7 %													
	Max	-73.71 mdB	-104.6 %													
	Sum	-308.6 mdB	-219.3 %													
<b>X</b>	Trial 1	-74 mdB	-	(See image)	(See image)	(See image)	(See image)	1000	840.505 mV	739.274 mV	1.115 dB	2.7 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0
<b>X</b>	Trial 2 (Worst)	-235 mdB	-	(See image)	(See image)	(See image)	(See image)	1000	961.052 mV	723.691 mV	2.464 dB	1.62 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0

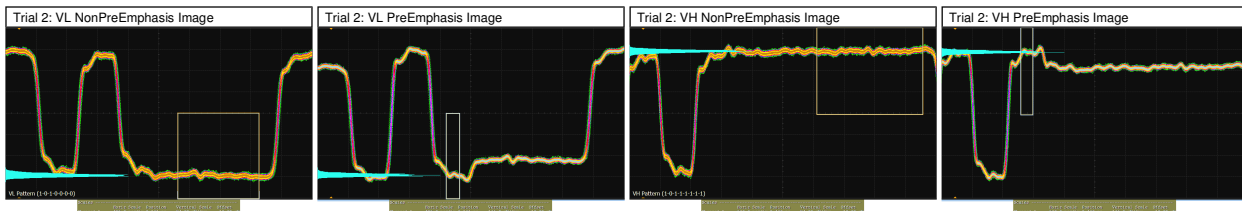
Trial 1



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	285.0 ps/div	1.296 ns	73.50 mV/div	-9.300 mV



Trial 2



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**✘ Lane 1 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

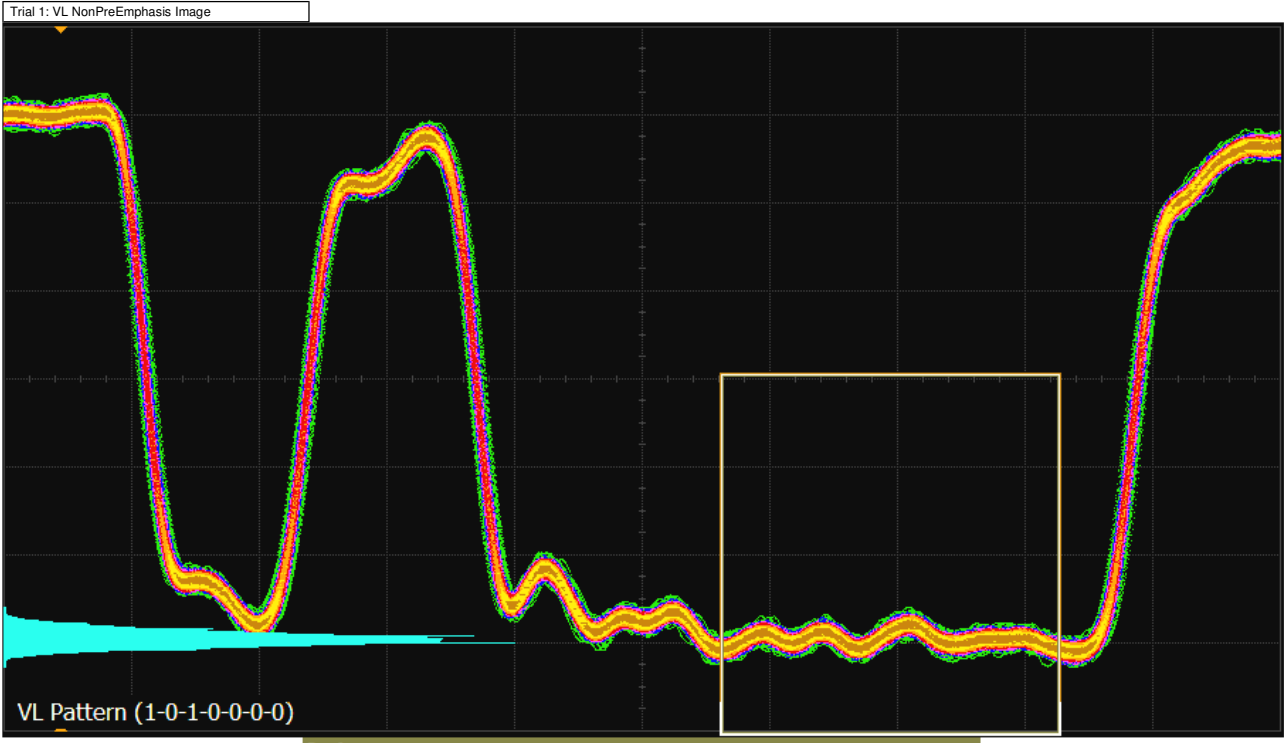
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2) (Worst of 2 Trials) -3.200 dB** | **# Trials Run: 2** | **Worst Trial: Trial 2**

Overall Summary + details of 2 worst trials

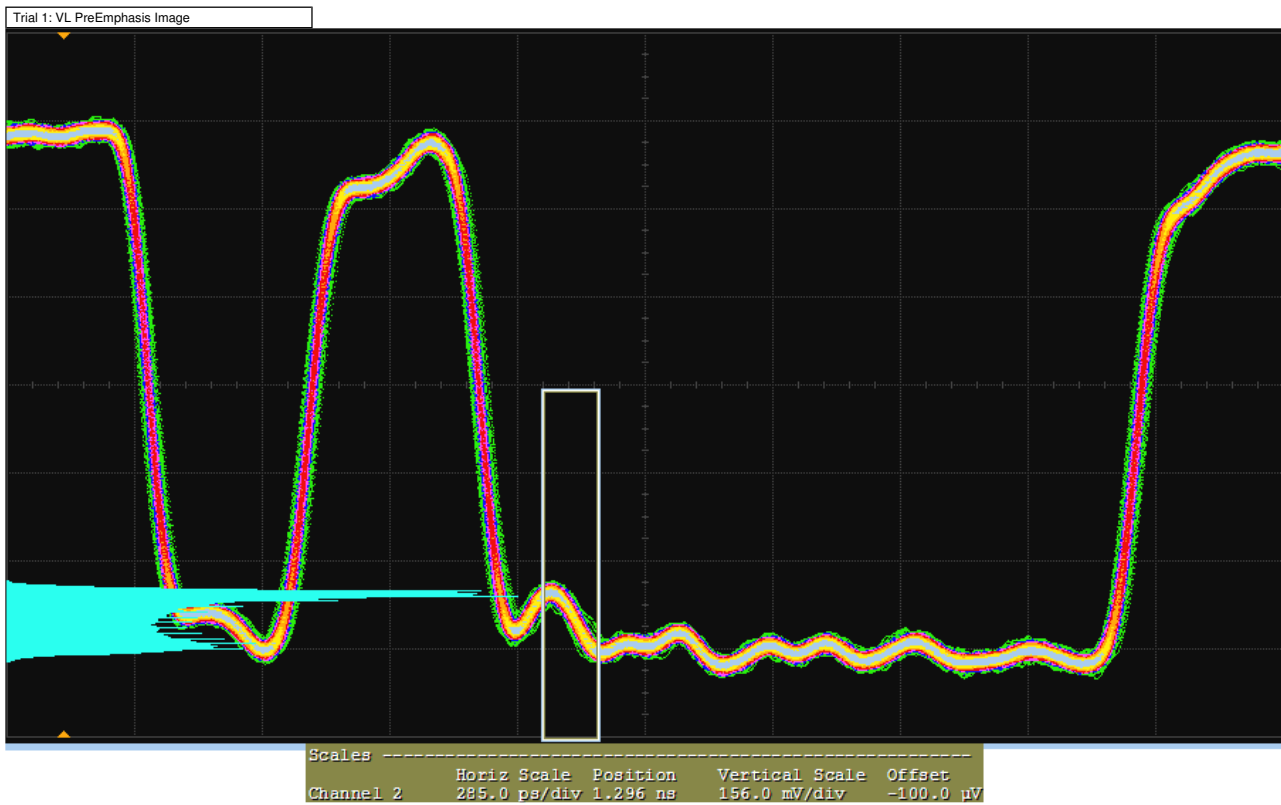
Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-3.099 dB	-293.7 %													
	StdDev	142.7 mdB	8.927 %													
	Range	201.9 mdB	12.63 %													
	Min	-3.200 dB	-300.0 %													
	Max	-2.998 dB	-287.4 %													
	Sum	-6.197 dB	-587.4 %													
✘	Trial 1	-2.998 dB	-	(See image)	(See image)	(See image)	(See image)	1000	786.676 mV	920.058 mV	-1.360 dB	2.7 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0
✘	Trial 2 (Worst)	-3.200 dB	-300.0%	(See image)	(See image)	(See image)	(See image)	1000	852.466 mV	910.964 mV	-576 mdB	1.62 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0

Trial 1

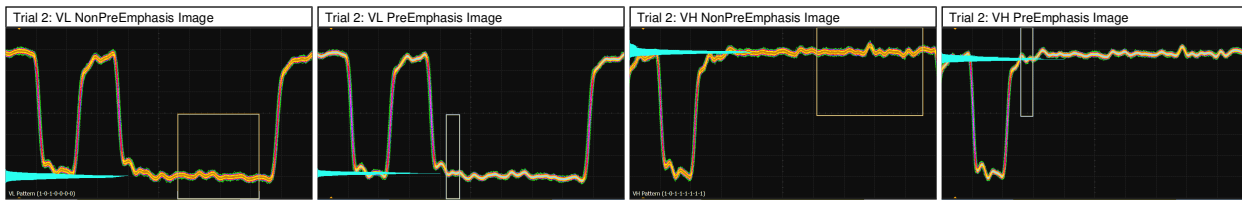


Channel 2	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	285.0 ps/div	1.296 ns	73.50 mV/div	-8.300 mV





Trial 2



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**✘ Lane 2 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)** Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

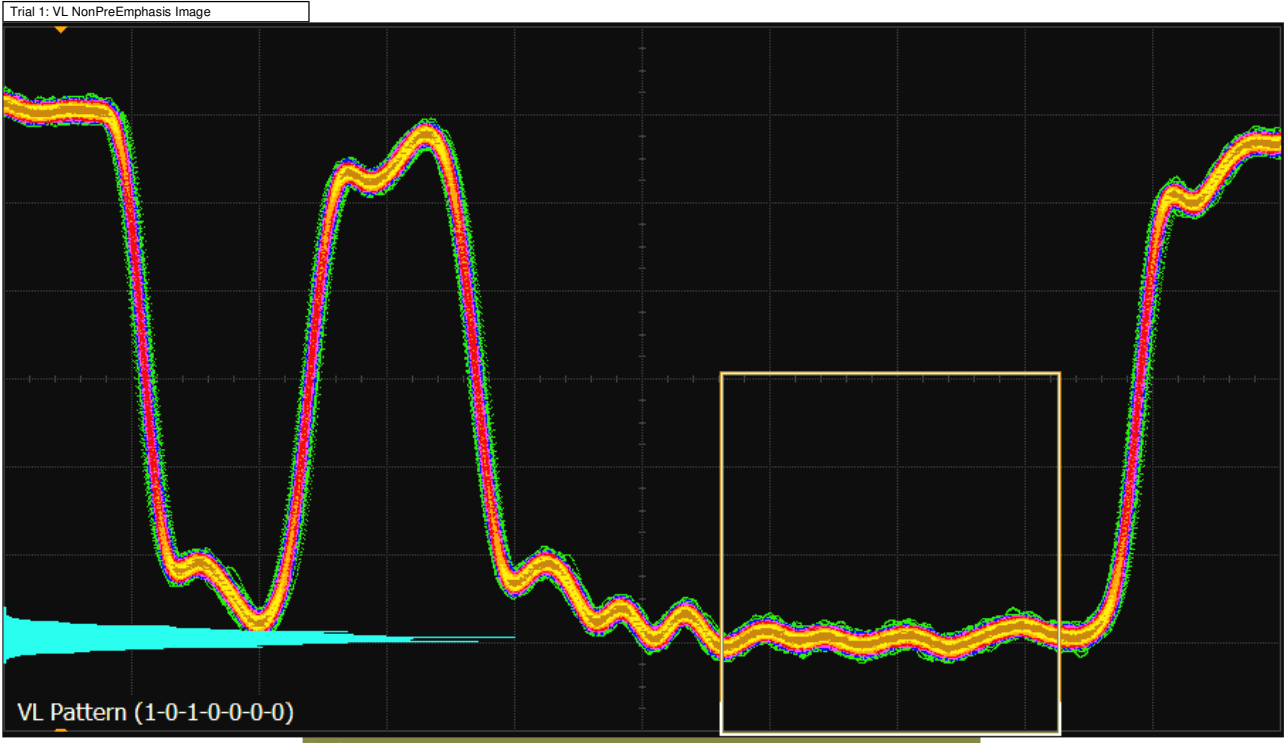
Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: **>= 1.600 dB** | **PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2) (Worst of 2 Trials) -5.641 dB** | **# Trials Run: 2** | **Worst Trial: Trial 2**

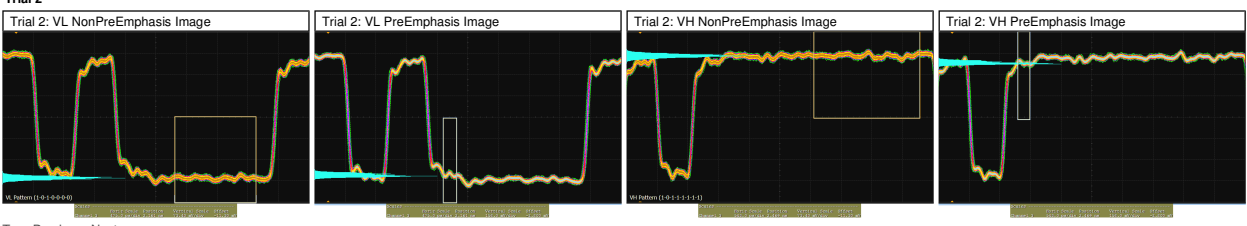
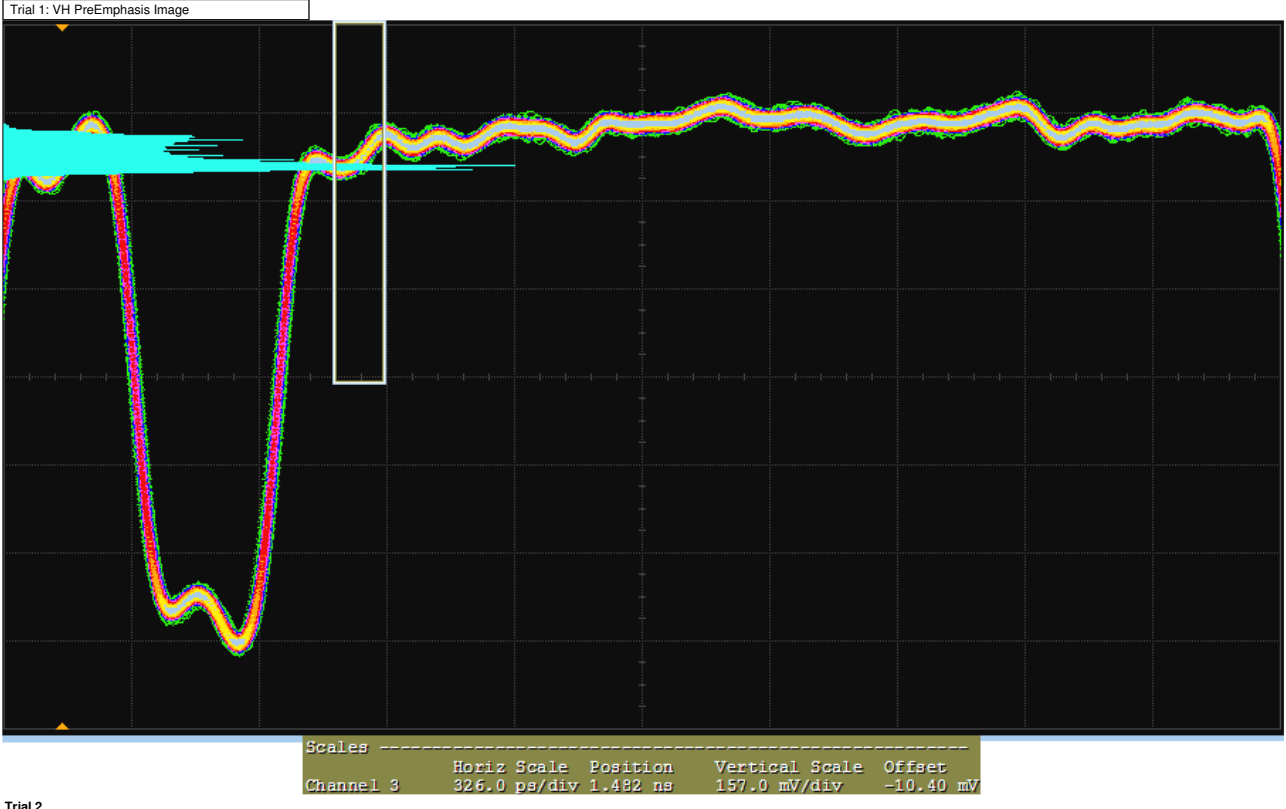
Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	-5.553 dB	-447.1 %													
	StdDev	124.5 mdB	7.778 %													
	Range	176.1 mdB	11.00 %													
	Min	-5.641 dB	-452.6 %													
	Max	-5.465 dB	-441.6 %													
	Sum	-11.11 dB	-894.1 %													
✘	Trial 1	-5.465 dB	-	(See image)	(See image)	(See image)	(See image)	1000	777.883 mV	922.273 mV	-1.479 dB	2.7 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0
✘	Trial 2 (Worst)	-5.641 dB	-	(See image)	(See image)	(See image)	(See image)	1000	830.194 mV	902.707 mV	-727 mdB	1.62 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0

Trial 1



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
3	285.0 ps/div	1.296 ns	74.80 mV/div	-9.300 mV	



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✓ Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
**Pass Limits:** >= 1.600 dB | **PreEmphasis(Pre-emphasis 3) - PreEmphasis(Pre-emphasis 2) (Worst of 2 Trials)** 3.149 dB | **# Trials Run:** 2 | **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VL NonPreEmphasis Image	VL PreEmphasis Image	VH NonPreEmphasis Image	VH PreEmphasis Image	Number of UI	VSwing PreEmphasis (Transition Bit)	VSwing PreEmphasis (Non Transition Bit)	PreEmphasis Result	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	3.179 dB	98.69 %													
	StdDev	42.59 mdB	2.652 %													
	Range	60.23 mdB	3.750 %													
	Min	3.149 dB	96.81 %													
	Max	3.209 dB	100.6 %													
	Sum	6.358 dB	197.4 %													
✓	Trial 1 (Worst)	3.149 dB	96.8%	(See image)	(See image)	(See image)	(See image)	1000	899.839 mV	735.382 mV	1.753 dB	2.7 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0
✓	Trial 2	3.209 dB	100.6%	(See image)	(See image)	(See image)	(See image)	1000	952.414 mV	735.085 mV	2.250 dB	1.62 Gbps	0	3	Swing Pre-emphasis Disabled	Level 0

Trial 1



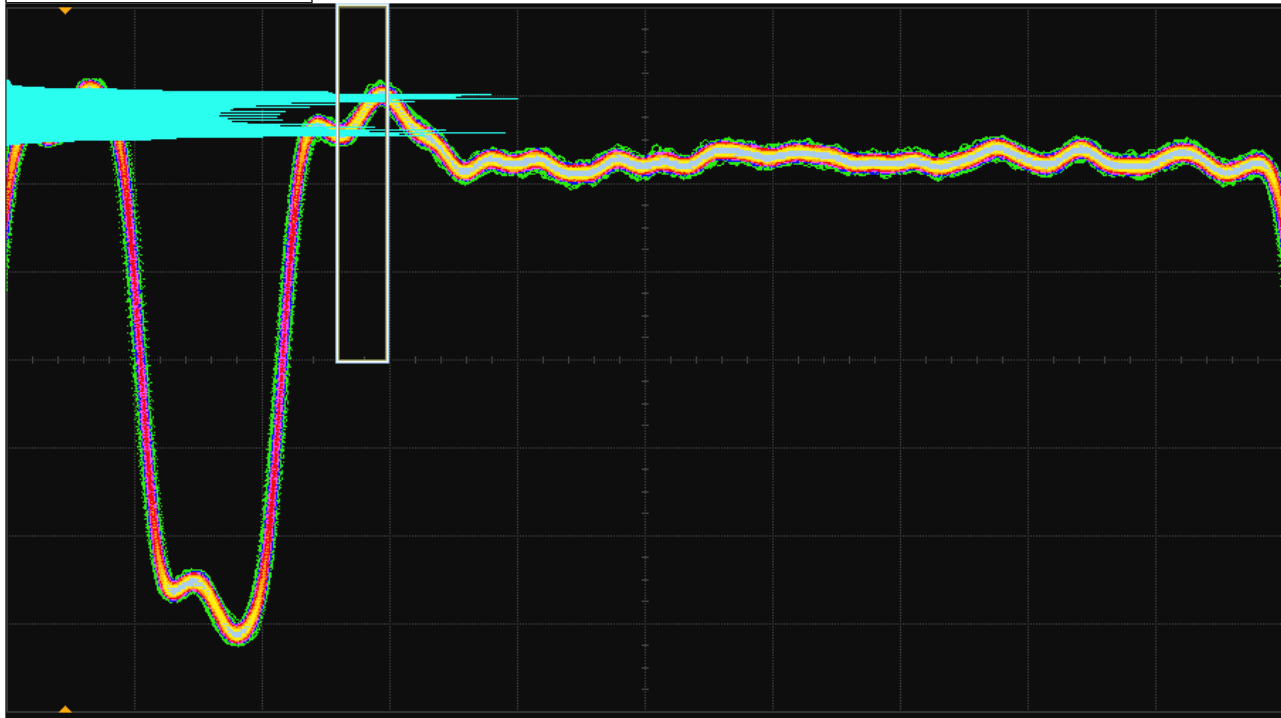
Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	285.0 ps/div	1.296 ns	72.40 mV/div	-14.00 mV

Trial 1: VL PreEmphasis Image



Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	285.0 ps/div	1.296 ns	157.0 mV/div	-14.20 mV

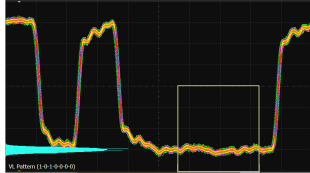
Trial 1: VH PreEmphasis Image



Channel 4	Horiz Scale	Position	Vertical Scale	Offset
	326.0 ps/div	1.481 ns	157.0 mV/div	-14.20 mV

Trial 2

Trial 2: VL NonPreEmphasis Image



Trial 2: VL PreEmphasis Image



Trial 2: VH NonPreEmphasis Image



Trial 2: VH PreEmphasis Image



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**X** Lane 0 - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **FAIL** Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.  
**Pass Limits:** >= 850 mV | **Non-Transition Voltage Range (Worst of 2 Trials)** 814 mV | **# Trials Run:** 2 | **Worst Trial:** Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit(Pre-emphasis 3)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	<i>Avg</i>	816.0 m	-4.000 %											
	<i>StdDev</i>	3.232 m	332.8 m%											
	<i>Range</i>	4.571 m	470.6 m%											
	<i>Min</i>	813.7 m	-4.235 %											
	<i>Max</i>	818.3 m	-3.765 %											
	<i>Sum</i>	1.632	-8.000 %											
<b>X</b>	Trial 1	818 m	-3.8%	429.059 mV	351.082 mV	491.273 mV	739.274 mV	739.274 mV	351.082 mV	2.7 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0
<b>X</b>	Trial 2 (Worst)	814 m	-4.2%	422.883 mV	344.096 mV	483.965 mV	723.691 mV	723.691 mV	344.096 mV	1.62 Gbps	Swing 0	Pre-emphasis 3	SSC Disabled	Level 0

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✓ Lane 1 - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 850 m **Non-Transition Voltage Range (Worst of 2 Trials)** 1.140 # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit(Pre-emphasis 3)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	1.142	34.35 %											
	StdDev	2.846 m	332.8 m%											
	Range	4.025 m	470.6 m%											
	Min	1.140	34.12 %											
	Max	1.144	34.59 %											
	Sum	2.284	68.71 %											
✓	Trial 1 (Worst)	1.140	34.1%	430.084 mV	519.236 mV	490.382 mV	920.058 mV	920.058 mV	490.382 mV	2.7 Gbps	0 3	Swing Pre-emphasis	SSC Disabled	Level 0
✓	Trial 2	1.144	34.6%	425.355 mV	515.472 mV	486.701 mV	910.964 mV	910.964 mV	486.701 mV	1.62 Gbps	0 3	Swing Pre-emphasis	SSC Disabled	Level 0

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✓ Lane 2 - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 850 m | Non-Transition Voltage Range (Worst of 2 Trials) 945 m | # Trials Run: 2 | Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit (Pre-emphasis 0)	VSwing Non-Transition Bit (Pre-emphasis 1)	VSwing Non-Transition Bit (Pre-emphasis 2)	VSwing Non-Transition Bit (Pre-emphasis 3)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	951.6 m	11.94 %											
	StdDev	9.555 m	1.081 %											
	Range	13.51 m	1.529 %											
	Min	944.8 m	11.18 %											
	Max	958.3 m	12.71 %											
	Sum	1.903	23.88 %											
✓	Trial 1 (Worst)	945 m	11.2%	442.925 mV	429.295 mV	418.478 mV	922.273 mV	922.273 mV	418.478 mV	2.7 Gbps	0 3	Pre-emphasis	SSC Disabled	Level 0
✓	Trial 2	958 m	12.7%	423.088 mV	416.393 mV	405.453 mV	902.707 mV	902.707 mV	405.453 mV	1.62 Gbps	0 3	Pre-emphasis	SSC Disabled	Level 0

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✓ Lane 3 - Non-Transition Voltage Range Measurement (Swing 0) Reference: DisplayPort CTS Sec. 3.3; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Pass Limits: >= 850 m | **Non-Transition Voltage Range (Worst of 2 Trials)** 1.231 | # Trials Run: 2 | Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	VSwing Non-Transition Bit(Pre-emphasis 0)	VSwing Non-Transition Bit(Pre-emphasis 1)	VSwing Non-Transition Bit(Pre-emphasis 2)	VSwing Non-Transition Bit(Pre-emphasis 3)	VSwing Non-Transition Bit (Max)	VSwing Non-Transition Bit (Min)	BitRate	Level	PreEmphasis	SSC	PostCursor2
	Avg	1.233	45.06 %											
	StdDev	2.956 m	332.8 m%											
	Range	4.180 m	470.6 m%											
	Min	1.231	44.82 %											
	Max	1.235	45.29 %											
	Sum	2.465	90.12 %											
✓	Trial 1 (Worst)	1.231	44.8%	417.935 mV	514.278 mV	597.463 mV	735.382 mV	735.382 mV	514.278 mV	2.7 Gbps	0	3	Pre-emphasis Disabled	SSC Level 0
✓	Trial 2	1.235	45.3%	415.061 mV	512.476 mV	595.386 mV	735.085 mV	735.085 mV	512.476 mV	1.62 Gbps	0	3	Pre-emphasis Disabled	SSC Level 0

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✓ Lane 0 - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [800.0 mdB to 6.0000 dB] **Lane 0 Non-PreEmphasis Level Test (Swing 3/Swing 2) (Worst of 2 Trials)** 1.8316 dB **# Trials Run:** 2 **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

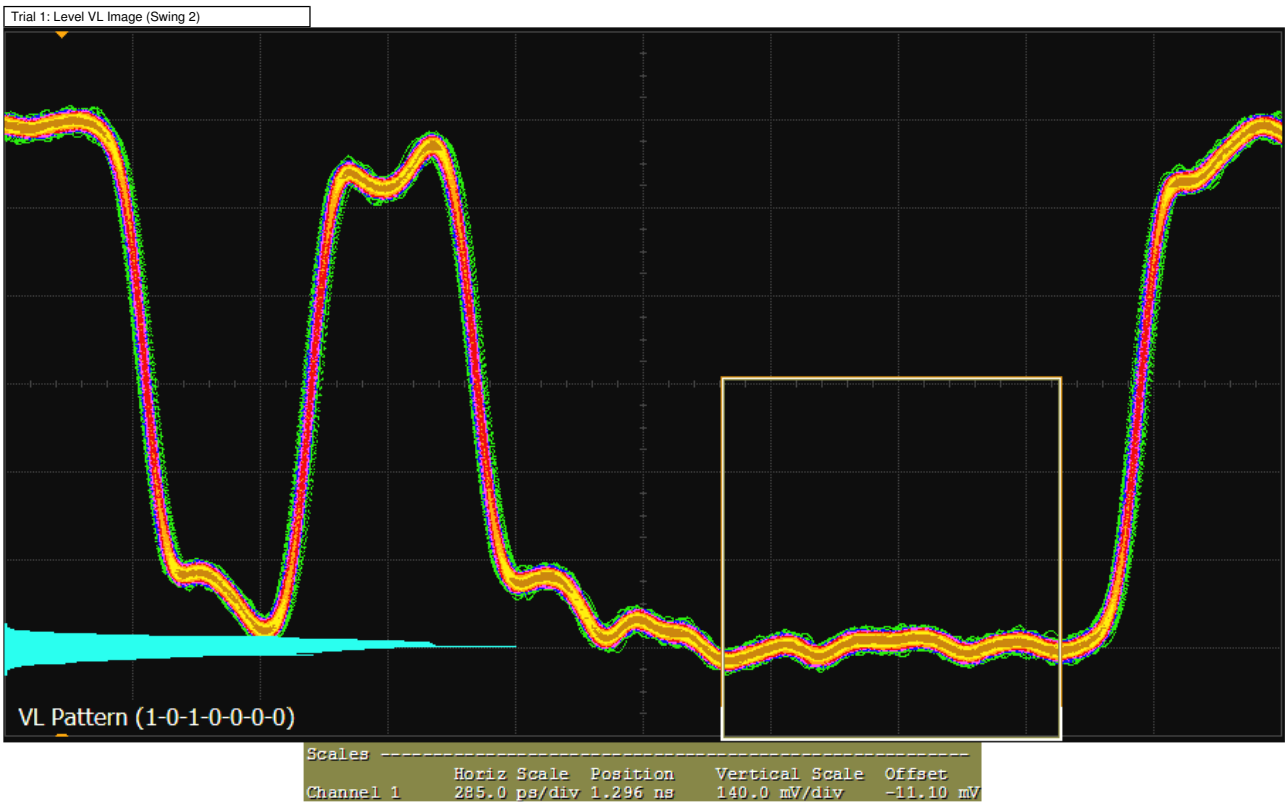
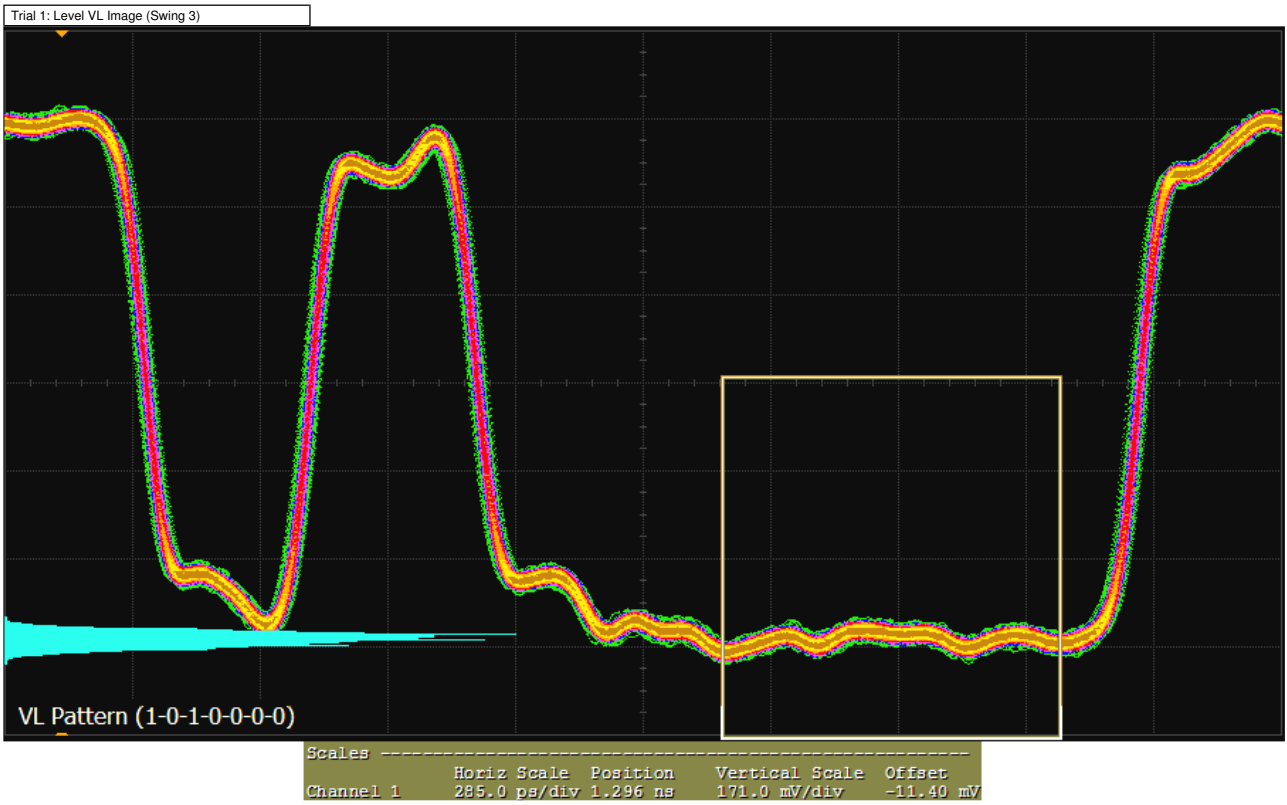
Pass	Actual Value	Margin	Level VH Image (Swing 3)	Level VL Image (Swing 2)	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 3)	VBase (Swing 3)	VSwing (Swing 3)	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	Bit
<b>Avg</b>	1.836 dB	19.92 %																				
<b>StdDev</b>	6.005 mdB	115.6 m%																				
<b>Range</b>	8.492 mdB	163.5 m%																				
<b>Min</b>	1.832 dB	19.84 %																				
<b>Max</b>	1.840 dB	20.00 %																				
<b>Sum</b>	3.672 dB	39.84 %																				
✓ Trial 1 (Worst)	1.8316 dB	19.8%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	491.530 mV	520.786 mV	1.012316 V	397.440 mV	422.410 mV	819.850 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gb/s
✓ Trial 2	1.8401 dB	20.0%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	491.759 mV	514.567 mV	1.006326 V	396.092 mV	418.110 mV	814.202 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.6 Gb/s

Trial 1

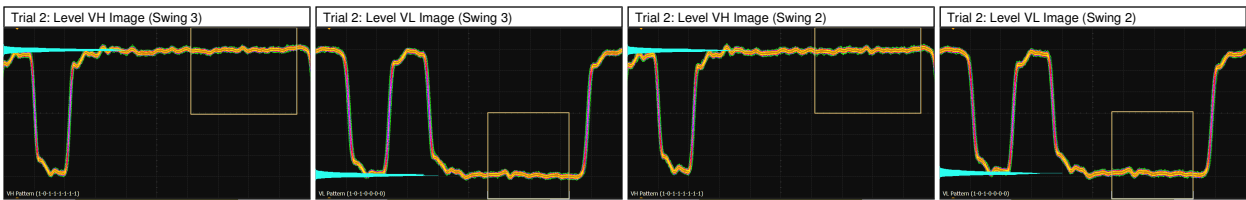
Trial 1: Level VH Image (Swing 3)



Channel 1	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	326.0 ps/div	1.482 ns	171.0 mV/div	-11.40 mV



Trial 2



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✓ Lane 1 - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

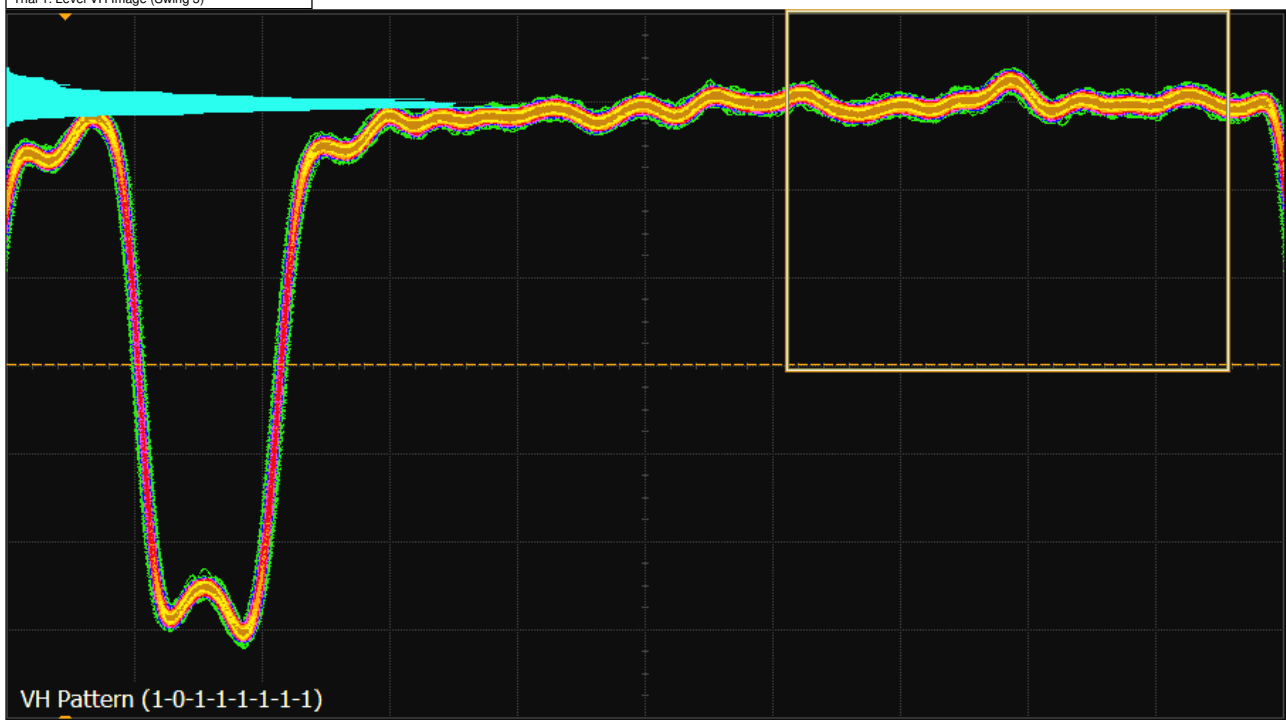
Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [800.0 mdB to 6.0000 dB] **Lane 1 Non-PreEmphasis Level Test (Swing 3/Swing 2) (Worst of 2 Trials)** 1.8212 dB **# Trials Run:** 2 **Worst Trial:** Trial 1

Overall Summary + details of 2 worst trials

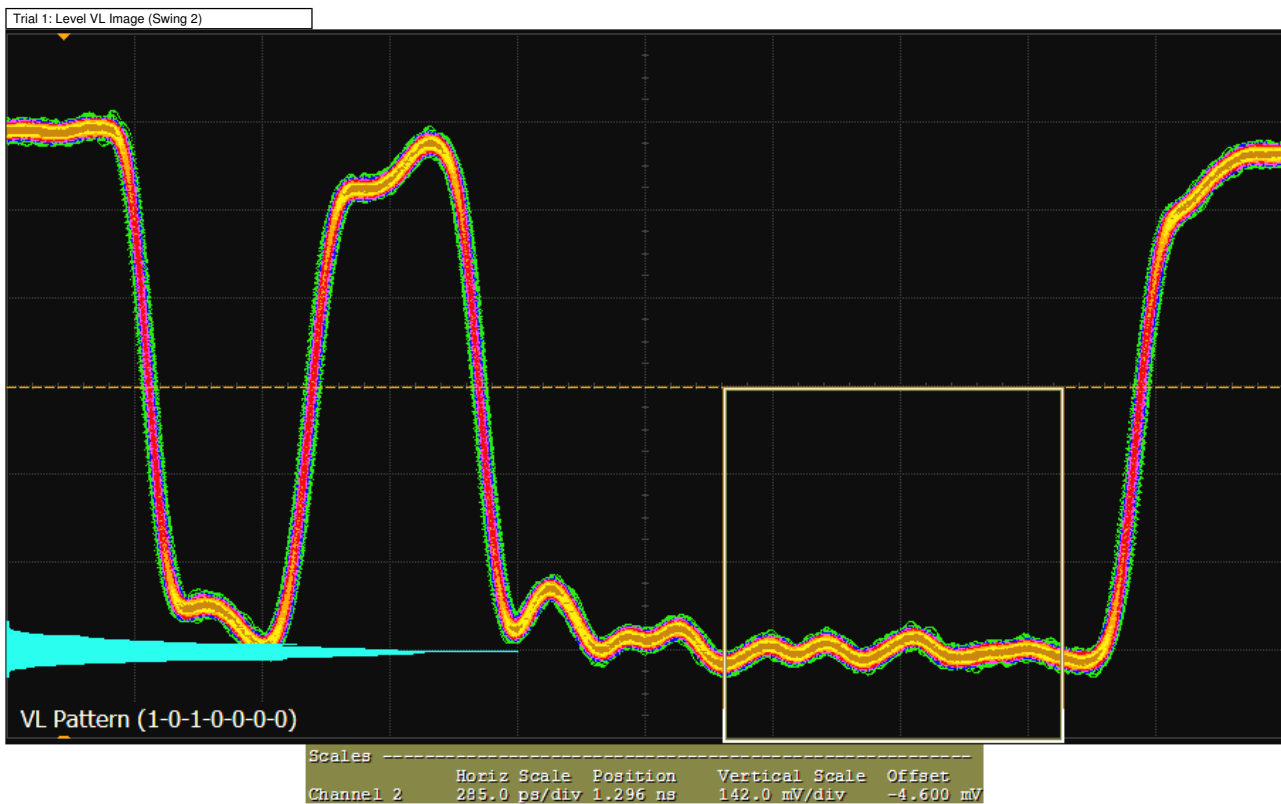
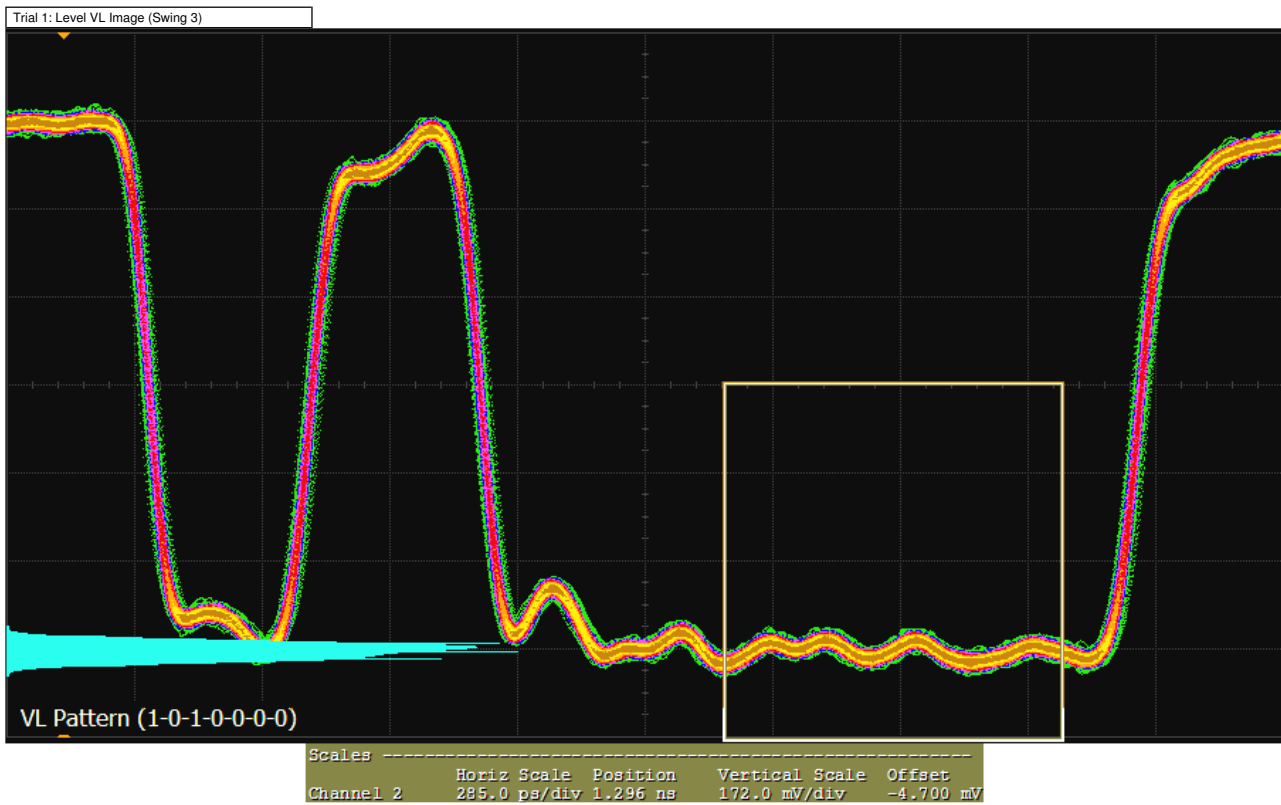
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 3)	Level VL Image (Swing 2)	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 3)	VBase (Swing 3)	VSwing (Swing 3)	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	Bit
	Avg	1.832 dB	19.85 %																				
	StdDev	15.71 mdB	301.9 m%																				
	Range	22.22 mdB	426.9 m%																				
	Min	1.821 dB	19.64 %																				
	Max	1.843 dB	20.07 %																				
	Sum	3.665 dB	39.70 %																				
✓	Trial 1 (Worst)	1.8212 dB	19.6%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	496.328 mV	514.672 mV	1.010999 V	401.220 mV	418.548 mV	819.768 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gb/s
✓	Trial 2	1.8434 dB	20.1%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	494.402 mV	512.761 mV	1.007163 V	398.058 mV	416.513 mV	814.571 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.6 Gb/s

Trial 1

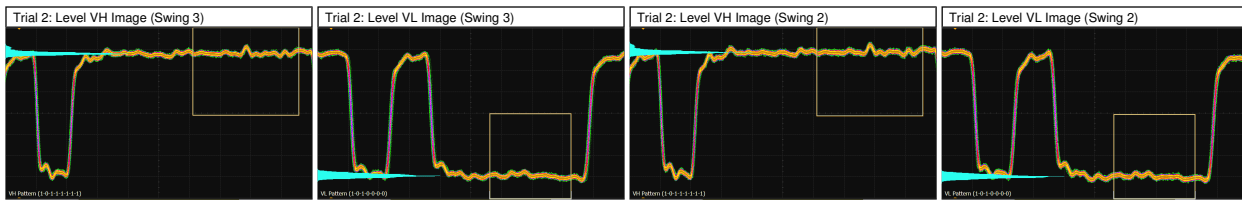
Trial 1: Level VH Image (Swing 3)



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 2		326.0 ps/div	1.481 ns	172.0 mV/div	-4.700 mV



Trial 2



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✓ Lane 2 - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
 Pass Limits: [800.0 mdB to 6.0000 dB] Lane 2 Non-PreEmphasis Level Test (Swing 3/Swing 2) (Worst of 2 Trials) 1.6330 dB # Trials Run: 2 Worst Trial: Trial 1

Overall Summary + details of 2 worst trials

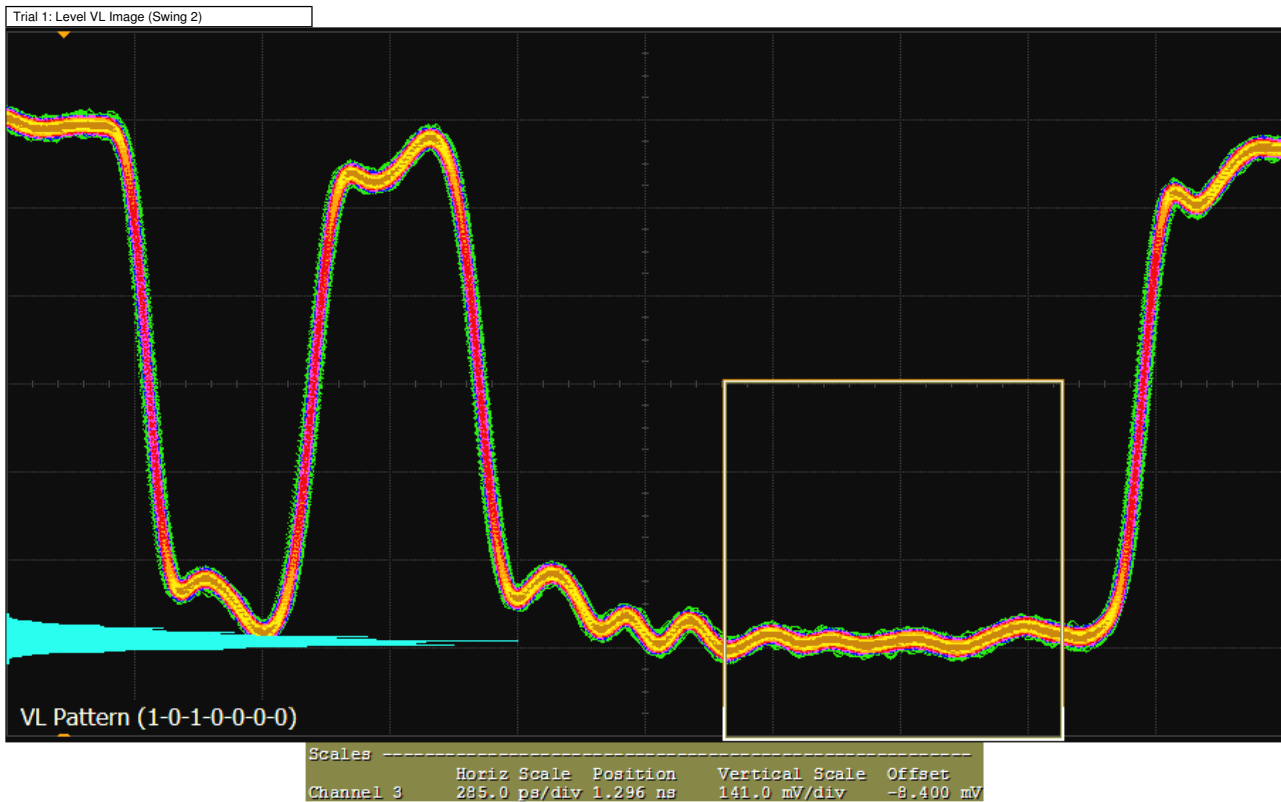
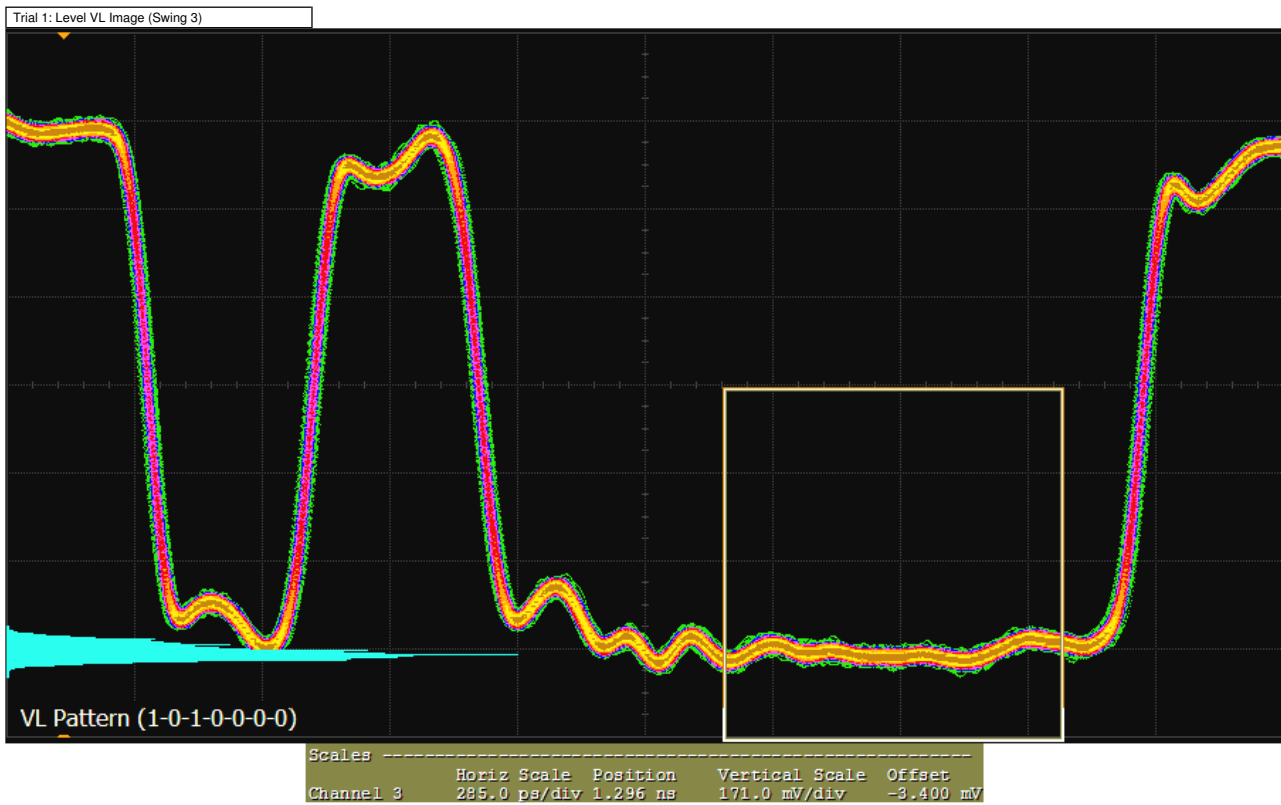
Pass	Trial	Actual Value	Margin	Level VH Image (Swing 3)	Level VL Image (Swing 2)	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 3)	VBase (Swing 3)	VSwing (Swing 3)	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	Bit
	Avg	1.688 dB	17.07 %																				
	StdDev	77.48 mdB	1.489 %																				
	Range	109.6 mdB	2.106 %																				
	Min	1.633 dB	16.02 %																				
	Max	1.743 dB	18.13 %																				
	Sum	3.375 dB	34.14 %																				
✓	Trial 1 (Worst)	1.6330 dB	16.0%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	484.229 mV	516.502 mV	1.000731 V	401.228 mV	427.992 mV	829.219 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gb/s
✓	Trial 2	1.7425 dB	18.1%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	488.305 mV	507.674 mV	995.978 mV	398.274 mV	416.661 mV	814.935 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.6 Gb/s

Trial 1

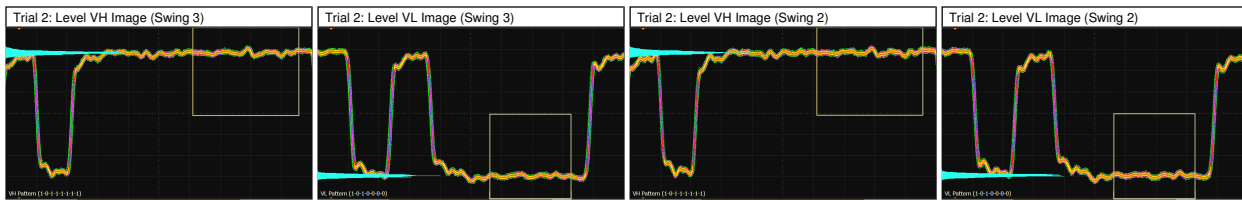
Trial 1: Level VH Image (Swing 3)



Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	326.0 ps/div	1.482 ns		171.0 mV/div	-3.400 mV



Trial 2



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✓ Lane 3 - Non-PreEmphasis Level Test (Swing 3/ Swing 2) Reference: DisplayPort CTS Sec. 3.2; Table 3.10 VESA DisplayPort Standard specification

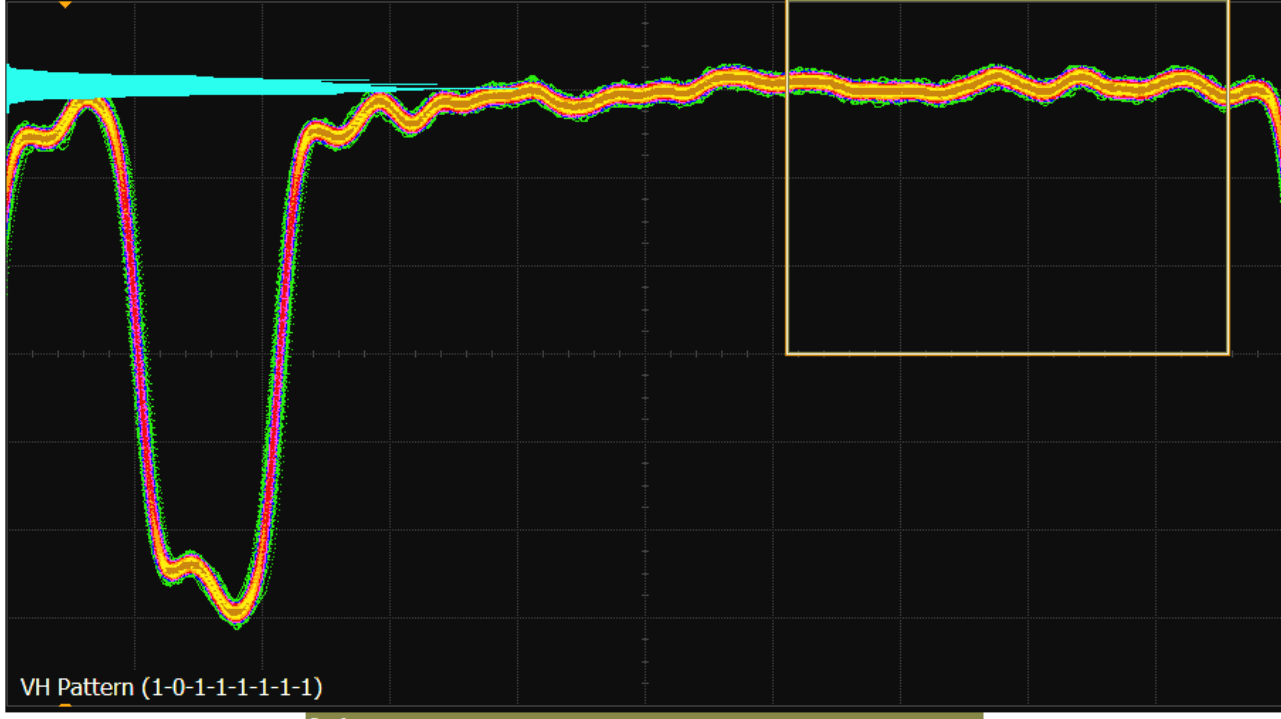
Test Summary: **Pass** Test Description: To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.  
**Pass Limits:** [800.0 mdB to 6.0000 dB] **Lane 3 Non-PreEmphasis Level Test (Swing 3/Swing 2) (Worst of 2 Trials)** 1.8759 dB **# Trials Run:** 2 **Worst Trial:** Trial 2

Overall Summary + details of 2 worst trials

Pass	Trial	Actual Value	Margin	Level VH Image (Swing 3)	Level VL Image (Swing 2)	Level VH Image (Swing 2)	Level VL Image (Swing 2)	Number of UI	VH Trigger Pattern	VL Trigger Pattern	VTop (Swing 3)	VBase (Swing 3)	VSwing (Swing 3)	VTop (Swing 2)	VBase (Swing 2)	VSwing (Swing 2)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	Bit
	Avg	1.903 dB	21.22 %																				
	StdDev	38.77 mdB	745.2 m%																				
	Range	54.83 mdB	1,054 %																				
	Min	1.876 dB	20.69 %																				
	Max	1.931 dB	21.74 %																				
	Sum	3.807 dB	42.43 %																				
✓	Trial 1	1.9307 dB	21.7%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	495.407 mV	522.932 mV	1.018339 V	395.694 mV	419.681 mV	815.375 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	2.7 Gb/s
✓	Trial 2 (Worst)	1.8759 dB	20.7%	(See image)	(See image)	(See image)	(See image)	1000	10111111	1010000	491.964 mV	518.567 mV	1.010531 V	395.436 mV	418.812 mV	814.248 mV	Compliance Tests	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.6 Gb/s

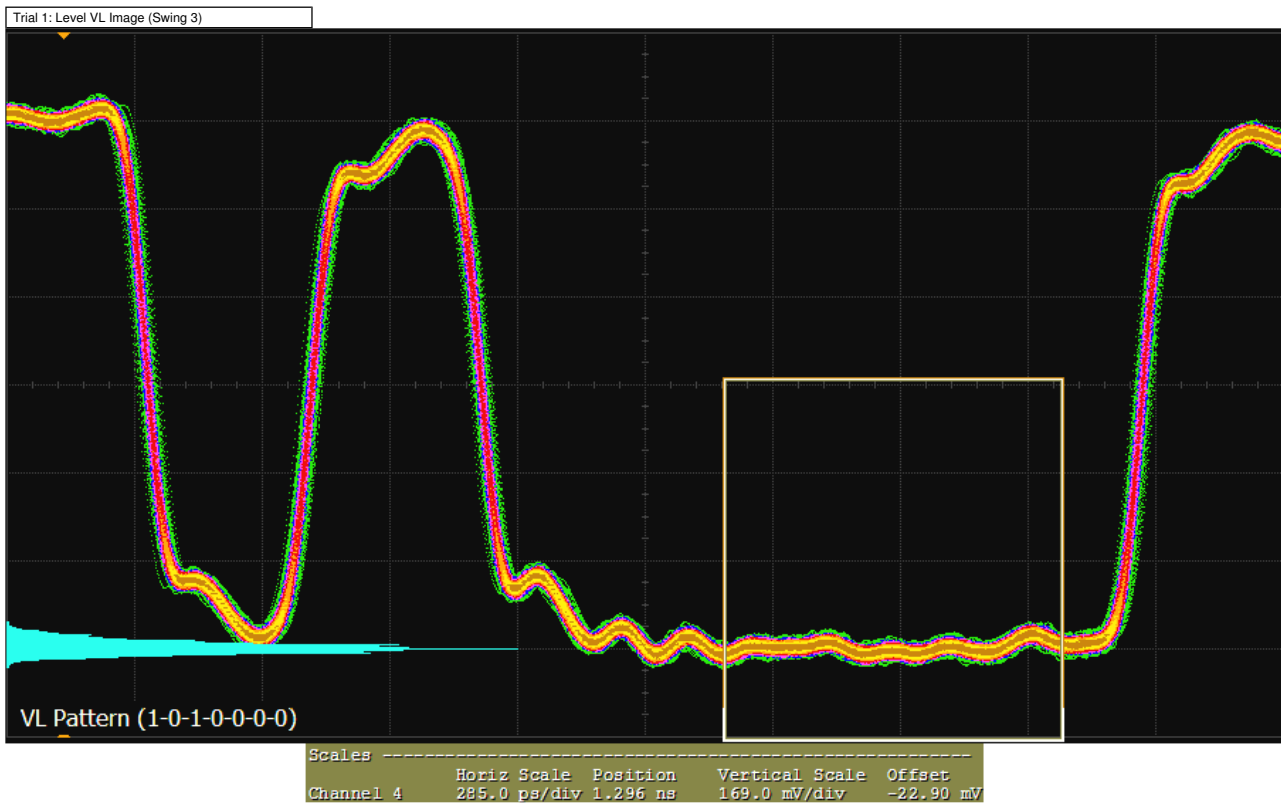
Trial 1

Trial 1: Level VH Image (Swing 3)

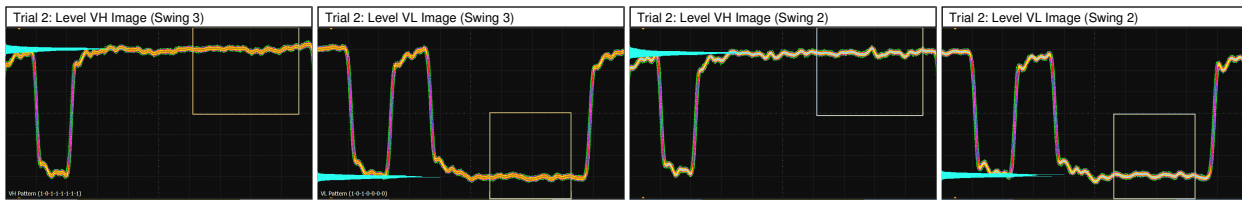


Channel	Scale	Horiz Scale	Position	Vertical Scale	Offset
Channel 4	326.0 ps/div	1.481 ns		169.0 mV/div	-22.90 mV





Trial 2



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✓ Lane 0 - Total Jitter Test (Low BitRate) Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass    Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

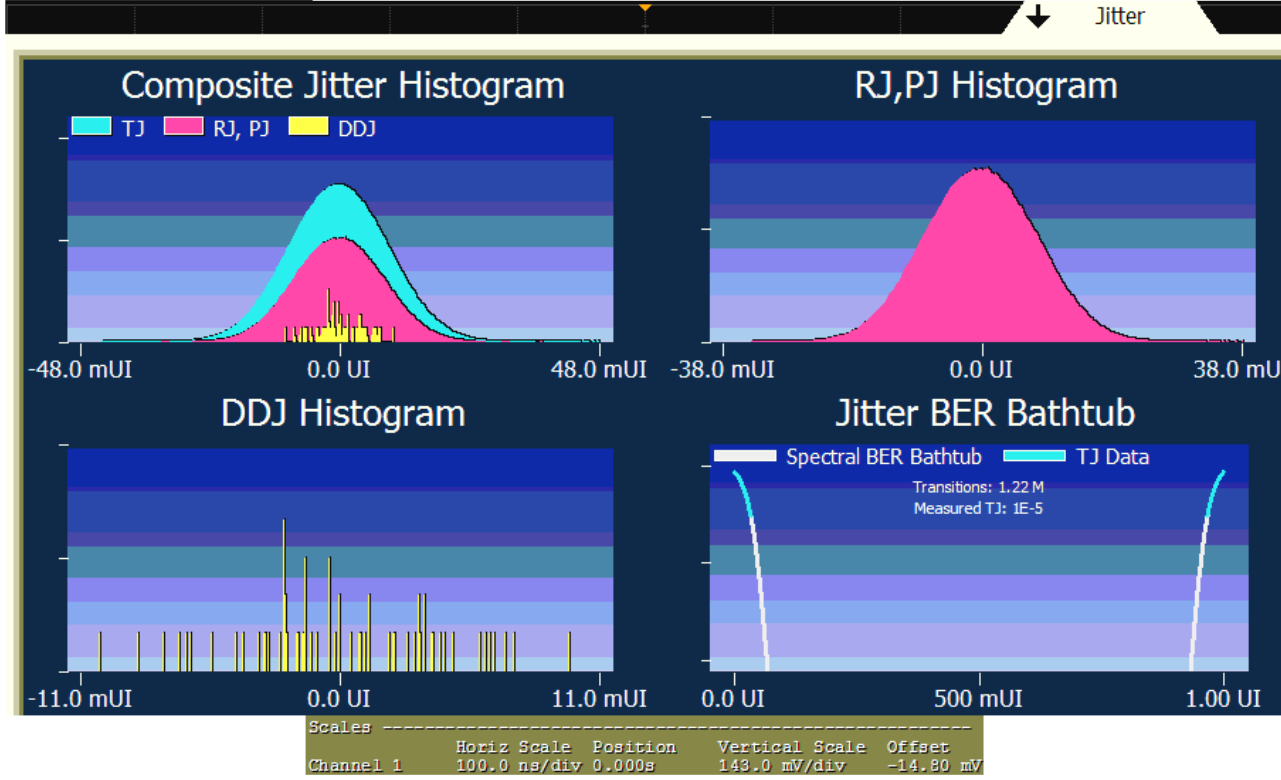
Pass Limits: <= 270.000 mUI    Lane 0 Total Jitter Test (Low BitRate) (Worst of 4 Trials) 99.200 mUI    # Trials Run: 4    Worst Trial: Trial 3

**Overall Summary + details of 4 worst trials**

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Total Jitter (TJ) in mUI	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	<i>Avg</i>	98.45 mUI	63.54 %																			
	<i>StdDev</i>	544.7 μUI	201.7 m%																			
	<i>Range</i>	1,300 mUI	481.5 m%																			
	<i>Min</i>	97.90 mUI	63.26 %																			
	<i>Max</i>	99.20 mUI	63.74 %																			
	<i>Sum</i>	393.8 mUI	254.1 %																			
✓	Trial 1	98.400 mUI	63.6%	(See image)	1.00000000 M	60.7397 ps	98.4 mUI	4.3 mUI	9.7 mUI	18.1 mUI	6.7 mUI	17.6 mUI	20.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 2	98.300 mUI	63.6%	(See image)	1.00000000 M	60.6789 ps	98.3 mUI	4.3 mUI	10.3 mUI	18.0 mUI	6.7 mUI	17.4 mUI	19.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 3 (Worst)	99.200 mUI	63.3%	(See image)	1.00000000 M	61.2345 ps	99.2 mUI	4.2 mUI	9.2 mUI	17.3 mUI	6.8 mUI	19.0 mUI	19.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 4	97.900 mUI	63.7%	(See image)	1.00000000 M	60.4320 ps	97.9 mUI	4.5 mUI	8.8 mUI	18.1 mUI	6.7 mUI	19.6 mUI	19.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	

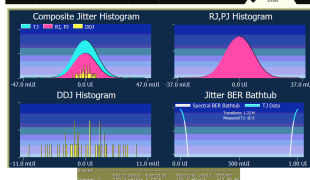
**Trial 1**

Trial 1: Jitter Separation Image



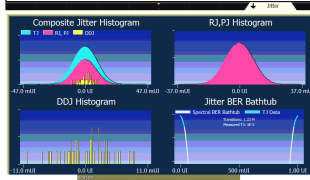
**Trial 2**

Trial 2: Jitter Separation Image



**Trial 3**

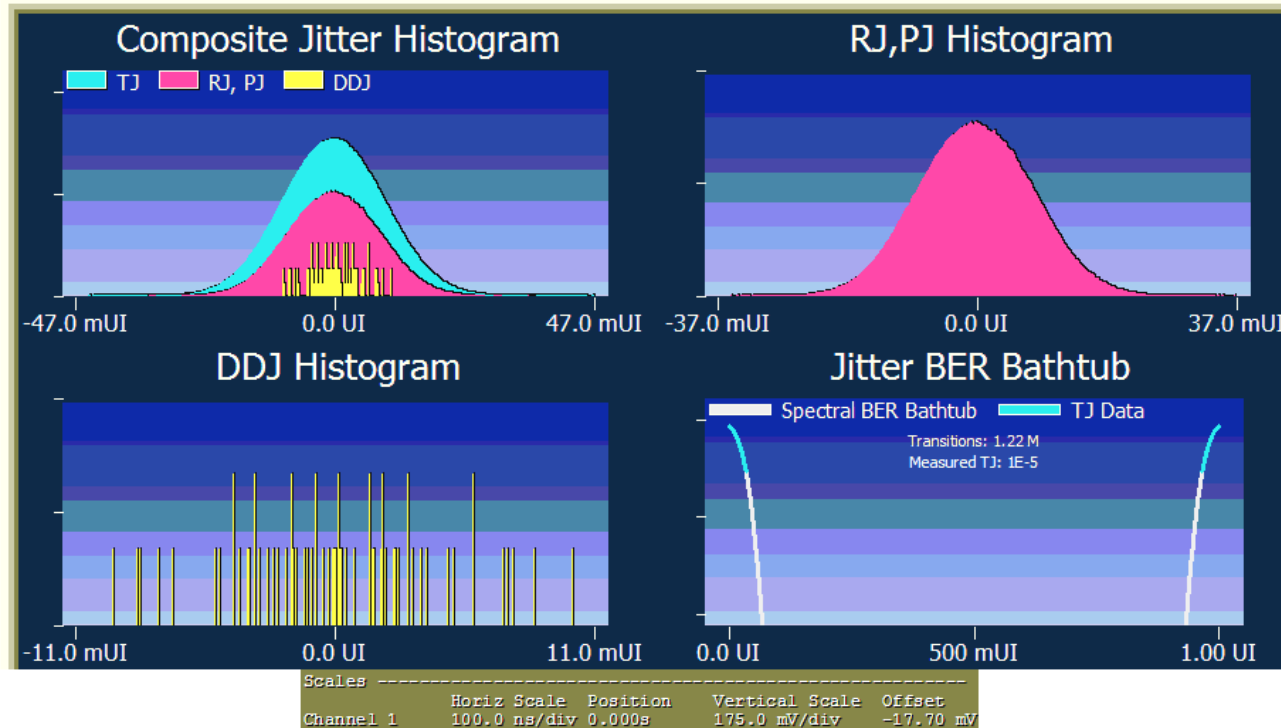
Trial 3: Jitter Separation Image



**Trial 4**

Trial 4: Jitter Separation Image

Jitter



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**✓ Lane 1 - Total Jitter Test (Low BitRate)** Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

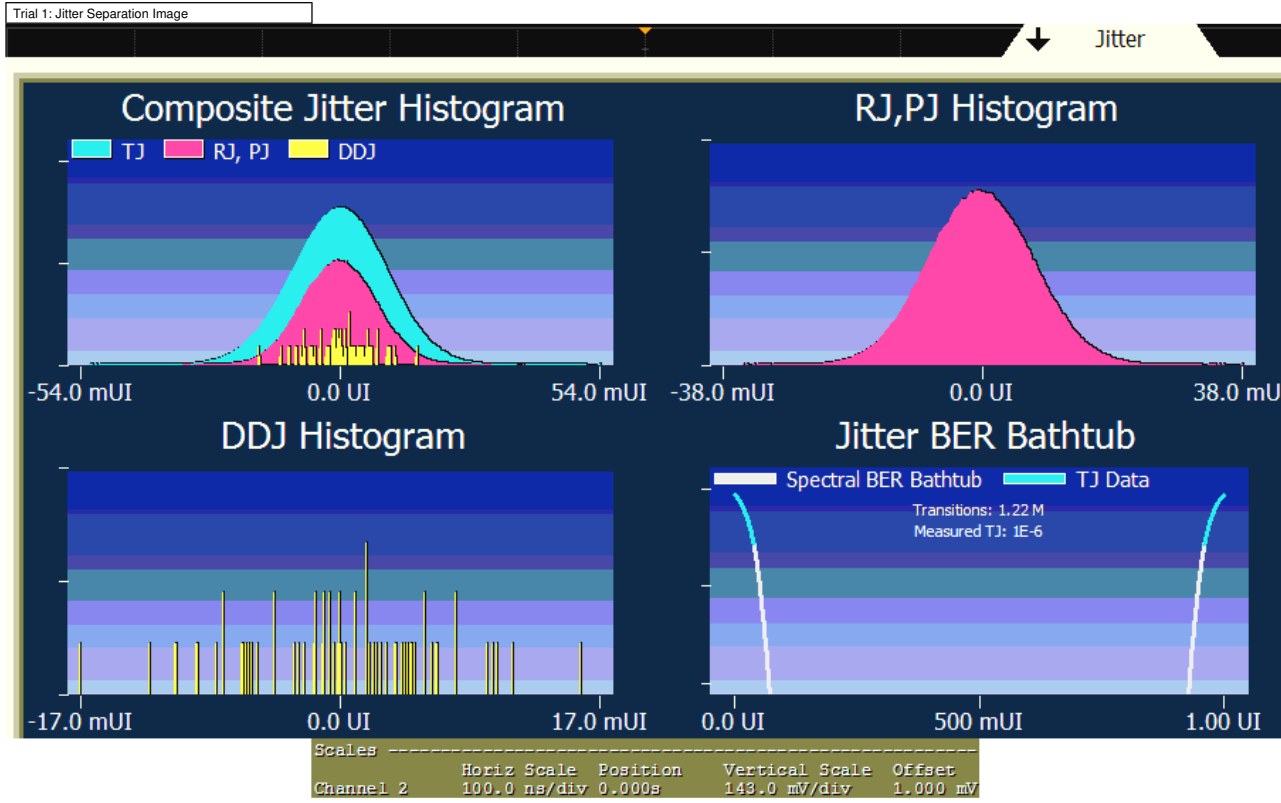
Test Summary: **Pass** Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

**Pass Limits:** <= 270.000 mUI | **Lane 1 Total Jitter Test (Low BitRate) (Worst of 4 Trials)** 108.100 mUI | **# Trials Run:** 4 | **Worst Trial:** Trial 3

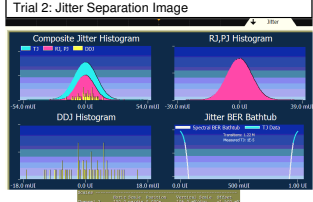
**Overall Summary + details of 4 worst trials**

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	<i>Avg</i>	106.4 mUI	60.60 %																		
	<i>StdDev</i>	1.914 mUI	708.8 m%																		
	<i>Range</i>	4.400 mUI	1.630 %																		
	<i>Min</i>	103.7 mUI	59.96 %																		
	<i>Max</i>	108.1 mUI	61.59 %																		
	<i>Sum</i>	425.5 mUI	242.4 %																		
✓	Trial 1	107.300 mUI	60.3%	(See image)	M	107.3 mUI	66.2337 ps	3.5 mUI	7.4 mUI	26.7 mUI	6.7 mUI	26.7 mUI	33.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 2	106.400 mUI	60.6%	(See image)	M	106.4 mUI	65.6780 ps	3.7 mUI	8.3 mUI	26.3 mUI	6.7 mUI	26.9 mUI	32.3 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 3 (Worst)	108.100 mUI	60.0%	(See image)	M	108.1 mUI	66.7274 ps	3.6 mUI	8.6 mUI	27.1 mUI	6.7 mUI	27.3 mUI	31.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 4	103.700 mUI	61.6%	(See image)	M	103.7 mUI	64.0114 ps	3.7 mUI	7.9 mUI	24.1 mUI	6.6 mUI	25.2 mUI	29.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps

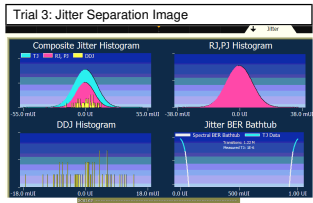
**Trial 1**



**Trial 2**



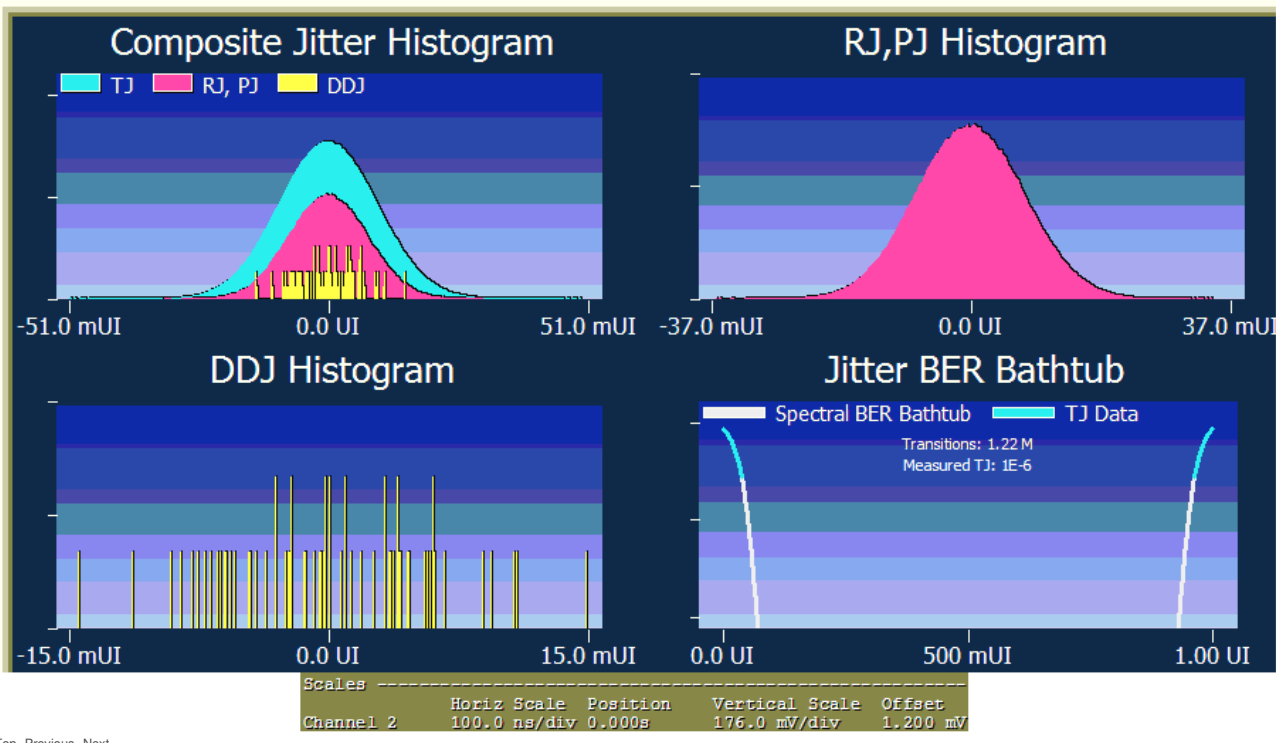
**Trial 3**



**Trial 4**

Trial 4: Jitter Separation Image

Jitter



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✓ Lane 2 - Total Jitter Test (Low BitRate) Reference: DisplayPort Spec v1.2: Table 3.23 VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

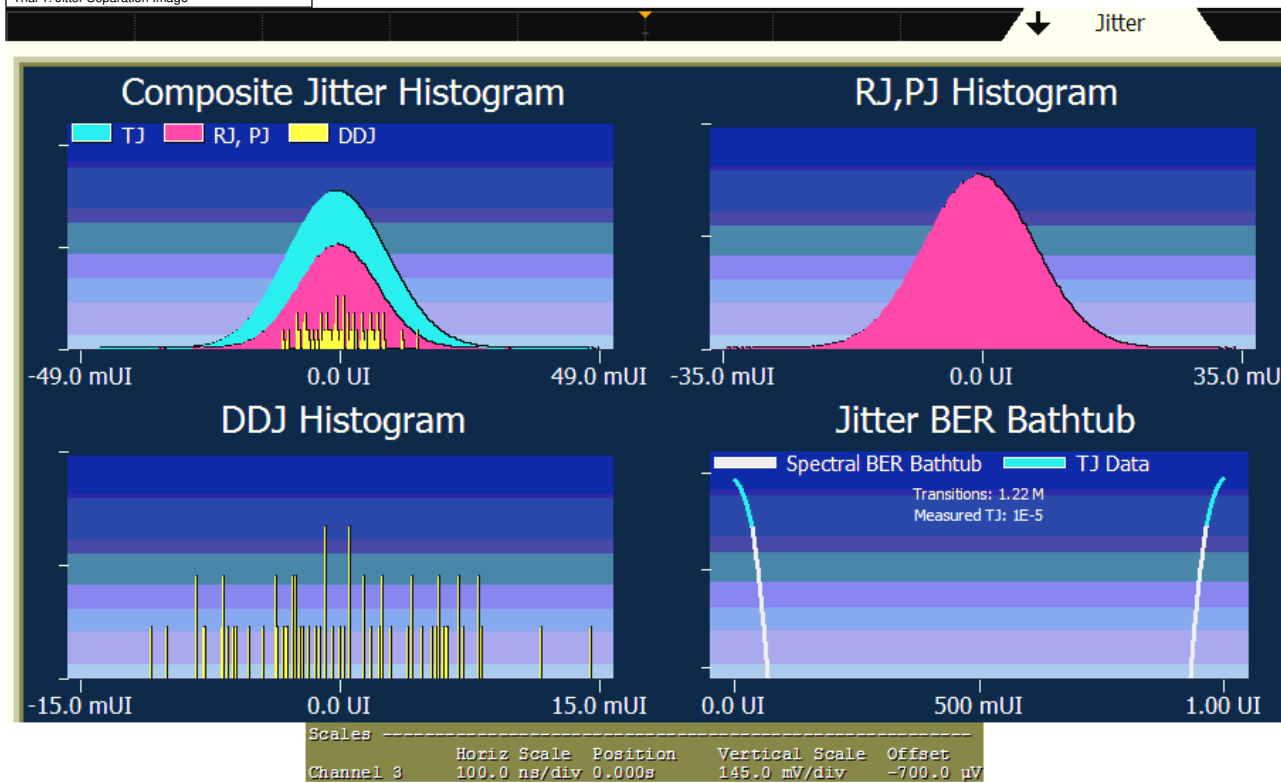
Pass Limits: <= 270.000 mUI Lane 2 Total Jitter Test (Low BitRate) (Worst of 4 Trials) 101.200 mUI # Trials Run: 4 Worst Trial: Trial 3

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	99.90 mUI	63.00 %																		
	StdDev	1.023 mUI	378.9 m%																		
	Range	2.500 mUI	925.9 m%																		
	Min	98.70 mUI	62.52 %																		
	Max	101.2 mUI	63.44 %																		
	Sum	399.6 mUI	252.0 %																		
✓	Trial 1	99.900 mUI	63.0%	(See image)	1.00000000 M	99.9 mUI	61.6655 ps	3.0 mUI	6.2 mUI	20.2 mUI	6.6 mUI	24.6 mUI	25.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 2	99.800 mUI	63.0%	(See image)	1.00000000 M	99.8 mUI	61.6040 ps	3.0 mUI	6.8 mUI	19.9 mUI	6.7 mUI	24.7 mUI	25.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 3 (Worst)	101.200 mUI	62.5%	(See image)	1.00000000 M	101.2 mUI	62.4682 ps	3.0 mUI	6.2 mUI	21.5 mUI	6.6 mUI	24.9 mUI	26.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 4	98.700 mUI	63.4%	(See image)	1.00000000 M	98.7 mUI	60.9250 ps	3.1 mUI	7.0 mUI	19.8 mUI	6.6 mUI	23.3 mUI	24.4 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps

Trial 1

Trial 1: Jitter Separation Image



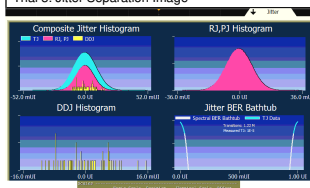
Trial 2

Trial 2: Jitter Separation Image



Trial 3

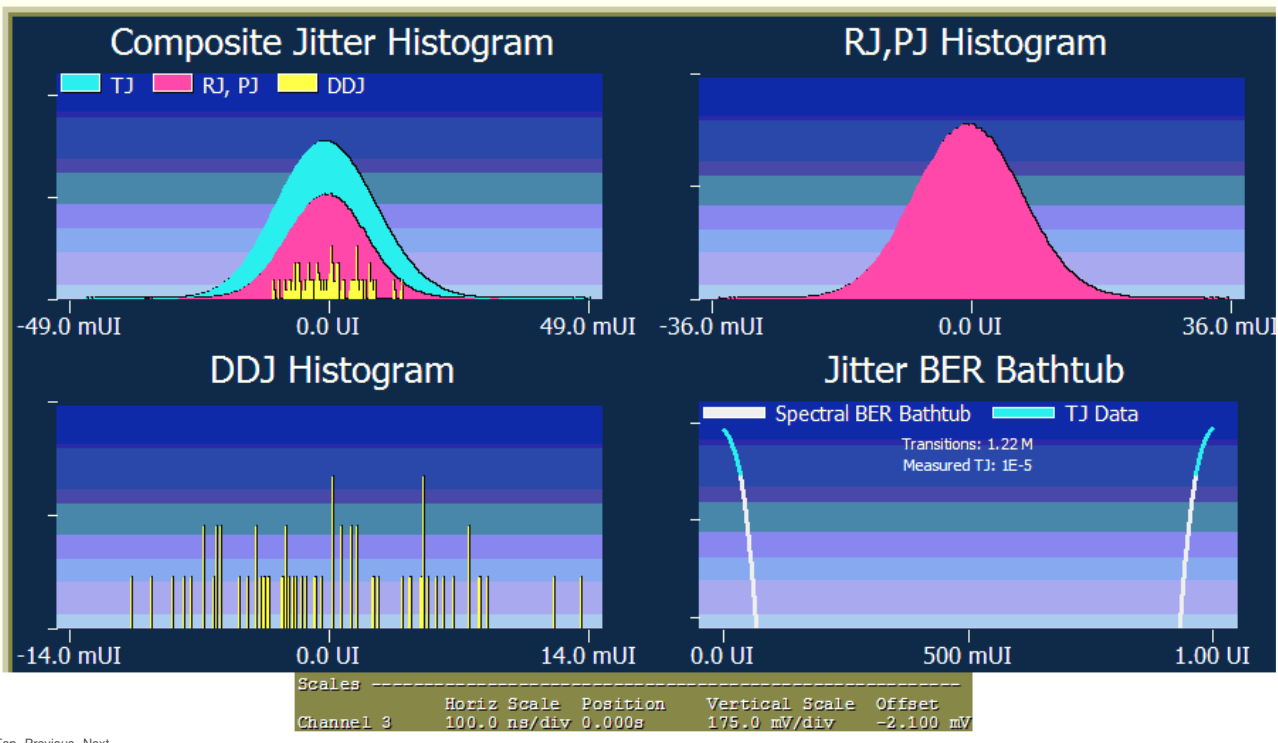
Trial 3: Jitter Separation Image



Trial 4

Trial 4: Jitter Separation Image

Jitter



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**✓ Lane 3 - Total Jitter Test (Low BitRate)** Reference: DisplayPort Spec v1.2; Table 3.23 VESA DisplayPort Standard specification

Test Summary: **Pass** Test Description: To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

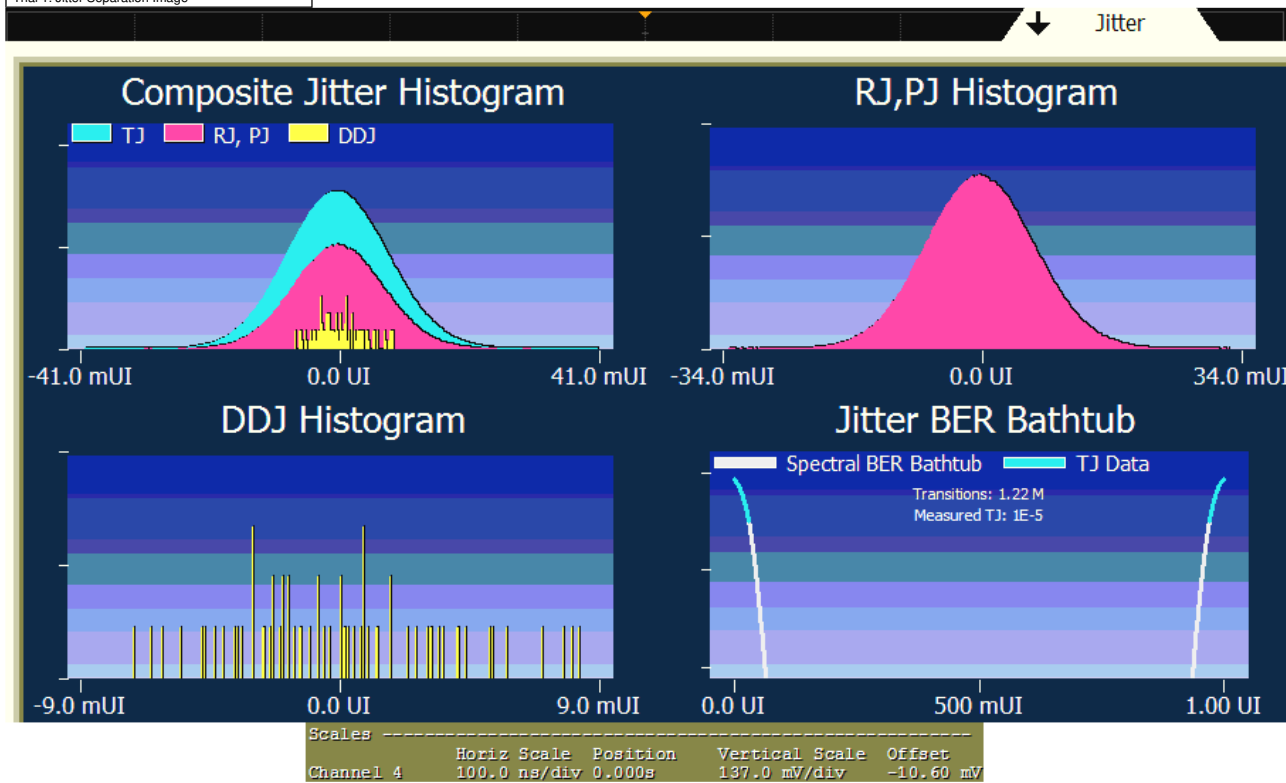
**Pass Limits:** <= 270.000 mUI | **Lane 3 Total Jitter Test (Low BitRate) (Worst of 4 Trials)** 93.600 mUI | **# Trials Run:** 4 | **Worst Trial:** Trial 3

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Margin	Jitter Separation Image	Edges	Total Jitter (TJ) in ps	Periodic Jitter (PJ) in rms	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	<b>Avg</b>	92.08 mUI	65.90 %																		
	<b>StdDev</b>	1.345 mUI	498.2 m%																		
	<b>Range</b>	2.800 mUI	1,037 %																		
	<b>Min</b>	90.80 mUI	65.33 %																		
	<b>Max</b>	93.60 mUI	66.37 %																		
	<b>Sum</b>	368.3 mUI	263.6 %																		
✓	Trial 1	90.800 mUI	66.4%	(See image)	1.00000000 M	90.8 mUI	56.0485 ps	2.3 mUI	4.9 mUI	11.5 mUI	6.6 mUI	15.2 mUI	15.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 2	92.800 mUI	65.6%	(See image)	1.00000000 M	92.8 mUI	57.2829 ps	2.4 mUI	6.4 mUI	13.2 mUI	6.6 mUI	17.2 mUI	17.7 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 3 (Worst)	93.600 mUI	65.3%	(See image)	1.00000000 M	93.6 mUI	57.7768 ps	2.2 mUI	4.3 mUI	13.3 mUI	6.7 mUI	20.0 mUI	20.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps
✓	Trial 4	91.100 mUI	66.3%	(See image)	1.00000000 M	91.1 mUI	56.2336 ps	2.4 mUI	5.8 mUI	11.6 mUI	6.6 mUI	14.2 mUI	14.3 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps

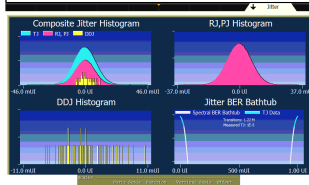
Trial 1

Trial 1: Jitter Separation Image



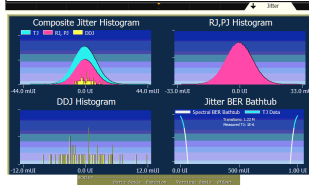
Trial 2

Trial 2: Jitter Separation Image



Trial 3

Trial 3: Jitter Separation Image

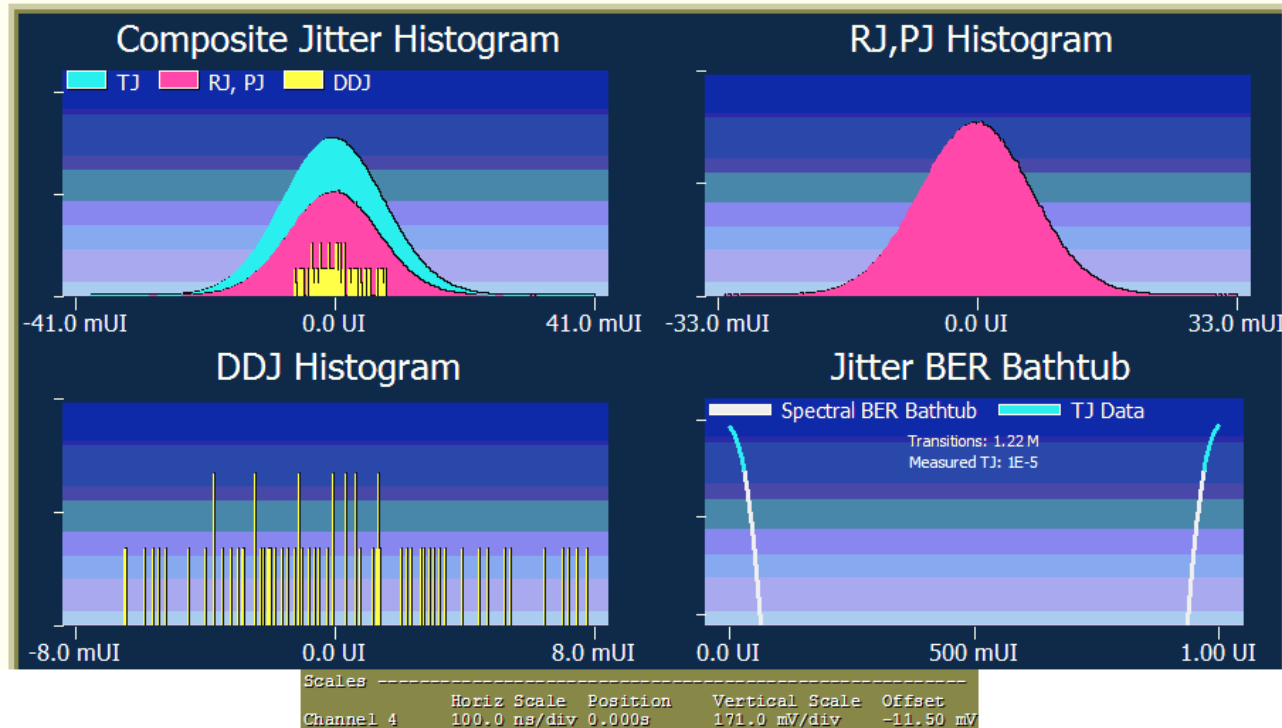


Trial 4



Trial 4: Jitter Separation Image

Jitter



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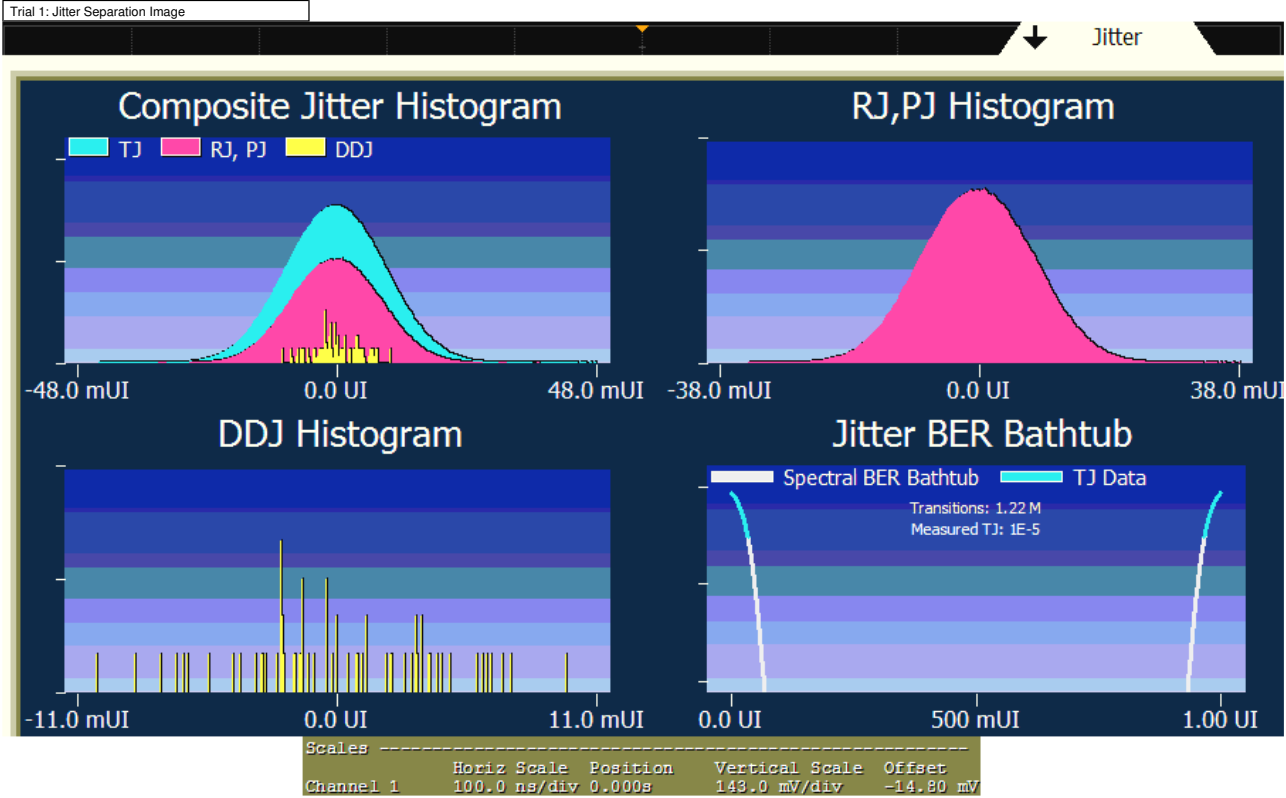
✓ Lane 0 - Non-ISI Jitter Test (Low BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 210.0000 mUI Lane 0 Non ISI Jitter Test (Low BitRate) (Worst of 4 Trials) 80.9000 mUI # Trials Run: 4 Worst Trial: Trial 2

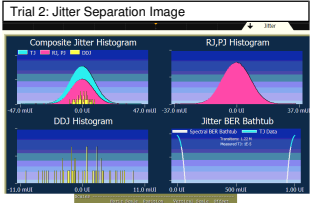
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ)	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	80.05 mUI	61.88 %																			
	StdDev	1.207 mUI	574.7 m%																			
	Range	2.600 mUI	1.238 %																			
	Min	78.30 mUI	61.48 %																			
	Max	80.90 mUI	62.71 %																			
	Sum	320.2 mUI	247.5 %																			
✓	Trial 1	80.8000 mUI	61.5%	(See image)	1.00000000 M	49.8757 ps	98.4 mUI	4.3 mUI	9.7 mUI	18.1 mUI	6.7 mUI	17.6 mUI	20.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 2 (Worst)	80.9000 mUI	61.5%	(See image)	1.00000000 M	49.9382 ps	98.3 mUI	4.3 mUI	10.3 mUI	18.0 mUI	6.7 mUI	17.4 mUI	19.1 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 3	80.2000 mUI	61.8%	(See image)	1.00000000 M	49.5061 ps	99.2 mUI	4.2 mUI	9.2 mUI	17.3 mUI	6.8 mUI	19.0 mUI	19.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 4	78.3000 mUI	62.7%	(See image)	1.00000000 M	48.3332 ps	97.9 mUI	4.5 mUI	8.8 mUI	18.1 mUI	6.7 mUI	19.6 mUI	19.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	

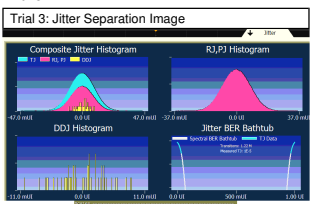
Trial 1



Trial 2



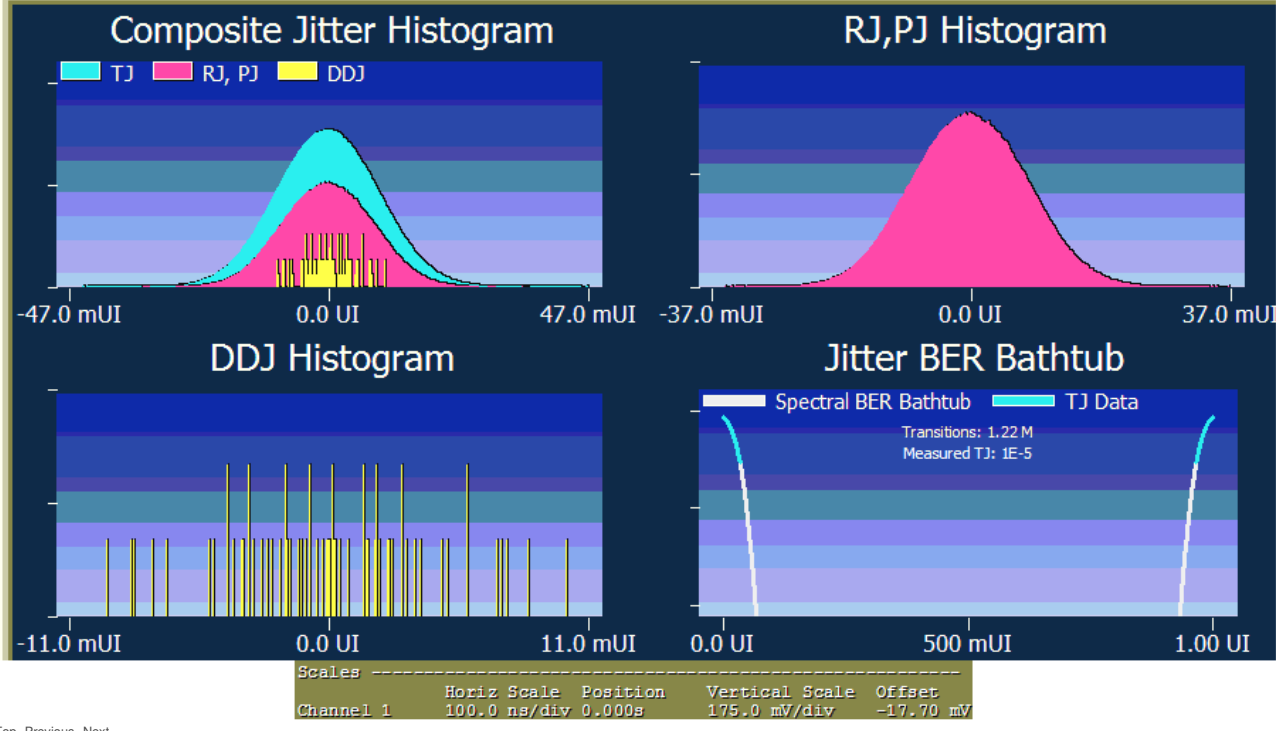
Trial 3



Trial 4

Trial 4: Jitter Separation Image

Jitter



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✓ Lane 1 - Non-ISI Jitter Test (Low BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

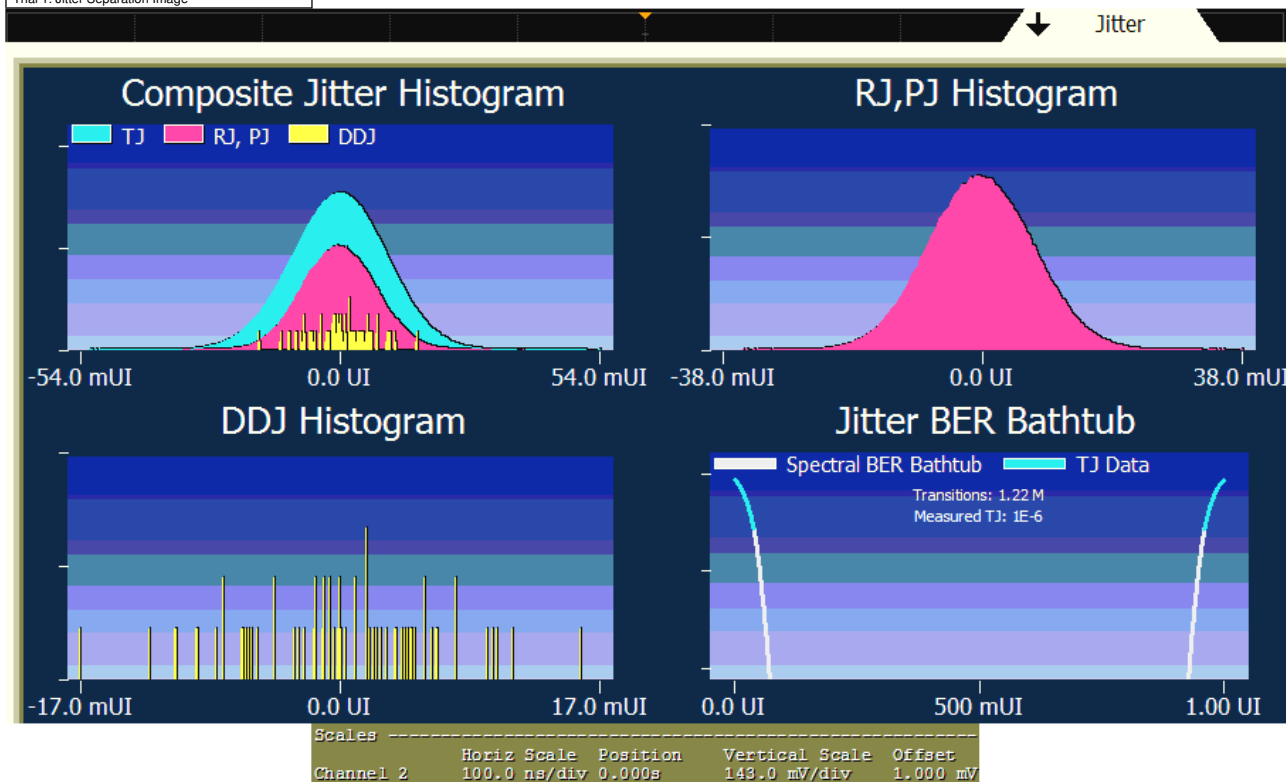
Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 210.00000 mUI Lane 1 Non ISI Jitter Test (Low BitRate) (Worst of 4 Trials) 80.80000 mUI # Trials Run: 4 Worst Trial: Trial 3

Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ)	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	79.85 mUI	61.98 %																			
	StdDev	1.066 mUI	507.7 m%																			
	Range	2.300 mUI	1.095 %																			
	Min	78.50 mUI	61.52 %																			
	Max	80.80 mUI	62.62 %																			
	Sum	319.4 mUI	247.9 %																			
✓	Trial 1	80.6000 mUI	61.6%	(See image)	1.00000000 M	49.7524 ps	107.3 mUI	3.5 mUI	7.4 mUI	26.7 mUI	6.7 mUI	26.7 mUI	33.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 2	79.5000 mUI	62.1%	(See image)	1.00000000 M	49.0733 ps	106.4 mUI	3.7 mUI	8.3 mUI	26.3 mUI	6.7 mUI	26.9 mUI	32.3 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 3 (Worst)	80.8000 mUI	61.5%	(See image)	1.00000000 M	49.8758 ps	108.1 mUI	3.6 mUI	8.6 mUI	27.1 mUI	6.7 mUI	27.3 mUI	31.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 4	78.5000 mUI	62.6%	(See image)	1.00000000 M	48.4560 ps	103.7 mUI	3.7 mUI	7.9 mUI	24.1 mUI	6.6 mUI	25.2 mUI	29.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	

Trial 1

Trial 1: Jitter Separation Image



Trial 2

Trial 2: Jitter Separation Image



Trial 3

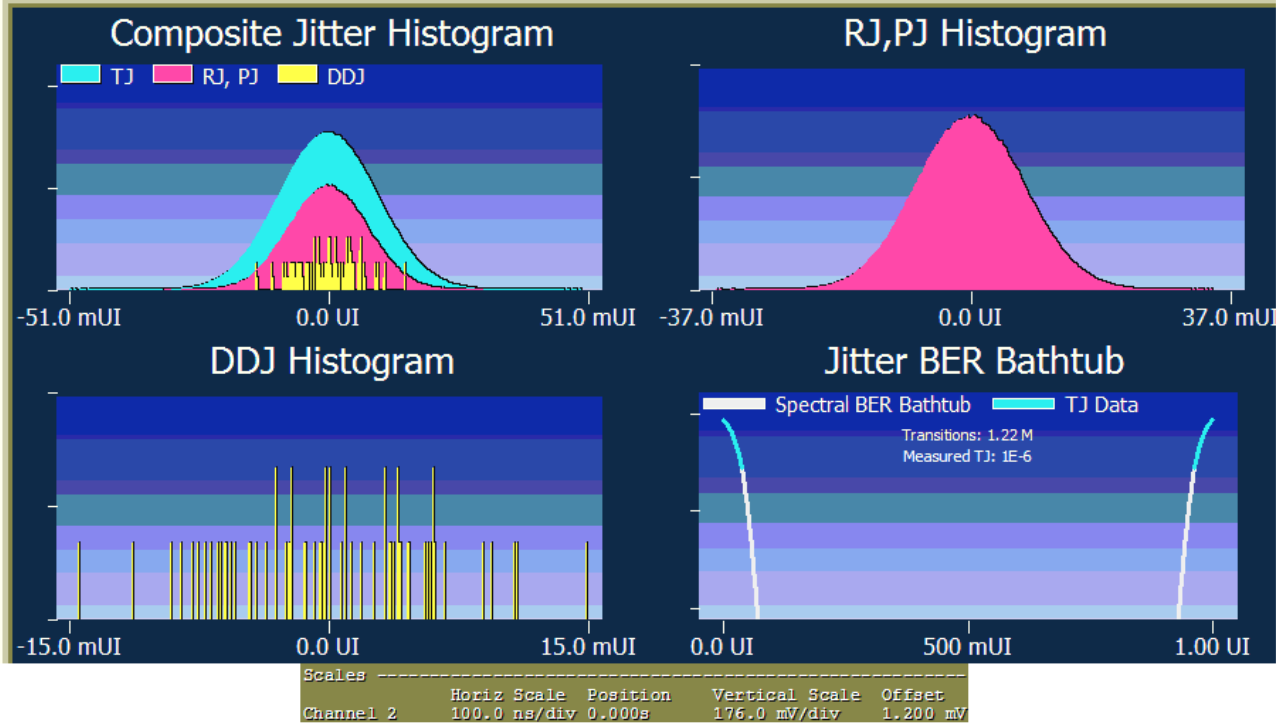
Trial 3: Jitter Separation Image



Trial 4

Trial 4: Jitter Separation Image

Jitter



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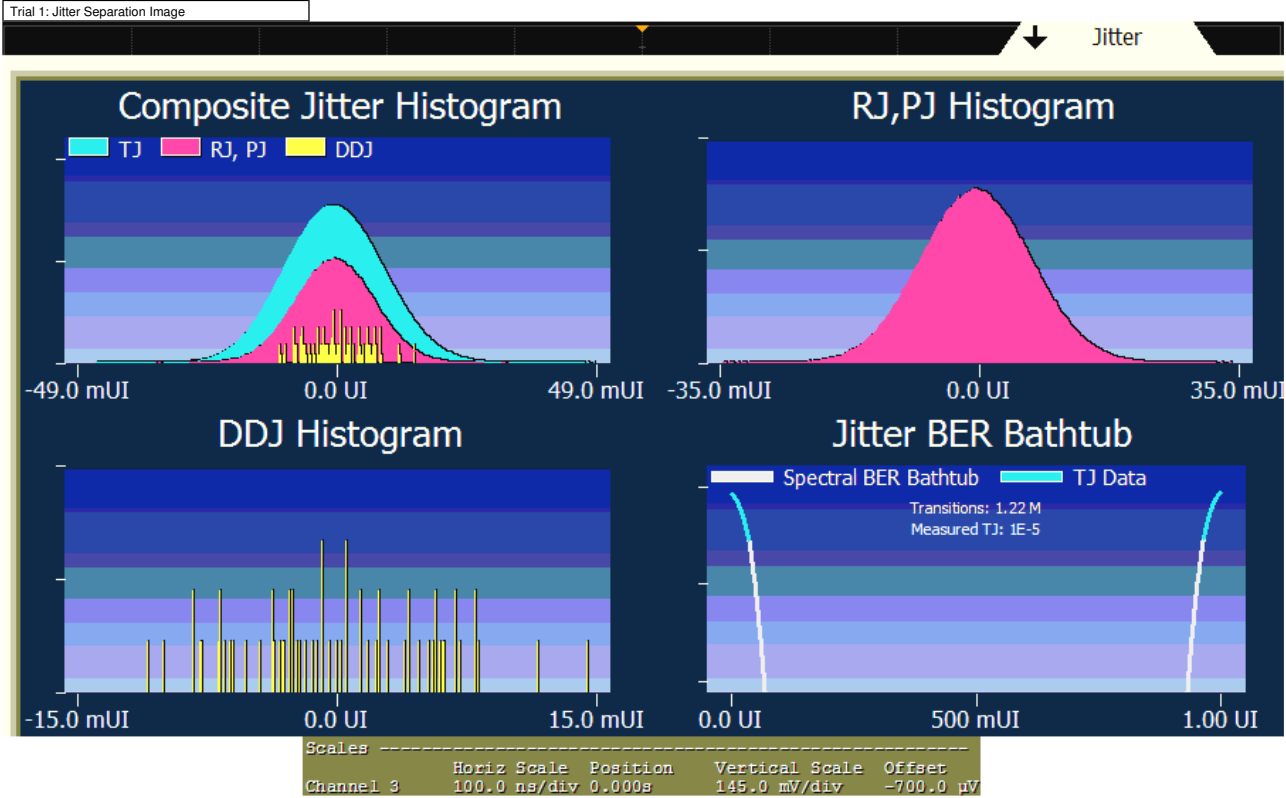
✓ Lane 2 - Non-ISI Jitter Test (Low BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 210.00000 mUI Lane 2 Non ISI Jitter Test (Low BitRate) (Worst of 4 Trials) 76.30000 mUI # Trials Run: 4 Worst Trial: Trial 3

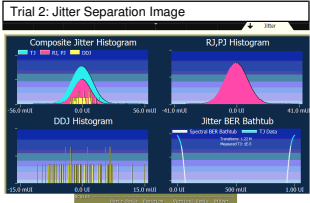
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Margin	Separation Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ)	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	75.53 mUI	64.04 %																			
	StdDev	531.5 μUI	253.1 m%																			
	Range	1.200 mUI	571.4 m%																			
	Min	75.10 mUI	63.67 %																			
	Max	76.30 mUI	64.24 %																			
	Sum	302.1 mUI	256.1 %																			
✓	Trial 1	75.30000 mUI	64.1%	(See image)	1.00000000 M	46.4806 ps	99.9 mUI	3.0 mUI	6.2 mUI	20.2 mUI	6.6 mUI	24.6 mUI	25.6 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 2	75.10000 mUI	64.2%	(See image)	1.00000000 M	46.3573 ps	99.8 mUI	3.0 mUI	6.8 mUI	19.9 mUI	6.7 mUI	24.7 mUI	25.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 3 (Worst)	76.30000 mUI	63.7%	(See image)	1.00000000 M	47.0981 ps	101.2 mUI	3.0 mUI	6.2 mUI	21.5 mUI	6.6 mUI	24.9 mUI	26.9 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 4	75.40000 mUI	64.1%	(See image)	1.00000000 M	46.5425 ps	98.7 mUI	3.1 mUI	7.0 mUI	19.8 mUI	6.6 mUI	23.3 mUI	24.4 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	

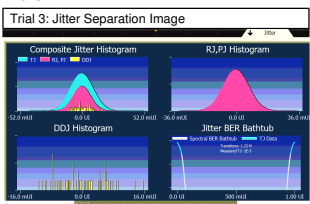
Trial 1



Trial 2



Trial 3

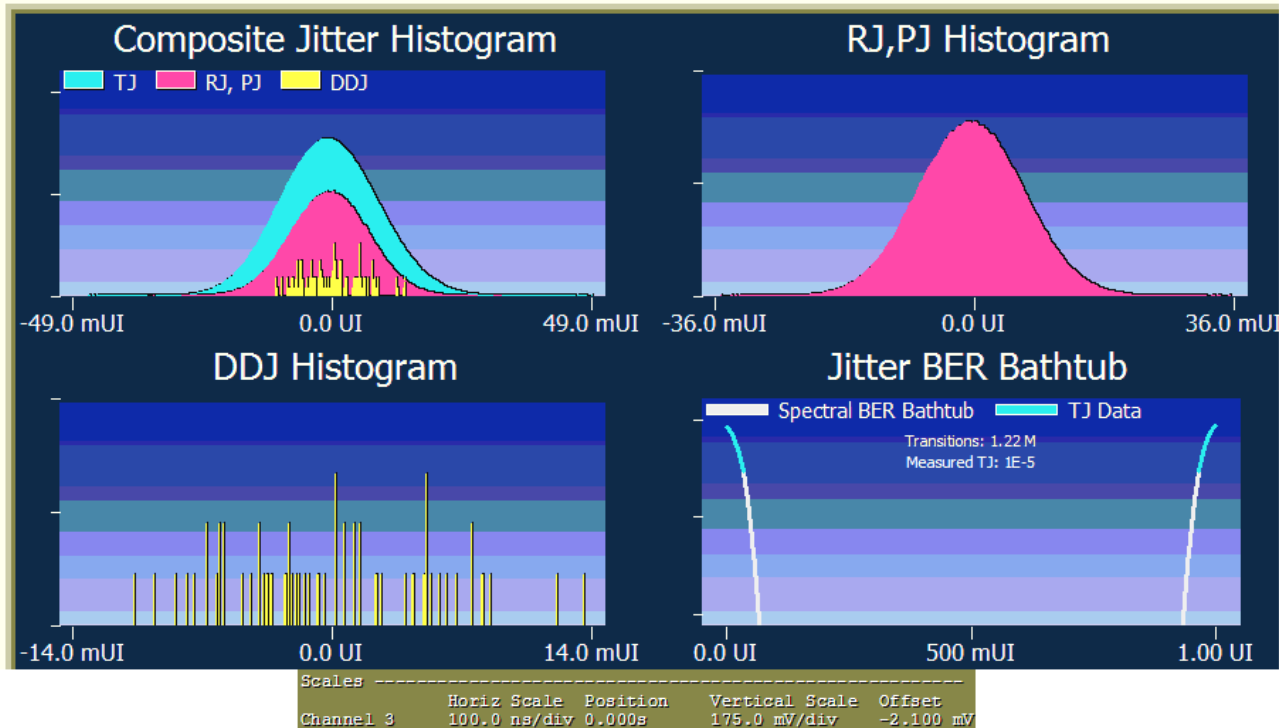


Trial 4



Trial 4: Jitter Separation Image

Jitter



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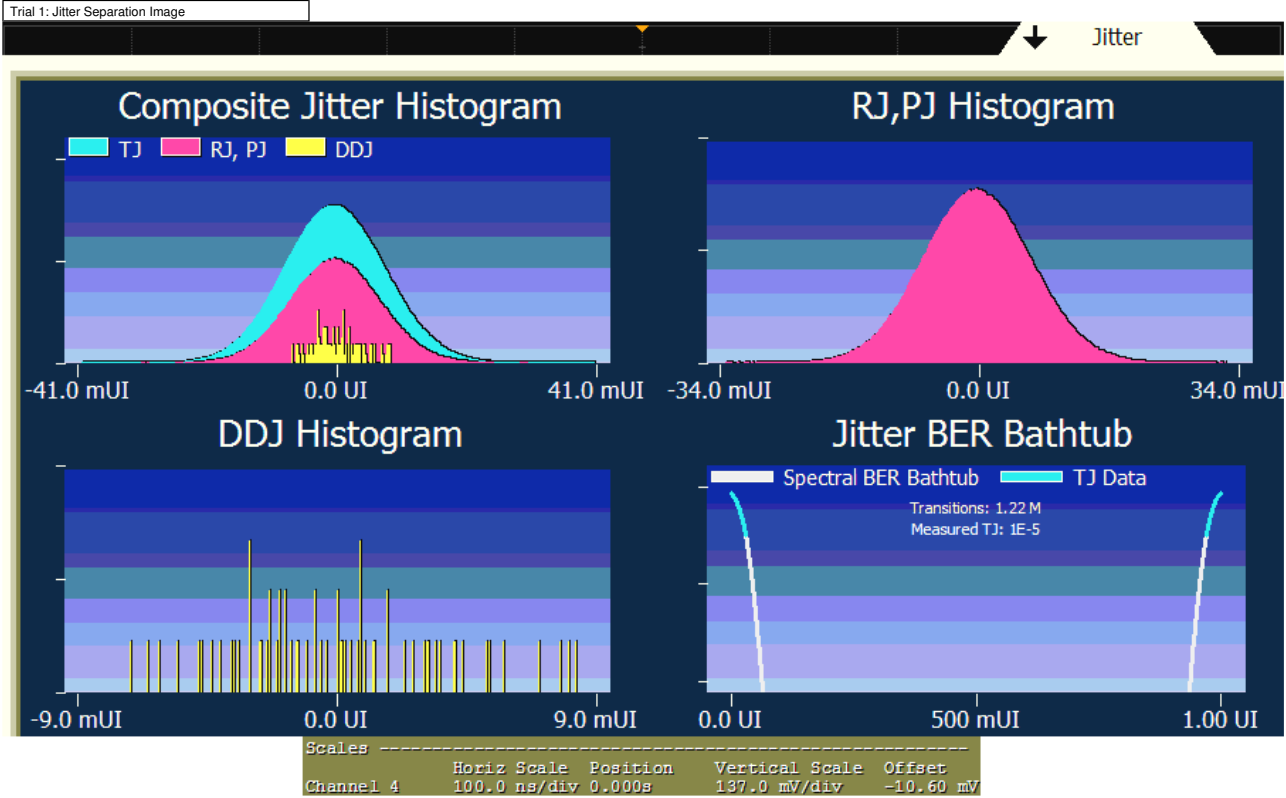
✓ Lane 3 - Non-ISI Jitter Test (Low BitRate) Reference: DisplayPort CTS Sec. 3.11: Figure 3.18 and Figure 3.19 in the VESA DisplayPort Standard specification

Test Summary: Pass Test Description: To evaluate the amount of Non-ISI jitter accompanying the data transmission.  
 Pass Limits: <= 210.00000 mUI Lane 3 Non ISI Jitter Test (Low BitRate) (Worst of 4 Trials) 76.90000 mUI # Trials Run: 4 Worst Trial: Trial 4

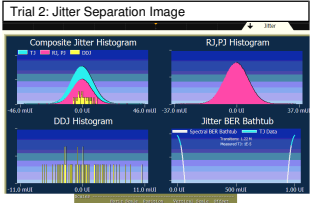
Overall Summary + details of 4 worst trials

Pass	Trial	Actual Value	Jitter Separation Margin	Image	Edges	Non-ISI Jitter in ps	Total Jitter (TJ) mUI	Periodic Jitter (PJ rms)	Periodic Jitter (PJ p-p)	Deterministic Jitter (DJ)	Random Jitter (RJ)	ISI Jitter (ISI)	Data Dependent Jitter (DDJ)	Bit Error Rate (BER)	Test Mode	Test Layer	Test Condition	DUT Type	Test Type	Connection Type	BitRate	
	Avg	75.43 mUI	64.08 %																			
	StdDev	1.362 mUI	648.7 m%																			
	Range	3.300 mUI	1.571 %																			
	Min	73.60 mUI	63.38 %																			
	Max	76.90 mUI	64.95 %																			
	Sum	301.7 mUI	256.3 %																			
✓	Trial 1	75.6000 mUI	64.0%	(See image)	1.00000000 M	46.6659 ps	90.8 mUI	2.3 mUI	4.9 mUI	11.5 mUI	6.6 mUI	15.2 mUI	15.5 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 2	75.6000 mUI	64.0%	(See image)	1.00000000 M	46.6658 ps	92.8 mUI	2.4 mUI	6.4 mUI	13.2 mUI	6.6 mUI	17.2 mUI	17.7 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 3	73.6000 mUI	65.0%	(See image)	1.00000000 M	45.4313 ps	93.6 mUI	2.2 mUI	4.3 mUI	13.3 mUI	6.7 mUI	20.0 mUI	20.0 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	
✓	Trial 4 (Worst)	76.9000 mUI	63.4%	(See image)	1.00000000 M	47.4683 ps	91.1 mUI	2.4 mUI	5.8 mUI	11.6 mUI	6.6 mUI	14.2 mUI	14.3 mUI	E9	Compliance	Physical Layer Tests	Compliance Conditions Only	Source	Differential Tests	Differential Probe	1.62 Gbps	

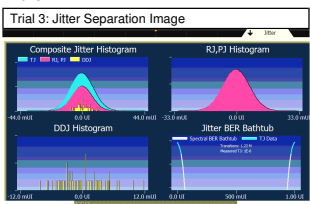
Trial 1



Trial 2



Trial 3

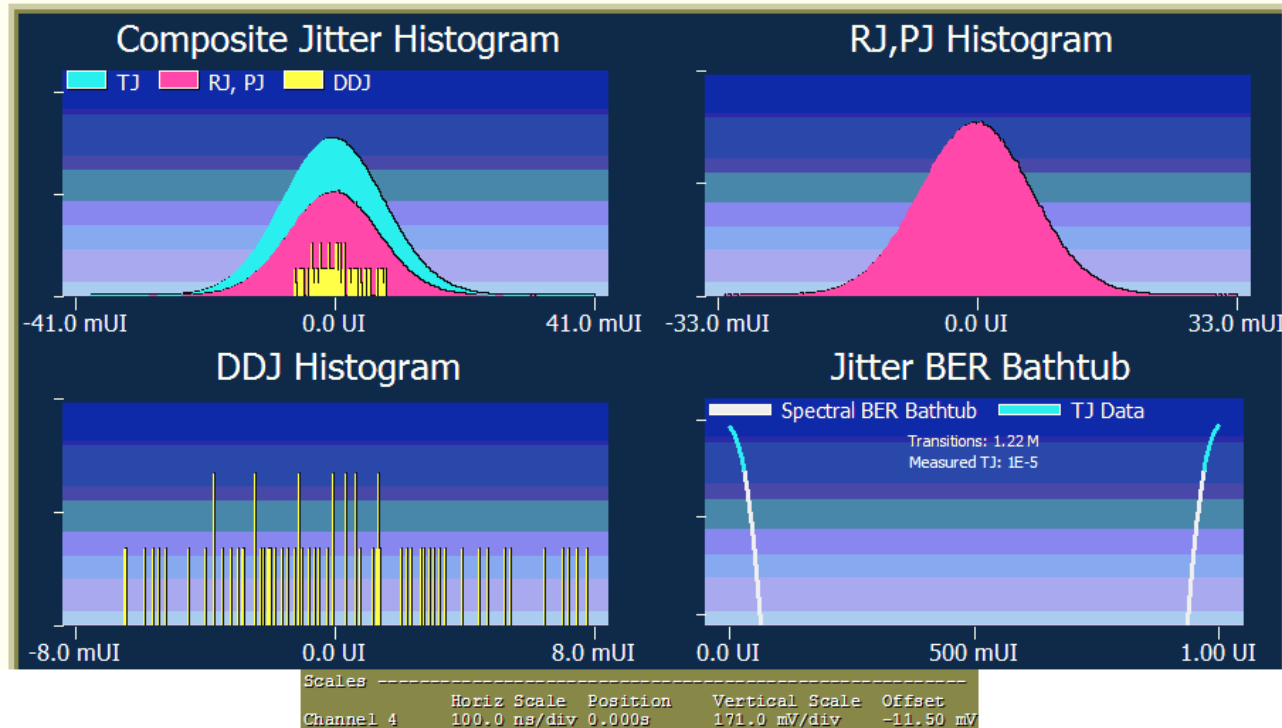


Trial 4



Trial 4: Jitter Separation Image

Jitter



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