Schematic Review Form

Pin #	Name	Info	Violations	*Description*
1	SWAP/POL	I2C_EN = High	Change DNI to use 65k resistors for control pins	Input lane SWAP and polarity control pin when I2C_EN/PIN = Low SWAP/POL = H receive lane polarity swap (retimer mode only) SWAP/POL = L receive lanes swap (retimer and redriver mode) SWAP/POL = No Connect normal working
2	IN_D2p			Channel 2 differential input
3	IN_D2n			Channel 2 differential input
4	HPD_SRC	If HPD_SRC goes to GPU, check the supported GPU voltages. If HPD snoop mode is implemented, leave HPD_SRC floating		Hot plug detect output
5	IN_D1p			Channel 1 differential input
6	IN_D1n			Channel 1 differential input
7	GND			Ground
8	IN_D0p			Channel 0 differential input
9	IN_D0n			Channel 0 differential input
10	I2C_EN/PIN		Use 65k resistors for control pins	I2C_EN/PIN = High; puts device into I2C control mode I2C_EN/PIN = Low; puts device into pin strap mode
11	IN_CLKp			Clock differential input
12	IN_CLKn			Clock differential input
13	VCC			3.3-V power supply
14	VDD			1.1-V power supply
15	SCL_CTL		Use 2k resistors	I2C clock signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I2C
16	SDA_CTL		Use 2k resistors	I2C data signal Note: When I2C_EN/PIN = Low Pin strapping take

				priority and those functions cannot be changed by I2C
17	NC			No connect
18	CEC_EN		Change DNI to use 65k resistors for control pins	CEC control pin for Dongle applications
19	GND			Ground
20	PRE_SEL		Change DNI to use 65k resistors for control pins	De-emphasis pin strap when I2C_EN/PIN = Low. PRE_SEL = L: - 2 dB de-emphasis PRE_SEL = No Connect: 0 dB PRE_SEL = H: Reserved
21	EQ_SEL/A0		Use 65k resistors for control pins	Input Receive Equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5 dB EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14 dB When I2C_EN/PIN = High Address bit 1 Note: (3 level for pin strap programming but 2 level when I2C address)
22	Vsadj		Start with 6.49 k resistor to ground resistor value, tuning depends on compliance result	TMDS-compliant voltage swing control nominal resistor to GND
23	VDD			1.1-V power supply
24	VDD			1.1-V power supply
25	OUT_CLKn			TMDS data clock differential output
26	OUT_CLKp			TMDS data clock differential output
27	HDMI_SEL/A1		Use 65k resistors for control pins	HDMI_SEL when I2C_EN/PIN = Low HDMI_SEL = High: Device configured for DVI HDMI_SEL = Low: Device configured for HDMI (Adaptor ID block is readable through I2C or I2C-over-AUX. When I2C_EN/PIN = High Address bit 2 Note: Weak internal pull down
28	OUT_D0n			TMDS data 0 differential output
29	OUT_D0p			TMDS data 0 differential output
30	GND			Ground
31	OUT_D1n			TMDS data 1 differential output

32	OUT_D1p			TMDS data 1 differential output
33	HPD_SNK	Some monitors have leakage on HPD when they are off, recommend adding a FET switch to gate off the leakage voltage on HPD.		Hot plug detect input
34	OUT_D2n			TMDS data 2 differential output
35	OUT_D2p			TMDS data 2 differential output
36	TX_TERM_CTL		Change DNI to use 65k resistors for control pins	Transmit Termination Control when I2C_EN/PIN = Low TX_TERM_CTL = H, No transmit termination TX_TERM_CTL = L, Transmit termination impedance in 75 to about 150 Ω TX_TERM_CTL = No Connect, automatically selects the termination impedance Data rate (DR) > 3.4 Gbps – 75- to 150-Ω differential near end termination 2 Gbps < DR < 3.4 Gbps – 150- to 300-Ω differential near end termination DR < 2 Gbps – no termination Note: If left floating will be in automatic select mode.
37	VDD			1.1-V power supply
38	SCL_SNK		Use 2k resistors	SCL_SNK
39	SDA_SNK		Use 2k resistors	SDA_SNK
40	SLEW_CTL		Change DNI to use 65k resistors for control pins	Slew rate control when I2C_EN/PIN = Low. SLEW_CTL = H, fastest data rate SLEW_CTL = L, 5 ps slow SLEW_CTL = No Connect, 10 ps slow When I2C_EN/PIN = High Slew rate is controlled through I2C.
41	GND			Ground
42	OE		Start with 0.2 µF, tune depending on the RC time constant delay (Tr) requirement in regard to power ramp up time	Operation enable/reset pin OE = L: Power-down mode OE = H: Normal operation Internal weak pullup: Resets device when transitions from H to L
43	VCC			3.3-V power supply
44	AUX_SRCn	Appears to be NC. If connected in future you will need a 100 nF AC coupled from sink connector/GPU to SNx5DP159.		Source side bidirectional DisplayPort auxiliary for I2C-over-AUX (DP159RGZ only)
45	AUX_SRCp	Appears to be NC. If connected in future you will need a 100 nF AC coupled from sink connector/GPU to SNx5DP159		Source side bidirectional DisplayPort auxiliary for I2C-over-AUX (DP159RGZ only)

46	SCL_SRC	The SNx5DP159 uses clock stretching for DDC transactions. Does the source and sink perform clock stretching? If not, you should use snoop mode. Snoop mode, tie this pin to GND.		SCL_SRC
47	SDA_SRC	The SNx5DP159 uses clock stretching for DDC transactions. Does the source and sink perform clock stretching? If not, you should use snoop mode. Snoop mode, tie this pin to GND.		SDA_SRC
48	VDD			1.1-V power supply

Comments

Place common mode choke on the HDMI output connector will help passing the intra-pair skew compliance testing.
ESD capacitance 0.25pF and ESD devices used for HDMI 2.0.
The SNx5DP159 uses clock stretching for DDC transactions. Does the source and sink perform clock stretching? If not, you should use snoop mode.