DP159 Pattern Generator
User's Guide
January 2015

User's Guide

v0.90

ABSTRACT

This document describes how to use and configure the DP159 internal pattern generator. Customers can use this document to understand how to program the DP159 pattern generator. This document should only be used with the DP159.

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Revision Notes

Version	Date	Notes
0.90	1/28/2015	- Initial Draft

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1 Overview

1.1 What is the DP159?

.The SN65DP159 device is a dual mode DisplayPort to TMDS retimer supporting DVI and HDMI 1.4b as well as HDMI 2.0.

1.2 PATTERNS SUPPORTED

The DP159 supports the following patterns:

- PRBS7
- PRBS11
- PRBS15
- PRBS20
- PRBS23
- PRBS31
- Clock
- Custom (16-bit or 20-bit based on state of PG_CP20 bit)

1.3 Registers

For the DP159, the pattern generator registers are located in Page 1. Software must select page 1 before attempting to access the pattern generator registers. An example of how to program the pattern generator registers is given in section 3 of this document.

Table 1-1. Page Register

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
0xFF	1:0	2'b00	PAGE_SELECT. 00 – Page 0 01 – Page 1	RW

Table 1-2. Pattern Generator Control Registers (Page 1)

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
0x18	7:4	4'b0000	Reserved.	RU
			PG_LD[3:0]. Load pattern-generator controls into TX lane. When asserted high, the PG_TO, PG_SEL, PG_LEN, PG_CP20, and PG_CP values are enabled into the corresponding TX lane. These values are then latched and held when PG_LD[n] is subsequently de-asserted low. 1 bit per lane.	
	3	1'b0	PG_LD3. Lane 3 is OUT_CLKP/N. Toggle from 0 to 1 and back to 0 to enable PG for this lane.	RW
	2	1'b0	PG_LD2. Lane 2 is OUT_D0P/N. Toggle from 0 to 1 and back to 0 to enable PG for this lane.	RW
	1	1'b0	PG_LD1. Lane 1 is OUT_D1P/N. Toggle from 0 to 1 and back to 0 to enable PG for this lane.	RW
	0	1'b0	PG_LD0. Lane 0 is OUT_D2P/N. Toggle from 0 to 1 and back to 0 to enable PG for this lane.	RW
0x19	7:4	4'b0000	Reserved.	R
	3:0	4'b0000	PG_ERR_INJ[3:0]. Inject error into pattern. Upon the rising edge of PG_ERR_INJ[n], an error is inserted into the transmitted pattern of the corresponding lane.	RW
0x1A	7	1'b0	PG_CP20. Custom pattern length 20/16 bits. 0 – 16 bits 1 – 20 bits	RW

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
	6	1'b0	Reserved.	R
	5	1'b0	PG_TO. Pattern generator timing-only mode.	RW
	4:2	3'b000	PG_LEN[2:0]. PRBS pattern length 000 – PRBS7 001 – PRBS11 010 – PRBS23 011 – PRBS31 100 – PRBS15 101 – PRBS15 110 – PRBS20 111 – PRBS20	RW
	1:0	2'b00	PG_SEL[1:0]. Pattern select. 00 – Disabled 01 – PRBS based on PG_LEN[2:0] 10 – Clock pattern 11 – Custom pattern based on PG_CP[19:0].	RW
0x1C	7:0	'h00	PG_CP[7:0]. Custom pattern data.	RW
0x1D	7:0	'h00	PG_CP[15:8]. Custom pattern data.	RW
0x1E	7:4	4'b0000	Reserved.	R
	3:0	4'b0000	PG_CP[19:16]. Custom pattern data. Used when PG_CP20 = 1'b1.	RW

2 References

1. SN65DP159 Datasheet (SLLSEJ2)
2. *Aardvark Adapter User Manual*

3 Total Phase Aardvark I2C Host Adapter Scripts

The scripts in the following sections are provided to configure the DP159 for transmitting a pattern.

3.1 PRBS7

This script will configure the DP159 for transmitting PRBS7 on lanes 0 thru 2.

```
<aardvark>
   <configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
   <i2c_bitrate khz="100"/>

======Select  Page 1======
<i2c_write addr="0x5e" count="1" radix="16">FF 01</i2c_write>/>

======Make sure PG_LD is deasserted before changing pattern controls ======
<i2c_write addr="0x5e" count="1" radix="16">18 00</i2c_write>/>

======Now change the pattern controls to PRBS7======
<i2c_write addr="0x5e" count="1" radix="16">1A 01</i2c_write>/>

======Now set the PG_LD for the channel of interest=====
<i2c_write addr="0x5e" count="1" radix="16">18 07</i2c_write>/>

======Be sure to deassert the PG_LDs======
<i2c_write addr="0x5e" count="1" radix="16">18 00</i2c_write>/>

======Select  Page 0======
<i2c_write addr="0x5e" count="1" radix="16">FF 00</i2c_write>/>

</aardvark>
```

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