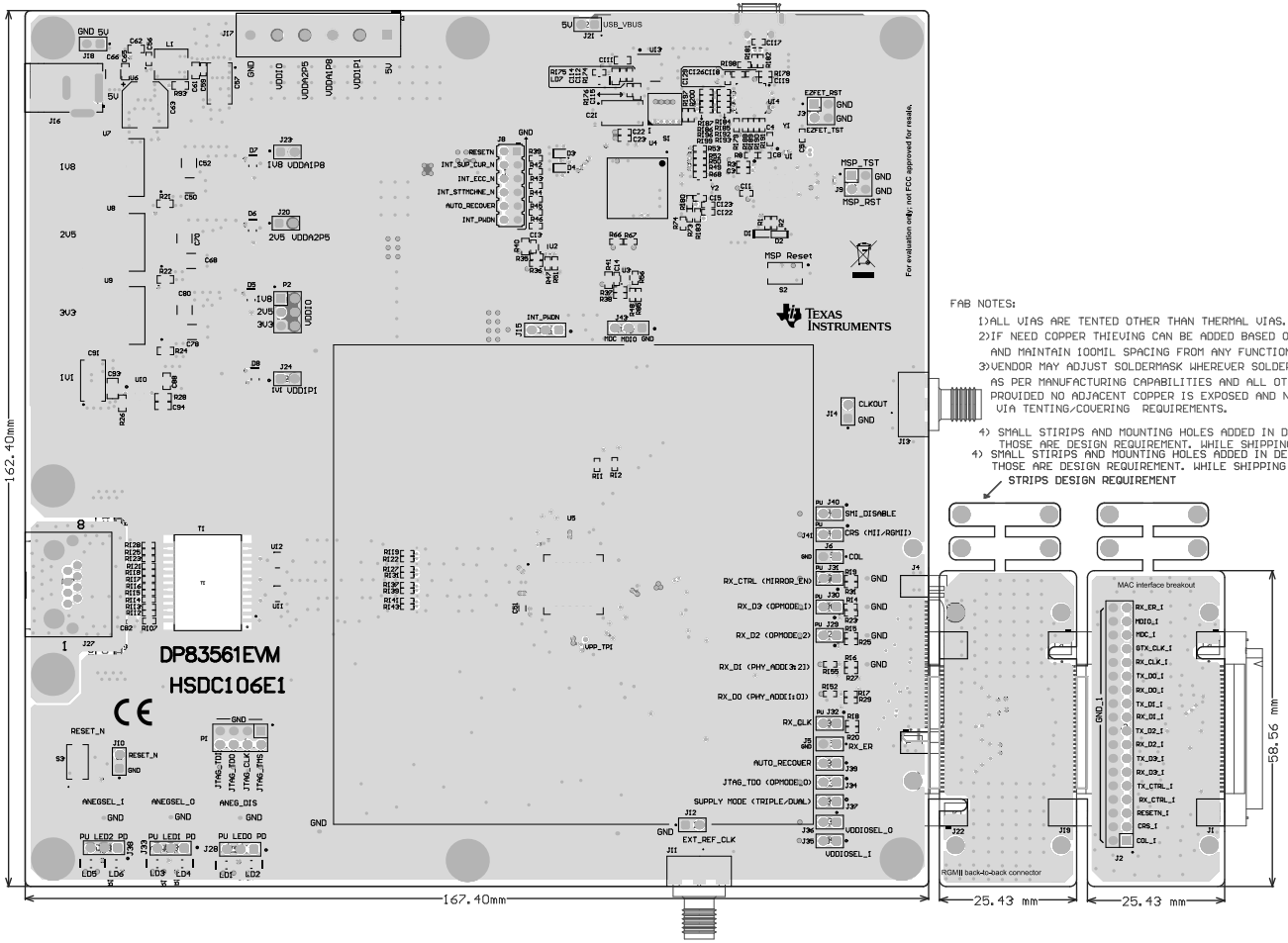

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.70mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	5.00mil	4.6	
5	GND1	Copper	1.40mil		
6	Dielectric 2	FR-4 High Tg	5.00mil	4.6	
7	SIG1	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	32.00mil	4.6	
9	SIG2	Copper	1.40mil		
10	Dielectric 4	FR-4 High Tg	5.00mil	4.6	
11	GND2	Copper	1.40mil		
12	Dielectric 5	FR-4 High Tg	5.00mil	4.6	
13	Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.70mil	3.5	
15	Bottom Overlay				

FAB NOTES:

1) ALL VIAS ARE TENTED OTHER THAN THERMAL VIAS..
2) IF NEED COPPER THIEVING CAN BE ADDED BASED ON COPPER BALANCING CALCULATION AND MAINTAIN 100MIL SPACING FROM ANY FUNCTIONAL CONDUCTOR.
3) VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE SAME SIZE(1:1) AS PER MANUFACTURING CAPABILITIES AND ALL OTHER SOLDERMASK PADS SHALL NOT BE MODIFIED PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT PRODUCED WITH ANY STATED VIA TENTING/COVERING REQUIREMENTS.
4) SMALL STIRIPS AND MOUNTING HOLES ADDED IN DESIGN THOSE ARE DESIGN REQUIREMENT. WHILE SHIPPING BOARDS, PLEASE HAND OVER TO CUSTOMER
4) SMALL STIRIPS AND MOUNTING HOLES ADDED IN DESIGN THOSE ARE DESIGN REQUIREMENT. WHILE SHIPPING BOARDS, PLEASE HAND OVER TO CUSTOMER

Impedance Control:

Differential Controlled to 100 Ohms (+/-10%)
All 6 mil traces with 12 mil spacing on Layers 1 and 6

Single Ended Controlled to 50 Ohms (+/-10%)
All 8 mil traces on Layers 1, 3, and 6

Differential Controlled to 90 Ohms (+/-10%)
All 5 mil traces with 4.6 mil spacing on Layers 1 and 6
All 5 mil traces with 6.1 mil spacing on Layer 3

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ1 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: No Variations

1000.00mil

DESIGN INFORMATION	
MIN. TRACK WIDTH:	6 MIL
MIN. CLEARANCE:	4.6 MIL
MIN. VIA PAD SIZE:	18 MIL

MINIMUM ANNULAR RING 0.127mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] MATTE [X] GREEN [ ] BLUE [ ] OTHER
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER MECH LAYER 1 [ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

TEXAS INSTRUMENTS

PROJECT TITLE: DP83561EVM
DESIGNED FOR: TI
FILE NAME: HSDC106A_EVM_DP83561_64p.PcbDoc
ENGINEER: Justin
LAYOUT BY: Tessolve
SCALE: 1.00
ALTIUM DESIGNER VERSION: 18.1.9.240

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Board S