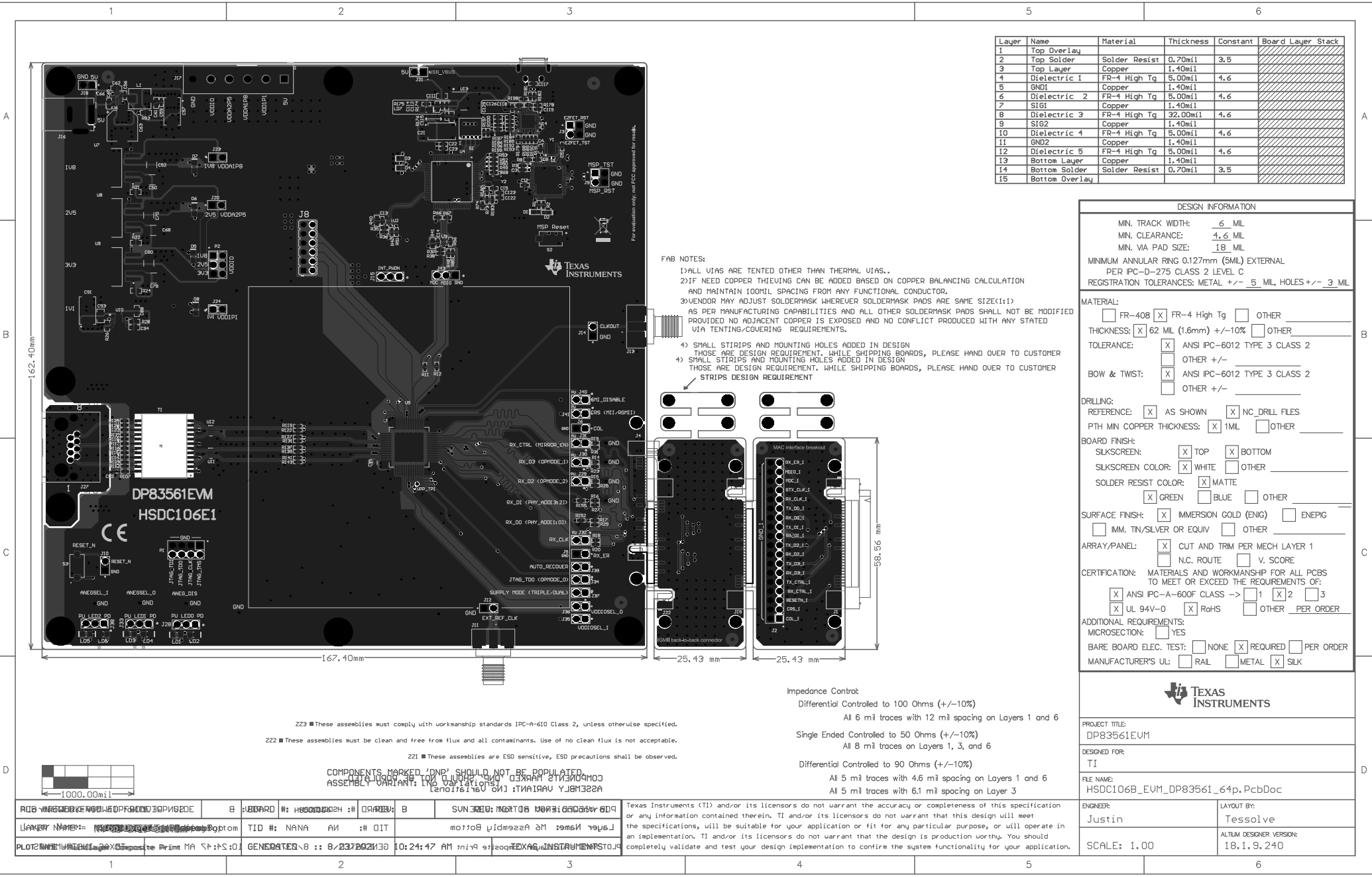




Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.70mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	5.00mil	4.6	
5	GND1	Copper	1.40mil		
6	Dielectric 2	FR-4 High Tg	5.00mil	4.6	
7	SIG1	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	32.00mil	4.6	
9	SIG2	Copper	1.40mil		
10	Dielectric 4	FR-4 High Tg	5.00mil	4.6	
11	GND2	Copper	1.40mil		
12	Dielectric 5	FR-4 High Tg	5.00mil	4.6	
13	Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.70mil	3.5	
15	Bottom Overlay				

- FAB NOTES:
- 1) ALL VIAS ARE TENTED OTHER THAN THERMAL VIAS.
 - 2) IF NEED COPPER THIEVING CAN BE ADDED BASED ON COPPER BALANCING CALCULATION AND MAINTAIN 100MIL SPACING FROM ANY FUNCTIONAL CONDUCTOR.
 - 3) VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE SAME SIZE (1:1) AS PER MANUFACTURING CAPABILITIES AND ALL OTHER SOLDERMASK PADS SHALL NOT BE MODIFIED PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT PRODUCED WITH ANY STATED VIA TENTING/COVERING REQUIREMENTS.
 - 4) SHALL STRIPS AND MOUNTING HOLES ADDED IN DESIGN THOSE ARE DESIGN REQUIREMENT. WHILE SHIPPING BOARDS, PLEASE HAND OVER TO CUSTOMER
 - 4) SHALL STRIPS AND MOUNTING HOLES ADDED IN DESIGN THOSE ARE DESIGN REQUIREMENT. WHILE SHIPPING BOARDS, PLEASE HAND OVER TO CUSTOMER STRIPS DESIGN REQUIREMENT

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 4.6 MIL
MIN. VIA PAD SIZE: 18 MIL

MINIMUM ANNUAL RING 0.127mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- .5 MIL, HOLES +/- .3 MIL

MATERIAL:

☐ FR-408 ☒ FR-4 High Tg ☐ OTHER

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☒ MATTE
☐ GREEN ☐ BLUE ☐ OTHER

SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENFPG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☒ CUT AND TRIM PER MECH LAYER 1
☐ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

MANUFACTURER'S UL: ☐ RAIL ☐ METAL ☒ SILK

222 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

222 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

221 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: TWO VARIATIONS

REV: 1.0	DATE: 08/23/2021	BY: J. S. J.	APP: J. S. J.	CHK: J. S. J.	DESIGNED BY: J. S. J.	DATE: 08/23/2021	TIME: 10:24:47 AM	FILE: DP83561EVM_HSDC106E1_PCB.DOC
DESIGNED BY: J. S. J.								
DATE: 08/23/2021								
TIME: 10:24:47 AM								
FILE: DP83561EVM_HSDC106E1_PCB.DOC								

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

TEXAS INSTRUMENTS

PROJECT TITLE: DP83561EVM

DESIGNED FOR: TI

FILE NAME: HSDC106E1_EVM_DP83561_64p.PcbDoc

ENGINEER: Justin

LAYOUT BY: Tesselove

SCALE: 1.00

ALTIUM DESIGNER VERSION: 18.1.9.240