//-----------------------------------------------------------------------////// 2019.03.20 DP83640 Synchronous Ethernet Mode EVM// AN-1728 IEEE 1588 Precision Time Protocol Time// Synchronization Performance// (SNLA098A October 2007?Revised April 2013)// AN-1729 DP83640 IEEE 1588 PTP Synchronized Clock Output// (SNLA099D September 2007?Revised April 2013)// AN-1730 DP83640 Synchronous Ethernet Mode: Achieving // Sub-Nanosecond Accuracy in PTP Applications// (SNLA100A September 2007?Revised April 2013)// AN-2006 Synchronizing a DP83640 PTP Master to a GPS Receiver// (SNOA548A May 2010?Revised April 2013)// USB-2-MDIO User's Guide(SNLU197?February 2016)// IEEE 1588 Precision Time Protocol Transceiver Demo Board User Guide // DP83640 TP&FX Demo Board////------------------------------------------------------------------------//// SNLA099D

begin//script TI// read 0000//3.1.4 IEEE 1588 Triggers // 3.1.4.1 Initialing a Trigger// Trigger == slave// PTP 1588 Operation Page4 0x14 and 0x15

0013 0004 // ★Page40014 0002 // PTP\_CTL= trigger0, disable state to Enable0014 0014 // PTP\_CTL= trigger0+LOAD\_CLK0015 0000 // PTP\_TDR= Start\_time\_ns[15:0] 0015 0000 // PTP\_TDR= Start\_time\_ns[29:16] 0015 1000 // PTP\_TDR= Start\_time\_sec[15:0] 0015 0000 // PTP\_TDR= Start\_time\_sec[31:16] 0014 0044 // PTP\_CTL= trigger0+TRIG\_LOAD//Pulsewidth (2-bit seconds, 30-bit nanoseconds) 0015 0000 // PTP\_TDR= Pulsewidth[15:0] 0015 0000 // PTP\_TDR= Pulsewidth[31:16] // Pulsewidth2 (2-bit seconds, 30-bit nanoseconds for Periodic Pulse) or (16-bit seconds for Periodic Edge) 0015 0001 // PTP\_TDR= Pulsewidth2[15:0] (for Triggers 0 and 1 only) 0015 0000 // PTP\_TDR= Pulsewidth2[31:16] (for Triggers 0 and 1 only) 0014 0004 // PTP\_CTL= trigger0+LOAD//0014 0100 // PTP\_CTL= trigger0+TRIG\_EN0014 0020001500150015001500150015001500150013 0005 // Page5//0014 D901 // GPIO9//0014 C001 // GPIO30014 C901 // GPIO9//0013 0004 // Page4//0014 0100 // PTP\_CTL= trigger0+TRIG\_EN0013 0004 // Page40017 // PTP Trigger Status //// PTP Rate////0013 0004 // Page5////0018 0000 // PTP\_RATEL= LSB16bit////0019 8020 // PTP\_RATEH= 10bit////0018 6DC6 // PTP\_RATEL= LSB16bit -SNLA099D////0019 8034 // PTP\_RATEH= 10bit -SNLA099D//0013 0005 // Page5//001F 0013 //2. Write 0x0013 to PTP\_TRDH//001E 12D0 //3. Write 0x12D0 to PTP\_TRDL//0013 0004 // Page4//0019 C000 //4. Write 0xC000 to PTP\_RATEH//0018 2844 //5. Write 0x2844 to PTP\_RATEL//★Strap Pin GPIO1 to high or PHYCR2[2] to clear0013 0000001C 3000 // Synchronous Ethernet Enable, Enable RX\_CLK on CLK\_OUT001F // Only [0]PCF\_EN is 1. Other bits are all 0.//2. 0013 0006 // ★Page60014 8019 // Write 0x8019 to PTP\_COC, CLK\_OUT\_EN+25div=10MHz//0014 800A // CLK\_OUT\_EN+10div=25MHz0013 0004 // ★Page40014 0004 // Write 0x0004 to PTP\_CTL. PTP clock enabled//3.0013 0005 // ★Page50015 1C0F // Write 0x1C0F to PTP\_EVNT0015 5C0F // Write 0x5C0F to PTP\_EVNT.

0013 0004 // ★Page4001E // Read PTP\_ESTS and then set the value to bit-0.001E // 001E // 001E // // Read PTP\_EDATA001F // 15：0001F // 29:16001F // 15：0001F // 31:16 //// PTP Event Configuration//0013 0005 // Page5//0015 1905 // PTP\_EVNT= EVNT\_RISE,single+GPIO9+SEL2+WR//0015 5905 // EVNT\_RISE、GPIO9 input、、SEL2+WR// PTP Transmit Configuration0016 80A3 // PTP\_TXCFG0 Enable0017 0000 // PTP\_TXCFG1 Message Enable0018 000F // PSF\_CFG0 Status Frame Enable0019 0003 // PTP\_RXCFG0 PTP\_VER1,EN001A 0000 // PTP\_RXCFG1 ReDATA// PTP Trigger Configuration//0013 0005 // Page5//0014 C901 // PTP\_TRIG= Pulse+Periodic+GPIO9+WR//0014 C301 // PTP\_TRIG= Pulse+Periodic+GPIO2+WR Output to GPIO3//// monitor//0013 0000 // Page0//0005 // BASE, Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), Address 0x05//0005 // BASE, Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page), Address 0x05//0006 // BASE, Auto-Negotiate Expansion Register (ANER), Address 0x06//0007 // BASE, Auto-Negotiation Next Page Transmit Register (ANNPTR), Address 0x07//0010 // BASE, PHY Status Register (PHYSTS), Address 0x10//0012 // BASE, MII Interrupt Status and Event Control Register (MISR), Address 0x12////0013 0000 // Page0//0014 // Page0, False Carrier Sense Counter Register (FCSCR), Address 0x14//0015 // Page0, Receiver Error Counter Register (RECR), Address 0x15//0016 // Page0, 100 Mb/s PCS Configuration and Status Register (PCSR), Address 0x16//0017 // Page0, RMII and Bypass Register (RBR), Address 0x17//0018 // LED Direct Control Register (LEDCR), Address 0x18//0019 // PHY Control Register (PHYCR), Address 0x19//001A // 10Base-T Status/Control Register (10BTSCR), Address 0x1A//001B // CD Test and BIST Extensions Register (CDCTRL1), Address 0x1B//001C // PHY Control Register 2 (PHYCR2), Address 0x1C//001D // Energy Detect Control (EDCR), Address 0x1D//001F // PHY Control Frames Configuration Register (PCFCR), Address 0x1F////0013 0001 // Page1//001E // Page1, Signal Detect Configuration (SD\_CNFG), Address 0x1E////0013 0002 // Page2//0014 // Page2, 100 Mb Length Detect Register (LEN100\_DET), Address 0x14//0015 // Page2, 100 Mb Frequency Offset Indication Register (FREQ100), Address 0x15//0016 // Page2, TDR Control Register (TDR\_CTRL), Address 0x16//0017 // Page2, TDR Window Register (TDR\_WIN), Address 0x17 ★//0018 // Page2, TDR Peak Register (TDR\_PEAK), Address 0x18//0019 // Page2, TDR Threshold Register (TDR\_THR), Address 0x19//001A // Page2, Variance Control Register (VAR\_CTRL), Address 0x1A//001B // Page2, Variance Data Register (VAR\_DATA), Address 0x1B//001D // Page2, Link Quality Monitor Register (LQMR), Address 0x1D//001E // Page2, Link Quality Data Register (LQDR), Address 0x1E//001F // Page2, Link Quality Monitor Register 2 (LQMR2), Address 0x1F////0013 0004 // Page4//0014 // Page4, PTP Control Register (PTP\_CTL), Address 0x14//0015 // Page4, PTP Time Data Register (PTP\_TDR), Address 0x15//0016 // Page4, PTP Status Register (PTP\_STS), Address 0x16//0017 // Page4, PTP Trigger Status Register (PTP\_TSTS), Address 0x17//0018 // Page4, PTP Rate Low Register (PTP\_RATEL), Address 0x18//0019 // Page4, PTP Rate High Register (PTP\_RATEH), Address 0x19//001A // Page4, PTP Read Checksum (PTP\_RDCKSUM), Address 0x1A//001B // Page4, PTP Write Checksum (PTP\_WRCKSUM), Address 0x1B//001C // Page4, PTP Transmit Timestamp Register (PTP\_TXTS), Address 0x1C//001D // Page4, PTP Receive Timestamp Register (PTP\_RXTS), Address 0x1D//001E // Page4, PTP Event Status Register (PTP\_ESTS), Address 0x1E//001F // Page4, PTP Event Data Register (PTP\_EDATA), Address 0x1F//001F // Page4, Extend, PTP Event Data Register (PTP\_EDATA), Address 0x1F////0013 0005 // Page5//0014 // Page5, PTP Trigger Configuration Register (PTP\_TRIG), Address 0x14//0015 // Page5, PTP Event Configuration Register (PTP\_EVNT), Address 0x15//0016 // Page5, PTP Transmit Configuration Register 0 (PTP\_TXCFG0), Address 0x16//0017 // Page5, PTP Transmit Configuration Register 1 (PTP\_TXCFG1), Address 0x17//0018 // Page5, PHY Status Frame Configuration Register 0 (PSF\_CFG0), Address 0x18//0019 // Page5, PTP Receive Configuration Register 0 (PTP\_RXCFG0), Address 0x19//001A // Page5, PTP Receive Configuration Register 1 (PTP\_RXCFG1), Address 0x1A//001B // Page5, PTP Receive Configuration Register 2 (PTP\_RXCFG2), Address 0x1B//001C // Page5, PTP Receive Configuration Register 3 (PTP\_RXCFG3), Address 0x1C//001D // Page5, PTP Receive Configuration Register 4 (PTP\_RXCFG4), Address 0x1D//001E // Page5, PTP Temporary Rate Duration Low Register (PTP\_TRDL), Address 0x1E//001F // Page5, PTP Temporary Rate Duration High Register (PTP\_TRDH), Address 0x1F////0013 0006 // Page6//0014 // Page6, PTP Clock Output Control Register (PTP\_COC), Address 0x14//0015 // Page6, PHY Status Frame Configuration Register 1 (PSF\_CFG1), Address 0x15//0016 // Page6, PHY Status Frame Configuration Register 2 (PSF\_CFG2), Address 0x16//0017 // Page6, PHY Status Frame Configuration Register 3 (PSF\_CFG3), Address 0x17//0018 // Page6, PHY Status Frame Configuration Register 4 (PTP\_PKTSTS4), Address 0x18//0019 // Page6, PTP SFD Configuration Register (PTP\_SFDCFG), Address 0x19//0019 0034 // Page6, PTP SFD Configuration Register (PTP\_SFDCFG), Address 0x19//0019 // Page6, PTP SFD Configuration Register (PTP\_SFDCFG), Address 0x19//001A // Page6, PTP Interrupt Control Register (PTP\_INTCTL), Address 0x1A//001B // Page6, PTP Clock Source Register (PTP\_CLKSRC), Address 0x1B//001C // Page6, PTP Ethernet Type Register (PTP\_ETR), Address 0x1C//001D // Page6, PTP Offset Register (PTP\_OFF), Address 0x1D//001E // Page6, PTP GPIO Monitor Register (PTP\_GPIOMON), Address 0x1E//001F // Page6, PTP Receive Hash Register (PTP\_RXHASH), Address 0x1F//////0013 0004 // Page4////0017 // PTP Trigger Status Register (PTP\_TSTS), Address 0x17////001E // PTP Event Status Register (PTP\_ESTS), Address 0x1E////001F // PTP Event Data Register (PTP\_EDATA), Address 0x1F////0013 0006 // Page4////001D // PTP Offset Register (PTP\_OFF), Address 0x1D////001E // PTP GPIO Monitor Register (PTP\_GPIOMON), Address 0x1Eend