We're using the "DP83822" of Ethernet chip and use the 1.8V external power(LDO Regulator) to the center tap of the Ethernet chip in our design.

But we have the LDO REGULATOR(1.8V) damage Issue from our field.

We can't apply the internal power source to the center tap of the Ethernet chip in our design.

I'd like to know why can't use the external power to center tap in Ethernet chip?

If we use the 1.8V external power to the center tap, what kind of risk is it?

If you have the internal circuit or detail block diagram, Could you share it?

Is the internal structure as below?

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6055408&tag=1

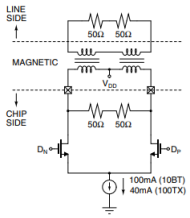

Fig. 1. Conventional open-drain IDAC line driver architecture.

Below is datasheet of "DP83822" regarding the Center tap power.

https://www.ti.com/lit/ds/symlink/dp83822i.pdf?ts=1602579516293&ref_url=https%253A%252F%252Fwww.ti.com%252Fsitesearch%252Fdocs%252Funiversalsearch.tsp%253FsearchTerm%253DDP83822I

Datasheet page 92

Center tap of the transformer must be connected to analog supply rail (AVD) with decoupling capacitors close to the transformer. All resistors and capacitors should be placed as close to the device as possible.

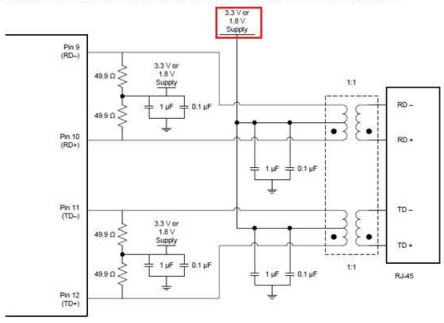

Figure 33. TPI Network Circuit

9.2.1.1 Design Requirements

The design requirements for the DP83822 in TPI operation (100BASE-TX or 10BASE-Te) are:

1. AVD Suppy = 3.3 V or 1.8 V
2. Center Tap Supply = AVD Supply