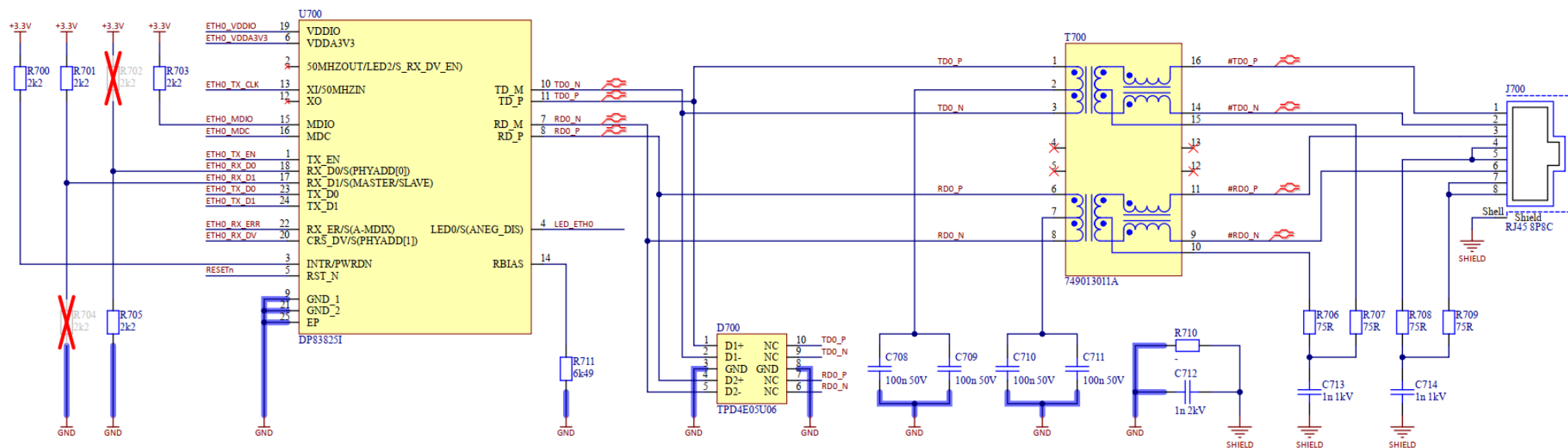
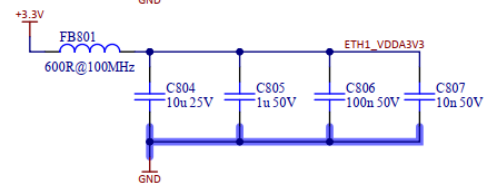


Clock shall be available at Power Ramp, else additional Reset is needed Datasheet p.11 - 6.7 Timing Diagrams

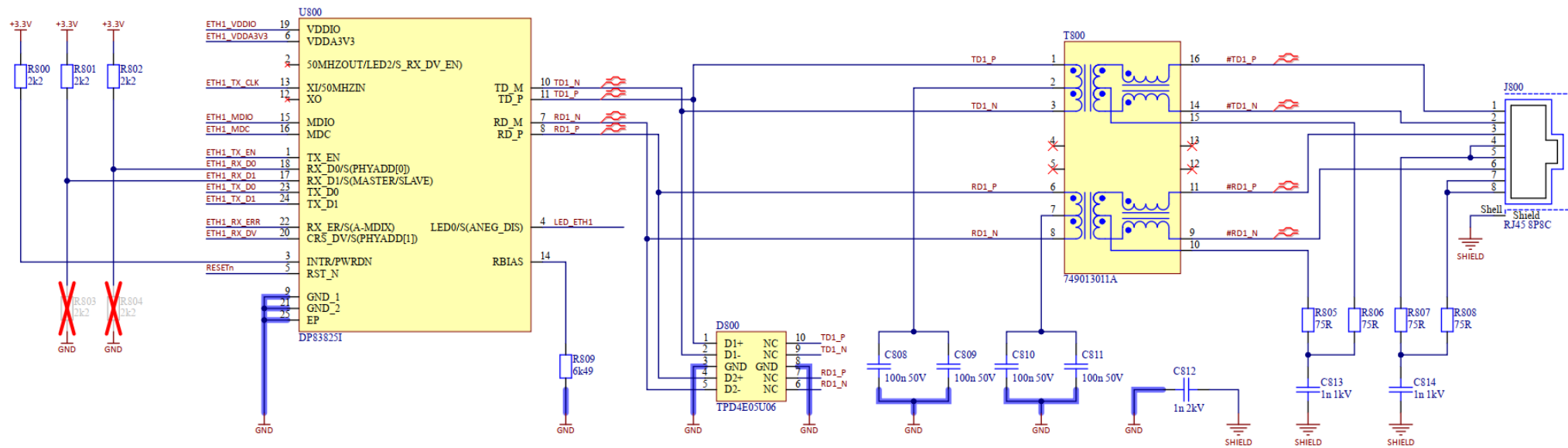




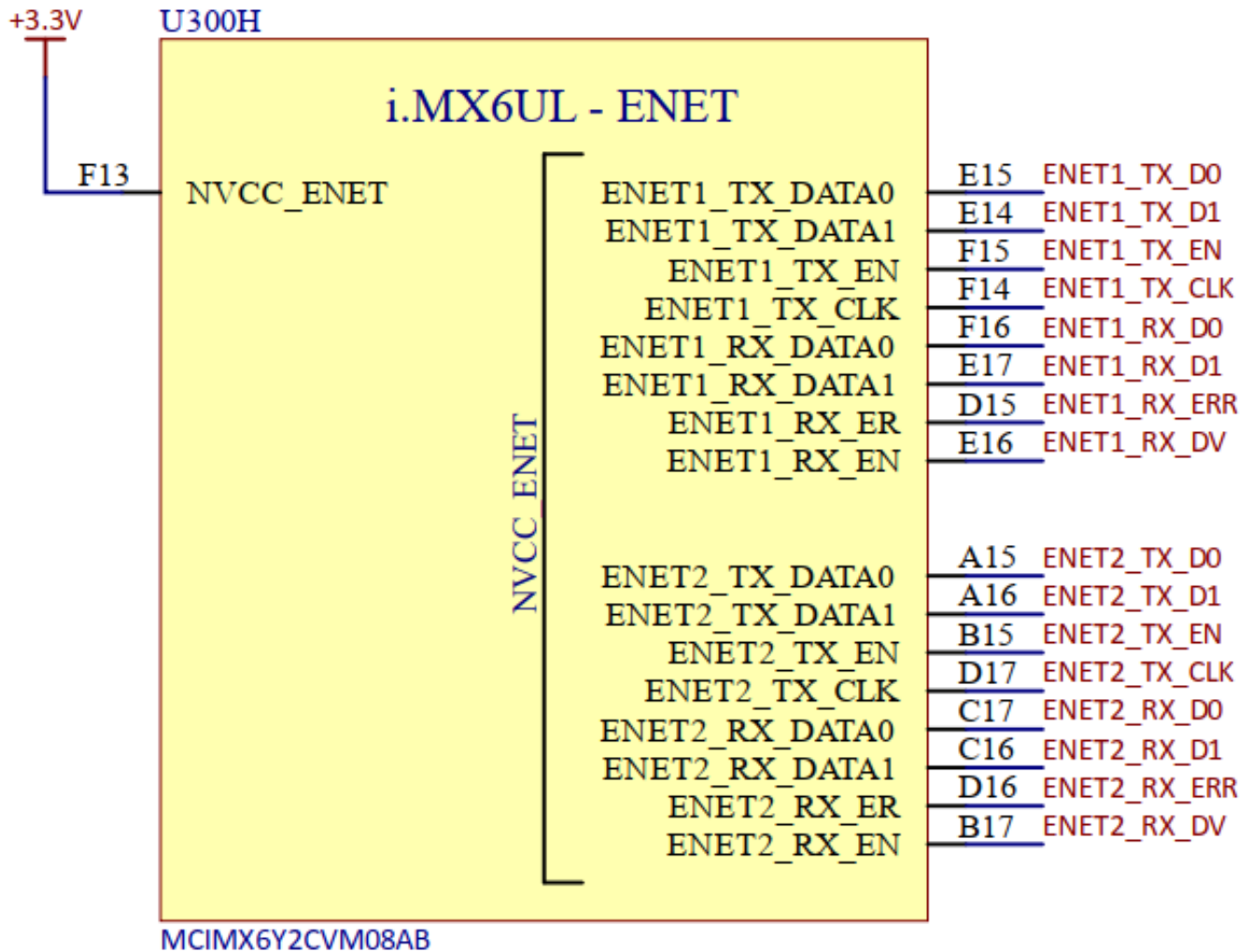
Integrated Termination Resistor

Nur Bootstrap für PHYADD -  
restliche werden per SW gesetzt

CLOCK Input gemäss i.MX6ULL  
Referenzdesign



ENET1\_TX\_CLK & ENET2\_TX\_CLK  
-> 50MHZ REF\_CLK



Decoupling Capacitor  
ENET

