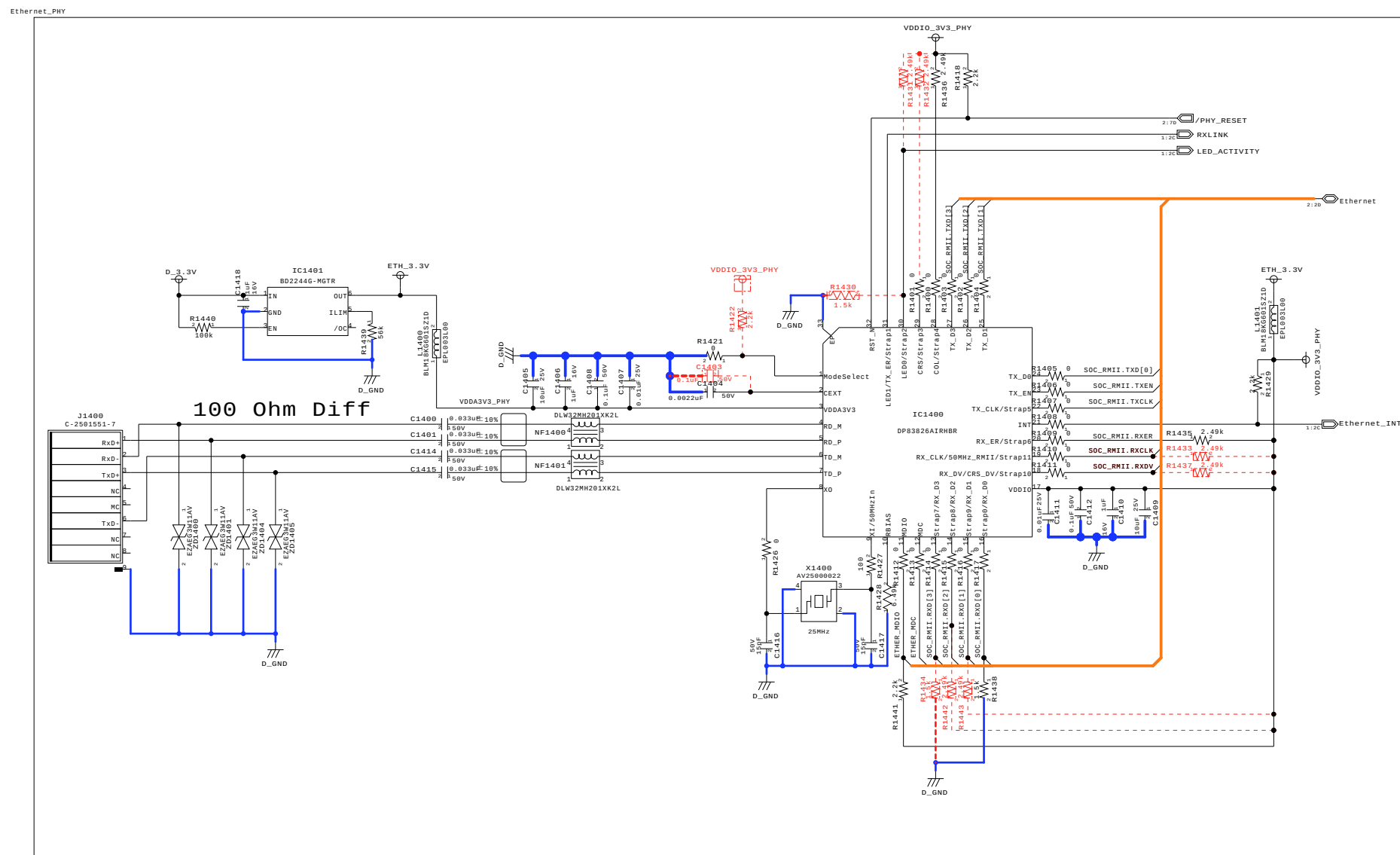




```

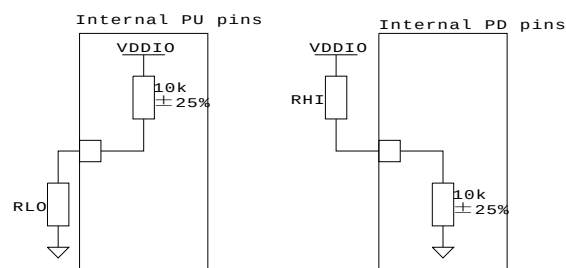
ModeSelect : Basic
Enhanced : VDD
★ Basic : GND
=====
PHY Addr = 0x1 (Default)
PHY Address:(1.5k --> GND)(2.49K--> VCC)
ADD[210] RX_D1 RX_D2 RX_D3
000(0X0) OPEN OPEN 1.5K
★ 001(0X1) OPEN OPEN OPEN <- Default
010(0X2) OPEN 2.49K 1.5K
011(0X3) OPEN 2.49K OPEN
100(0X4) 2.49K OPEN 1.5K
101(0X5) 2.49K OPEN OPEN
110(0X6) 2.49K 2.49K 1.5K
111(0X7) 2.49K 2.49K OPEN
=====
AUTO: Auto Negotiation
LED0(Internal PU)
0 1.5K Auto Negotiation Disable
★ 1 OPEN Auto Negotiation Enable <- Default
=====
MAC INTERFACE MODE: RMII (Default)
ADD[10] RX_DV COL
00 OPEN OPEN MII MAC Mode <- Default
★ 01 OPEN 2.49K RMII Leader Mode
10 2.49K OPEN RESERVED
11 2.49K 2.49K RMII Follower Mode
=====
SPEED:10Mbps
LED1 / TX_ER
0 1.5K 10Mbps
★ 1 OPEN 100Mbps <- Default
=====
DUPLEX:Half Duplex
RX_D0
★ 0 1.5K Full Duplex
1 OPEN Half Duplex <- Default
=====
MII ISOLATE:Enable MII Isolate
RX_ER
0 OPEN Disable MII Isolate <- Default
★ 1 2.49K Enable MII Isolate

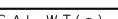
```

2-Level Strap Resistor Ratios

Mode	SUGGESTED RESISTORS	
	RHI (k Ω)	RLO (k Ω)
INTERNAL 10k Ω PULLDOWN (PD) PINS		
0-DEFAULT	OPEN	OPEN
1	2.49	OPEN
INTERNAL 10k Ω PULLUP (PU) PINS		
0	OPEN	1.5
1-DEFAULT	OPEN	OPEN

PIN		TYPE
NAME	NO.	
RX_D3	13	PU
RX_D2	14	PD
RX_D1	15	PD
COL	28	PD
RX_DV	18	PD
LED0	30	PU
LED1/ TX_ER	31	PU
RX_D0	16	PU
RX_ER	20	PD



			DWG	王靖坤	261006	CAL WT(g)	MATERIAL	NAME	
			DSGN	王靖坤	261006			CIRCUIT DIAGRAM	
			CHK	文迪穩	261006			ACT WT(g)	FINISH
SYM	DATE	REVISION		李涛鳴	261006	/AH-A0441-AA-CA-15/25			
MODEL		DATE	APPR				SCALE		FREE
P0-00MHO-0		261006					UNIT		mm
faurecia clarion ELECTRONICS									