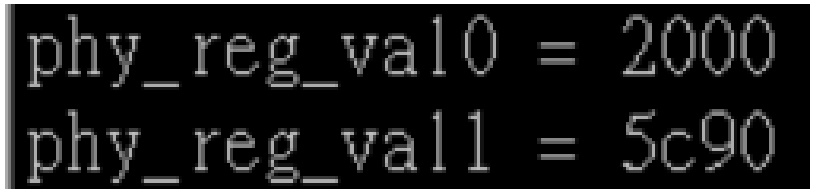
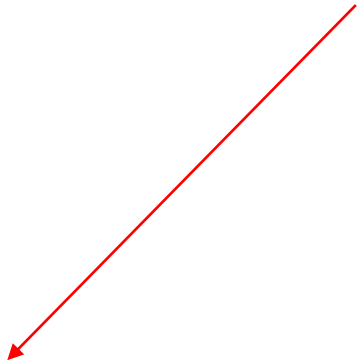
DP83848Q-Q1 address issue

- Read PHY identifier register #2 (address 0x03h) = 5c90 , but datasheet show =5Ca2 .





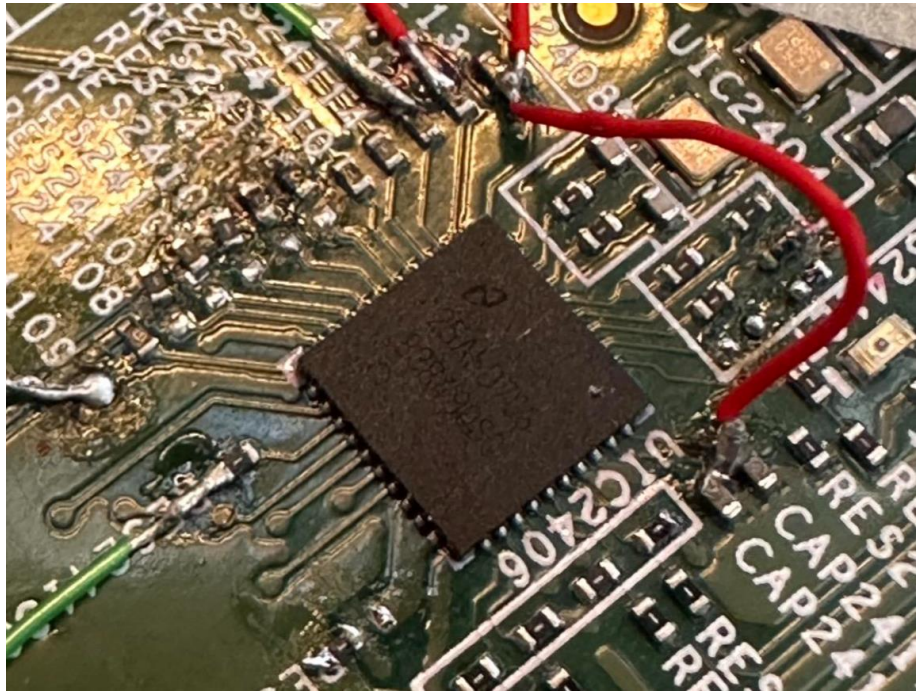
5.6.1.4 PHY Identifier Register #2 (PHYIDR2)

Table 5-12. PHY Identifier Register #2 (PHYIDR2), address 0x03h

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	<0101 11>, RO/P	**OUI Least Significant Bits:** Bits 19 to 24 of the OUI (080017h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	<00 1010>, RO/P	**Vendor Model Number:** The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	<0010>, RO/P	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

IC Top marking Confirm

- Check IC top marking is DP83848QSQ . In the DP83848Q-Q1 series PN.



- Back to check the register value 5C90 read the relative PN is DP83848-EP , not Automotive grade part

5.6.1.4 PHY Identifier Register #2 (PHYIDR2)

Table 5-12. PHY Identifier Register #2 (PHYIDR2), Address 0x03

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	<0101 11>, RO/P	OUI Least Significant Bits: Bits 19 to 24 of the OUI (080017h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	<00 1001 >, RO/P	Vendor Model Number: The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	<0000>, RO/P	Model Revision Number: Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.