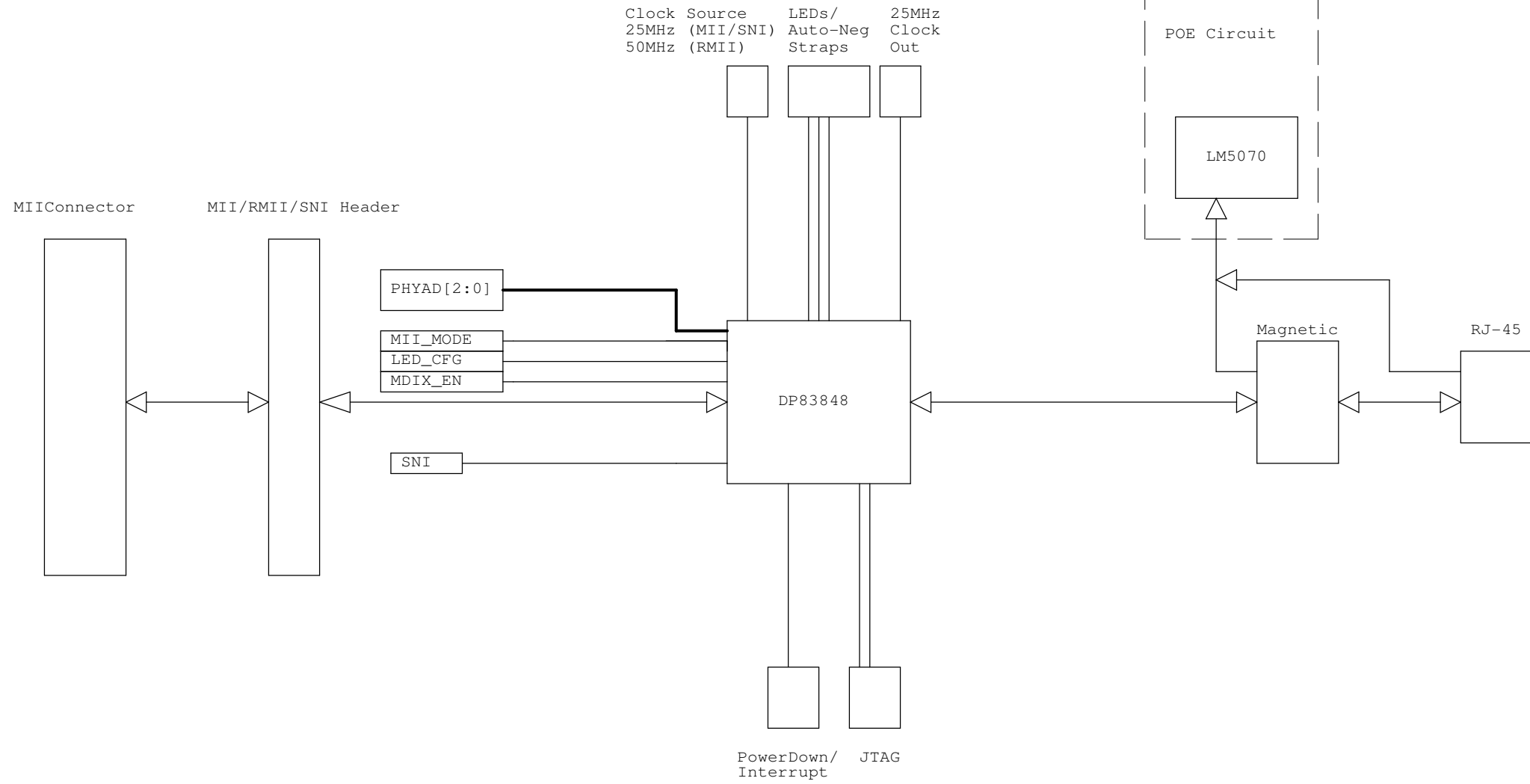
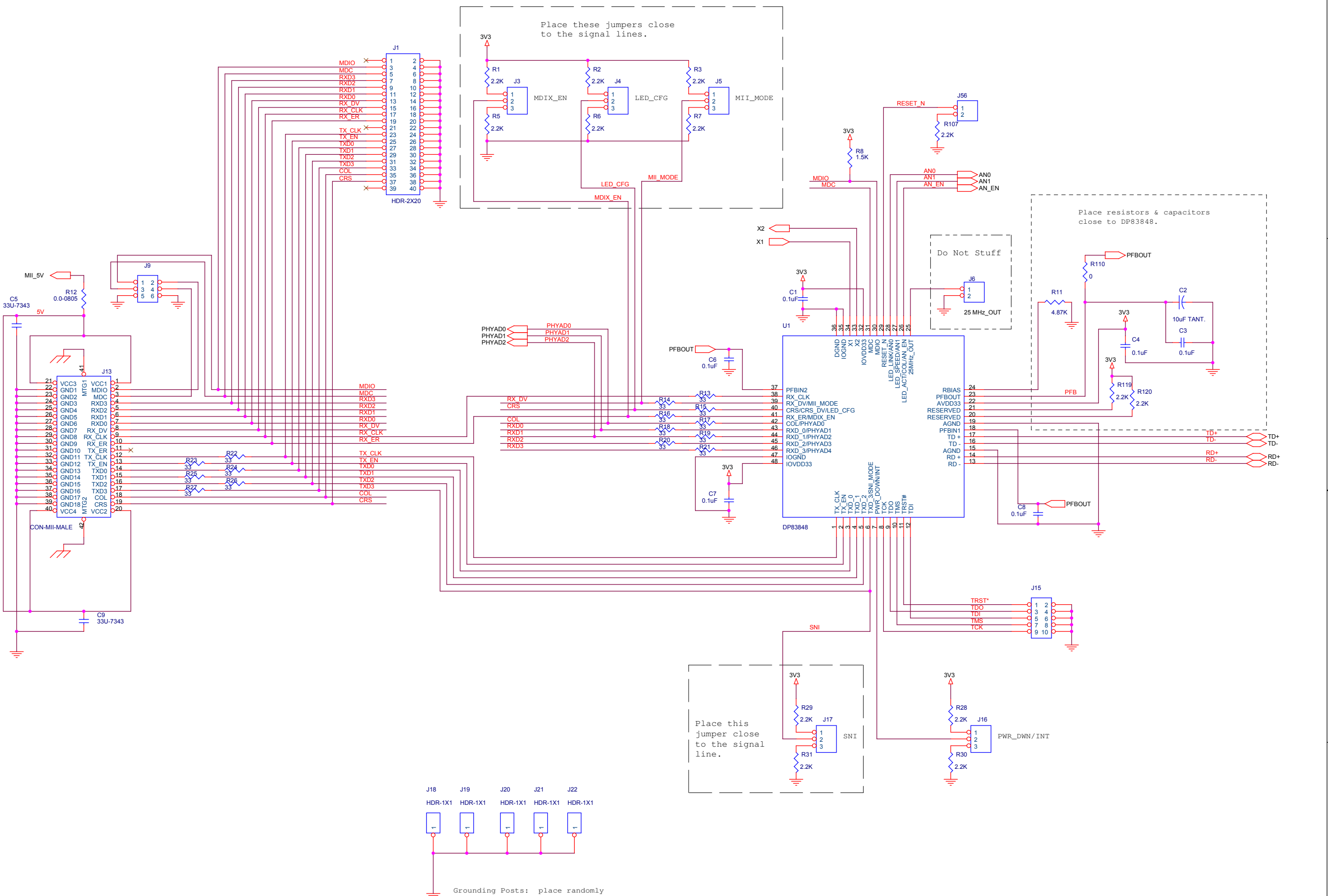


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Revisions note:
 Rev A: Initial release.
 Rev A2:
 - Replaced L2 with R121.
 - Replaced C11 and C15 with 33 pF.
 - Added note for EMI related on TP_IF page.



Title		
DP83848 AspenPhy Demo II - Cover		
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Place these jumpers close to the signal lines.

Place resistors & capacitors close to DP83848.

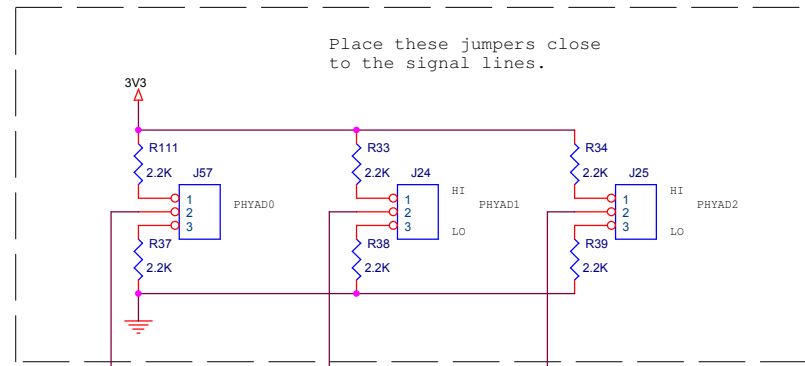
Do Not Stuff

Place this jumper close to the signal line.

J18 HDR-1X1
 J19 HDR-1X1
 J20 HDR-1X1
 J21 HDR-1X1
 J22 HDR-1X1

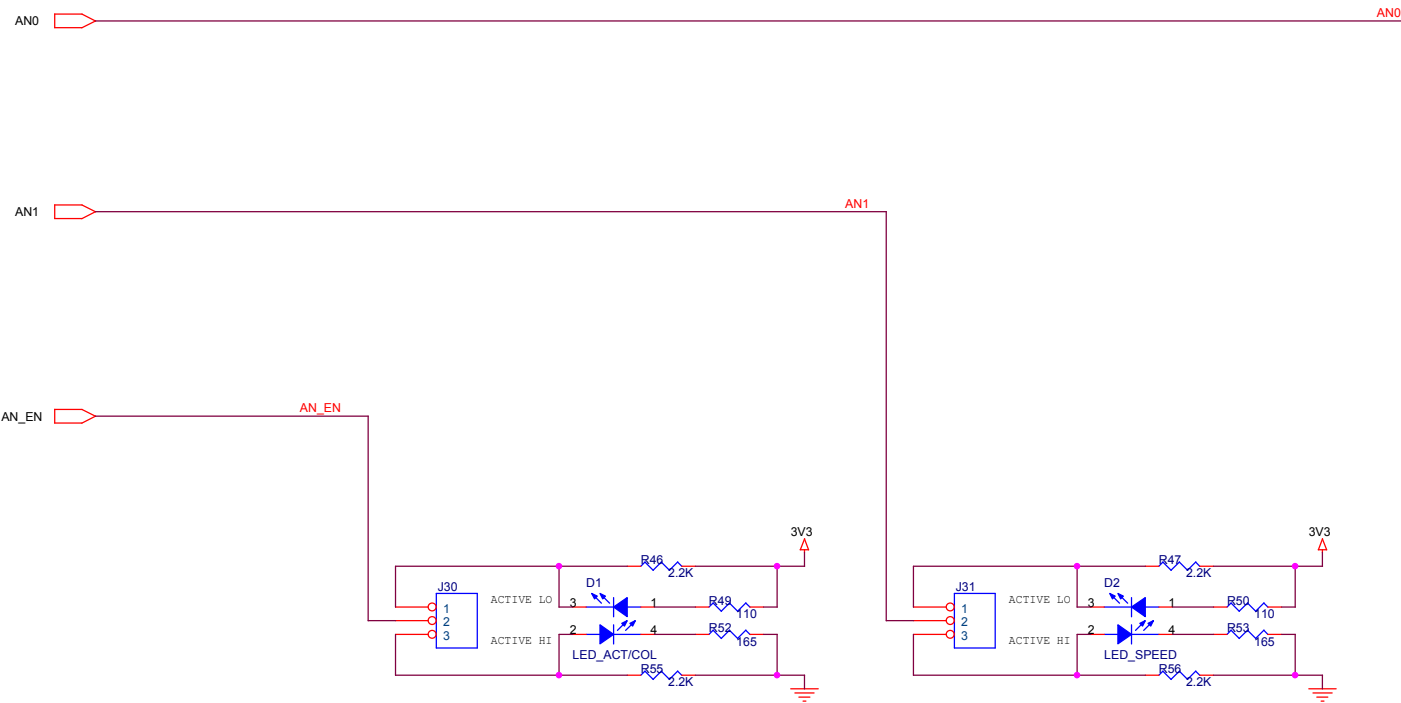
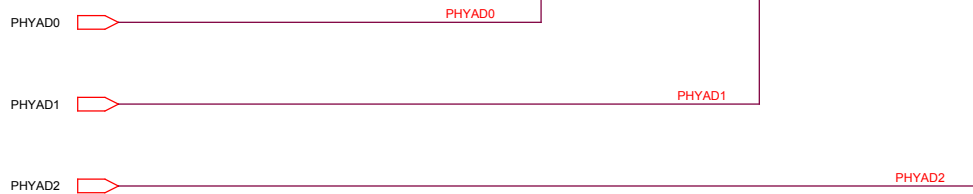
Grounding Posts: place randomly around board

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DP83848 AspenPhy Demo II - Ethernet Phy Page		
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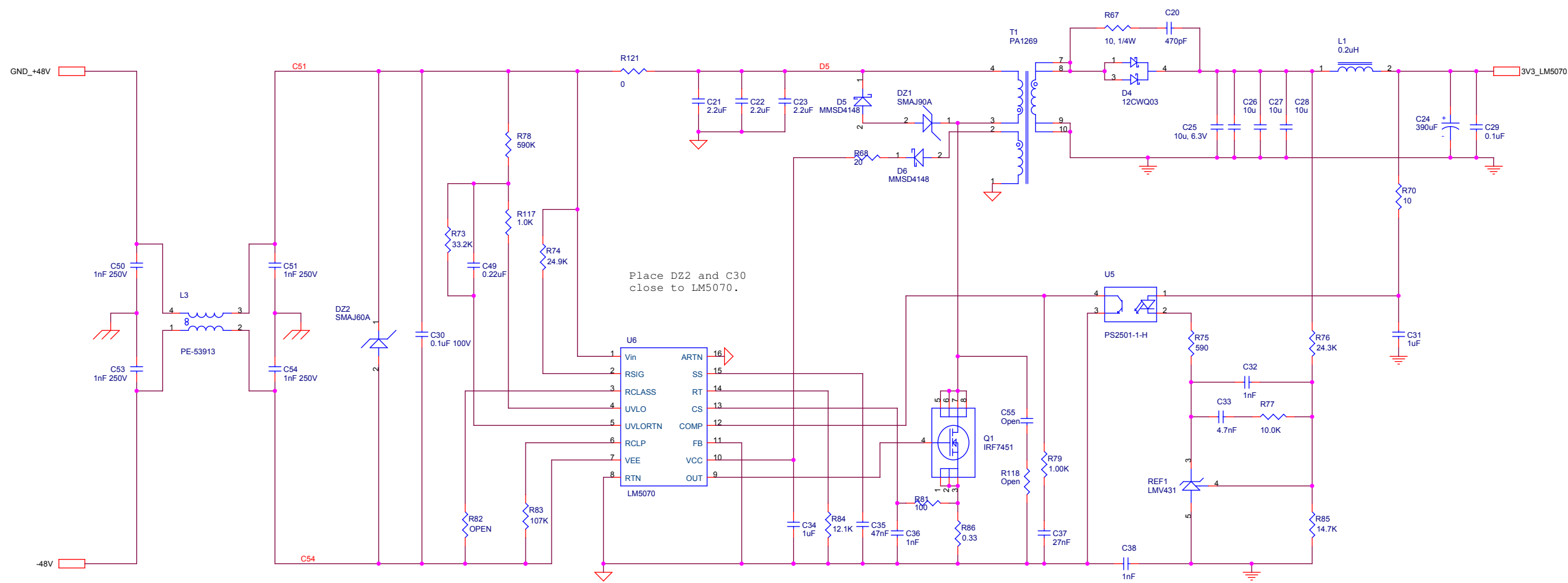
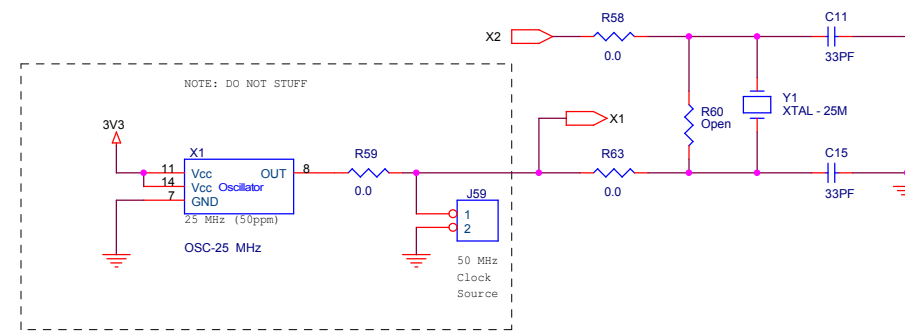
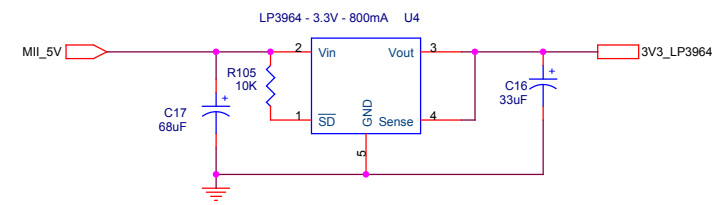
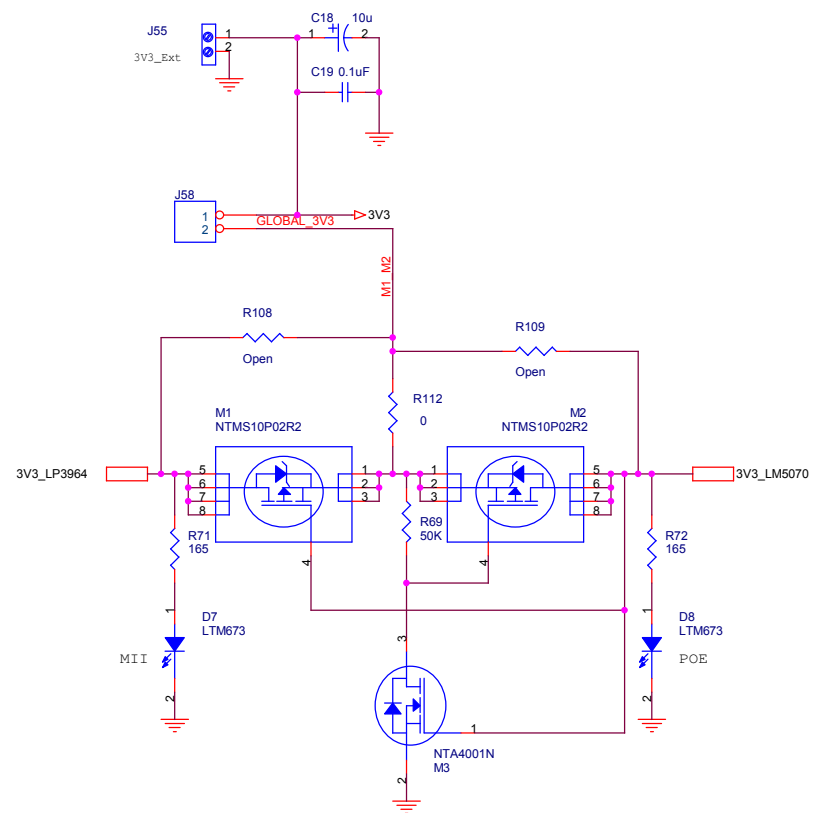
Phy Address Straps: Default is PHYAD0 = 1

J24	J25	Address
0	0	1
1	0	3
1	1	7
etc.		



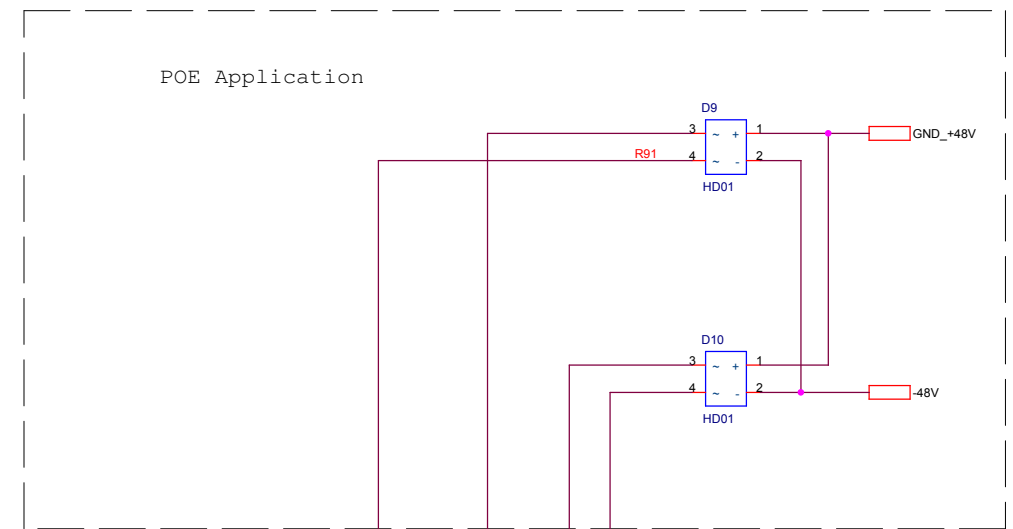
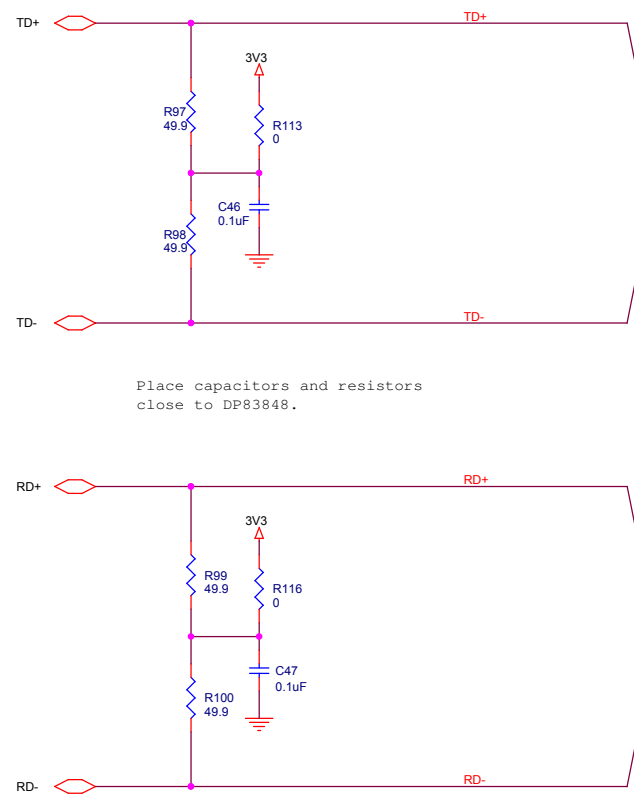
Auto-Negotiation Straps

AN0	AN1	AN_EN	Description
0	0	0	10Mbps HD Force
1	0	0	10Mbps FD Force
0	1	0	100Mbps HD Force
1	1	0	100Mbps FD Force
0	0	1	10Mbps H/FD Advertised
1	0	1	100Mbps H/FD Advertised
0	1	1	10/100Mbps HD Advertised
1	1	1	10/100Mbps H/FD Advertised (default)



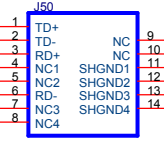
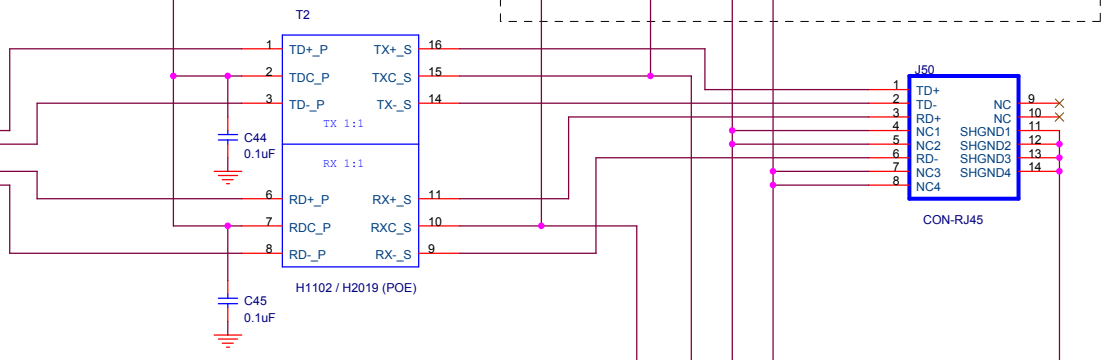
Note: Void Power and Ground planes underneath the POE circuit.

Title		
DP83848 AspenPhy Demo II - Power & Clock		
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Place jumpers, capacitors close to the transformer center taps.

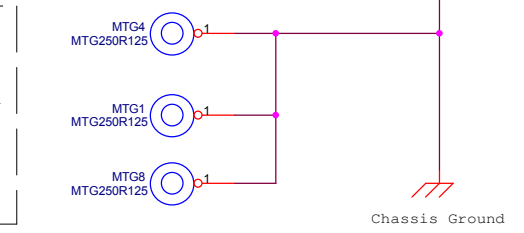
Place these resistors close to TXC_S, RXC_S, NC1- NC4 traces. Do Not Stuff.



Note: Void Power and Ground planes underneath the transformer.

Remove R101-R104 when R91-R94 (0 ohm values) are used.

Note for further improvement on EMI:
 - Allow only 1 mounting point connects to chassis ground.
 - Add two capacitive coupling networks between chassis and common ground. Coupling consists of two caps, .1 uF and .001 uF. Place this on either side of RJ-45.
 - See rev B for the implementation.



Title		
DP83848 AspenPhy Demo II - TP_IF		
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