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We follow up TI DP83867 reference design ，the processor is Xilinx ZU7E, but we had met a problem.



Strap sets as:(NC= No connect)



 RGMII layout total lengths：

RX\_CLK:8590.13mil

RX\_D0 :8595.40mil

RX\_D1 :8592.55mil

RX\_D2 :8589.35mil

RX\_D3 :8604.09mil

 TX\_CLK:7276.74mil

TX\_D0 :7267.87mil

TX\_D1 :7262.87mil

TX\_D2 :7275.74mil

TX\_D3 :7264.74mil

BoardMaterial：TU872，14layers；

the scope of MDI like this:



but reference  design MDI output like this:



Please look that the output wave of MDI/X is totally opposite. Then the RGMII link is failed. We sets mirror, but it seems to unuseful.so how we can solve this problem. Thanks?