



- ##011 Layout
- Trace routing between the PHY and the Switch/MAC should have a controlled characteristic impedance of 50 Ohm (28 to 48 G).
 - Trace length should be matched to a tolerance of 0.3 mm to keep the skew between signals less than 0.37
 - The receiver and transmit signals should be kept away from each other and other signals and clock signals to reduce crosstalk.
- ##012 Layout Guidelines
- All SMD1 connections must be AC-coupled through an 0.1-µF capacitor. Device capacitors must be 0.1-µF and the size should be 0922 or smaller.
 - SMD1 signals are not differential signals.
 - Trace width should be 12 to 15 µm.
 - Show matching within a pair must be less than 0.2 µm, which correlates to 30 mil for standard P94.
 - There is no requirement to match the TR pair for the SMD1.
 - SMD1 signals must be routed on the same layer.
 - Pairs must be referenced to parallel ground planes.
 - When operating in 4-wire mode, the 80 pair must match the clock pair to within 1 µm, which correlates to 30 mil for standard P94.

