1. 问题需求

当使用 DP83867ISRGZ 芯片时，出现了如下所示的异常波形。我们初步判断的原因是由于该芯片引脚驱动能力的不足。目前我们有如下两个问题：

1. 在查阅该芯片的数据手册时，看到了下面这个寄存器的描述，该寄存器可以调整内部，是否可以通过调整阻抗来增大驱动能力。

表 7-114. I/O Configuration (IO_MUX_CFG), Address 0x0170 （续）

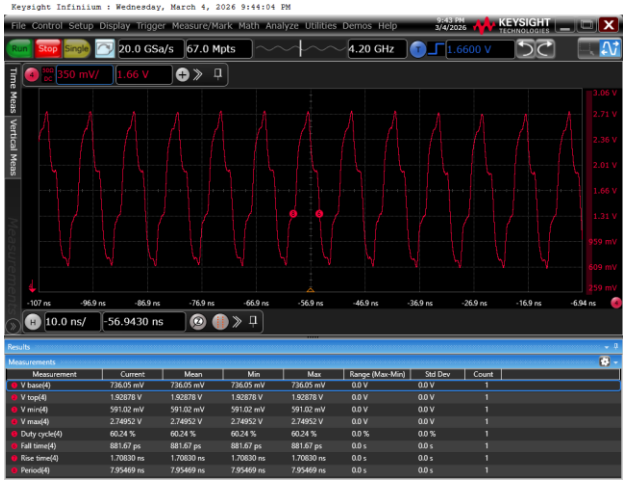
BIT	BIT NAME	DEFAULT	DESCRIPTION
12:8	CLK_O_SEL	0 1100, RW	Clock Output Select: 01101 - 11111: RESERVED 01100: Reference clock (synchronous to XI input clock) 01011: Channel D transmit clock 01010: Channel C transmit clock 01001: Channel B transmit clock 01000: Channel A transmit clock 00111: Channel D receive clock divided by 5 00110: Channel C receive clock divided by 5 00101: Channel B receive clock divided by 5 00100: Channel A receive clock divided by 5 00011: Channel D receive clock 00010: Channel C receive clock 00001: Channel B receive clock 00000: Channel A receive clock
7	RESERVED	0, RO	RESERVED
6	CLK_O_DISABLE	0 , RW	Clock Output Disable: 1 = Disable clock output on CLK_OUT pin. 0 = Enable clock output on CLK_OUT pin.
5	RESERVED	0, RO	RESERVED
4:0	IO_IMPEDANCE_CTRL	TRIM, RW	Impedance Control for MAC I/Os: Output impedance approximate range from 35-70Ω in 32 steps. Lowest being 11111 and highest being 00000. Range and Step size will vary with process. Default is set to 50Ω by trim. But the default register value can vary by process. Non default values of MAC I/O impedance can be used based on trace impedance. Mismatch between device and trace impedance can cause voltage overshoot and undershoot.

2. 面对下图的异常波形是否有其余解决办法？是否有别的寄存器来调整？

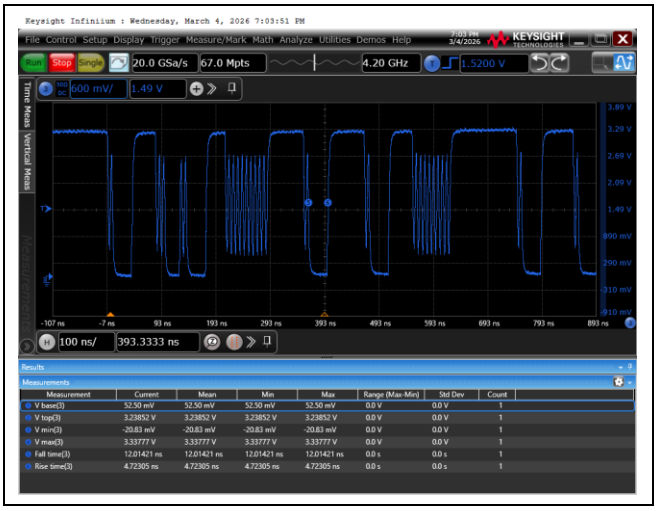
2. RGMII 信号测试

2.1 U13(DP83867ISRGZ)测试图片

RGMII_RXC



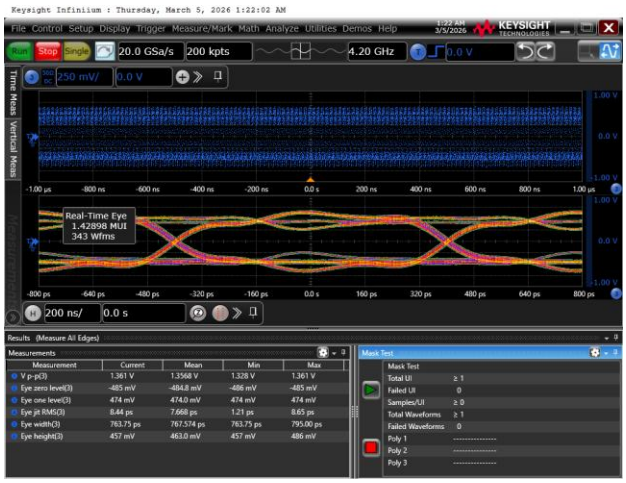
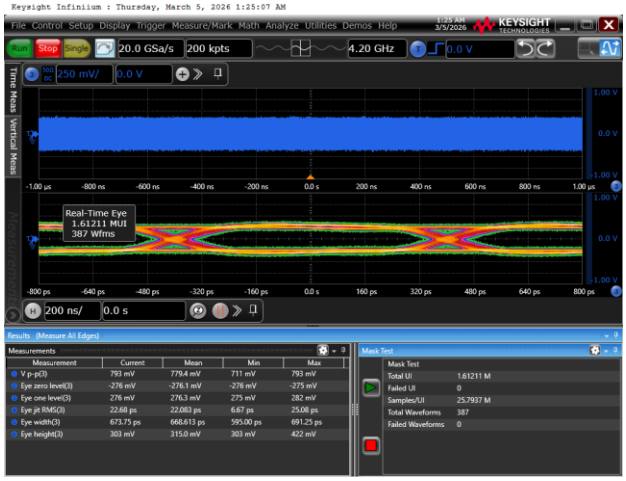
RGMII_RD3



由上图所示，引脚的驱动能力不足。想咨询一下该芯片是否有寄存器可以增加引脚驱动能力。

3. SGMII 信号测试

3.1 U13(DP83867ISRGZ)测试图片

Master	
	
Slave	
	

由上图所示，引脚的驱动能力不足。想咨询一下该芯片是否有寄存器可以增加引脚驱动能力。