

### 3.4 Unstable Link Up Debug in 1Gbps communication

If repeating link up and link down between Dp83867 and another Link Partner behavior occur, please follow this session for debug:

1. Write register 0x001F to 4000 (software reset) and see if you are able to link up.
2. Check if DP83867 is able to link up with another TI giga-bit PHY.
3. Check the [Schematic and Layout Checklist session](#) to make sure the board design follow the recommendation.
4. Read register 0x0013 bit[12] and register 0x0011 bit[12]. If both registers indicate page received in 1Gbps communication. Write register 0x01D5 = F508 to change DP83867PHY from low power mode to normal operational mode.

```
begin
// Check page recieved in 1Gbps communication
0012
0013
// changing from lower power mode to normal operational mode
01D5 F508
end
```

I cannot read "low power mode" and "normal operational mode" from Register 0x01D5

#### 7.6.130 Programmable Gain Register (PROG\_GAIN)

Table 7-140. Programmable Gain (PROG\_GAIN), Address 0x01D5

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	1111 0101 0000, RW	RESERVED
3	UNF_FUNC_MODE	0, RW	For Force Mode Only 1 = Sets required swing level for compliance testing. 0 = Normal operation.
2	RESERVED	0, RW	RESERVED
1	SGMII_TX_POL_IN	0, RW	SGMII TX Bus Polarity Invert 1 = Invert Polarity 0 = Normal Polarity
0	SGMII_RX_POL_IN	0, RW	SGMII RX Bus Polarity Invert 1 = Invert Polarity 0 = Normal Polarity