Schematic Review Form

DS100MB203 Review for Lisa Xu

Pin #	Name	Info	Violations	*Description*
10,11,15,16	D_IN0+, D_IN0-, D_IN1+, D_IN1-	looks good		Inverting and noninverting CML differential inputs to the equalizer. A gated on-chip 50-Ω termination resistor connects D_INn+ to VDD and D_INn– to VDD when enabled. AC coupling required on high-speed I/O.
3,4,7,8	D_OUT0+, D_OUT0-, D_OUT1+, D_OUT1-	looks good		Inverting and noninverting low power differential signaling 50-Ω outputs with deemphasis. Fully compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O.
45,44,40,39	S_INA0+, S_INA0-, S_INA1+, S_INA1-	looks good		Inverting and noninverting CML differential inputs to the equalizer. An on-chip 50-Ω termination resistor connects S_INAn+ to VDD and S_INAn– to VDD. AC coupling required on high-speed I/O.
43,42,38,37	S_INB0+, S_INB0-, S_INB1+, S_INB1-	looks good		Inverting and noninverting CML differential inputs to the equalizer. An on-chip 50-Ω termination resistor connects S_INBn+ to VDD and S_INBn– to VDD. AC coupling required on high-speed I/O.
35,34,31,30	S_OUTA0+, S_OUTA0-, S_OUTA1+, S_OUTA1-	looks good		Inverting and noninverting low power differential signaling 50-Ω outputs with deemphasis. Fully compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O.
33,32,29,28	S_OUTB0+, S_OUTB0-, S_OUTB1+, S_OUTB1-	looks good		Inverting and noninverting low power differential signaling 50-Ω outputs with deemphasis. Fully compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O.
48	ENSMB	looks good, HW strap or CPLD control are both sufficient to set ENSMB on the fly. HW strap shown sets SMBus slave mode.		System Management Bus (SMBus) enable pin Tie 1 kΩ to VDD = register access SMBus slave mode FLOAT = Read external EEPROM (master SMBUS mode) Tie 1 kΩ to GND = pin mode
52	RESET	looks good, RESET strapped low for normal operation.		0: Normal operation (device is enabled). 1: Low power mode.

25	VDD_SEL	looks good, 3.3V mode selected		Controls the internal regulator FLOAT: 2.5-V mode Tied to GND: 3.3-V mode
DAP	GND	looks good		Ground pad (DAP - die attach pad).
9,14,36,41,51	VDD	looks good		Power supply pins CML/analog 2.5-V mode, connect to 2.5V ±5% 3.3-V mode, connect 0.1-µF cap to each VDD pin
24	VIN	looks good		In 3.3-V mode, feed 3.3 V ±10% to VIN In 2.5-V mode, leave floating.
50	SCL	looks good, 1k pull-up to 3.3V is sufficient (shown on DEM_S1 net).		ENSMB master or slave mode SMBUS clock input pin is enabled (slave mode) SMBUS clock output when loading configuration from EEPROM (master mode)
49	SDA	looks good, 1k pull-up to 3.3V is sufficient (shown on DEM_S0 net).		ENSMB master or slave mode The SMBus bidirectional SDA pin is enabled. Data input or open-drain (pulldown only) output.
54,53,47,46	AD0-AD3	looks good, SMBus 8-bit address is set to 0xCE (7-bit address is 0x67).		ENSMB Master or Slave mode SMBus slave address inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.
26	READ_EN	N/A for SMBus slave mode or pin mode		ENSMB = FLOAT (SMBUS master mode) When using an external EEPROM, a transition from high to low starts the load from the external EEPROM
21	MODE		MODE pin is pulled high for 10-KR mode. Typically 10GE mode is used for SFP+ applications. I will give a definitive recommendation pending our discussion about use case on E2E.	0: SATA/SAS, PCIe GEN 1/2 and 10GE FLOAT: AUTO (PCIe GEN 1/2 or GEN 3) 1: 10-KR
22	INPUT_EN	looks good, FANOUT disabled, input always enabled with 50-ohm selected. Note that RX Detect feature is not recommended for ethernet applications.		0: Normal operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 Ω. 20 kΩ to GND: Reserved FLOAT: AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable 1: Normal operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 Ω.

23	SEL0	looks good, CPLD controls input/output mapping.		Select pin for lane 0. 0: selects input S_INB0±, output S_OUTB0±. 20 kΩ to GND: Selects input S_INB0±, output S_OUTA0±. FLOAT: selects input S_INA0±, output S_OUTB0±. 1: Selects input S_INA0±, output S_OUTA0±.
26	SEL1	looks good, CPLD controls input/output mapping.		Select pin for lane 1. 0: Selects input S_INB1±, output S_OUTB1±. 20 kΩ to GND: Selects input S_INB1±, output S_OUTA1±. FLOAT: Selects input S_INA1±, output S_OUTB1±. 1: Selects input S_INA1±, output S_OUTA1±.
27	ALL_DONE		ALL_DONE is an output pin and does not need to be pulled high. Additionally, ALL_DONE is N/A in SMBus slave mode and pin mode and can be left floating.	Valid register load status output 0: External EEPROM load passed 1: External EEPROM load failed
20,19,46,47	EQ_D0, EQ_D1, EQ_S0, EQ_S1	looks good. D side and S side EQ set to max setting (33.8dB @ 5 GHz). If you choose to use pin mode, some tuning may be required on the EQ setting.		EQ_D[1:0] and EQ_S[1:0] control the level of equalization on the high-speed input pins. The inputs are organized into two sides. The D side is controlled with the EQ_D[1:0] pins and the S side is controlled with the EQ_S[1:0] pins. See Table 2.
49,50,53,54	DEM_S0, DEM_S1, DEM_D0, DEM_D1	looks good. D side and S side DEM set to max setting (DEM = -9dB, VOD = 1.2 Vp-p). If you choose to use pin mode, some tuning may be required on DEM setting.		DEM_D[1:0] and DEM_S[1:0] control the level of VOD and de-emphasis on the high-speed output. The outputs are organized into two sides. The D side is controlled with the DEM_D[1:0] pins and the S side is controlled with the DEM_S[1:0] pins. See Table 3.

Comments