Schematic Review Form

DS125MB203 Test Board

Pin #	Name	Info	Violations	*Description*
10,11,15,16	D_IN0+, D_IN0-, D_IN1+, D_IN1-	Looks good. F2SFP connected to D_IN0 with AC coupling. D_IN1 left floating.		Inverting and noninverting CML differential inputs to the equalizer. A gated on-chip 50-Ω termination resistor connects D_INn+ to VDD and D_INn– to VDD when enabled. AC coupling required on high-speed I/O.
3,4,7,8	D_OUT0+, D_OUT0-, D_OUT1+, D_OUT1-	Looks good. F2SFP connected to D_OUT0 with AC coupling. D_OUT1 left floating.		Inverting and noninverting low power differential signaling 50-Ω outputs with deemphasis. Fully compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O.
45,44,40,39	S_INA0+, S_INA0-, S_INA1+, S_INA1-	Looks good. RF2SFP connected to S_INA0 with AC coupling. S_INA1 left floating.		Inverting and noninverting CML differential inputs to the equalizer. An on-chip 50-Ω termination resistor connects S_INAn+ to VDD and S_INAn– to VDD. AC coupling required on high-speed I/O.
43,42,38,37	S_INB0+, S_INB0-, S_INB1+, S_INB1-	Looks good. Both S_INB0 and S_INB1 left floating.		Inverting and noninverting CML differential inputs to the equalizer. An on-chip 50-Ω termination resistor connects S_INBn+ to VDD and S_INBn– to VDD. AC coupling required on high-speed I/O.
35,34,31,30	S_OUTA0+, S_OUTA0-, S_OUTA1+, S_OUTA1-	Looks good. RF2SFP connected to S_OUTA0 with AC coupling on board variant 3. S_OUTA0 left floating on board variant 2. S_OUTA1 left floating on both board variants.		Inverting and noninverting low power differential signaling 50-Ω outputs with deemphasis. Fully compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O.
33,32,29,28	S_OUTB0+, S_OUTB0-, S_OUTB1+, S_OUTB1-	Looks good. RF2SFP connected to S_OUTB0 with AC coupling on board variant 2. S_OUTB0 left floating on board variant 3. S_OUTB1 left floating on both board variants.		Inverting and noninverting low power differential signaling 50-Ω outputs with deemphasis. Fully compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O.
48	ENSMB	ENSMB pulled low for pin control mode by default.		System Management Bus (SMBus) enable pin Tie 1 kΩ to VDD = register access SMBus slave mode FLOAT = Read external EEPROM (master SMBUS mode) Tie 1 kΩ to GND = pin mode

52	RESET	Tied low for normal operation.		0: Normal operation (device is enabled). 1: Low power mode.
25	VDD_SEL	Tied low for 3.3V mode.		Controls the internal regulator FLOAT: 2.5-V mode Tied to GND: 3.3-V mode
DAP	GND	Looks good.		Ground pad (DAP - die attach pad).
9,14,36,41,51	VDD		In 3.3V mode, VDD pins should not be connected to any external supply. VDD pins will be supplied 2.5V by internal regulator. TI recommendation is to only connect a 0.1uF decoupling cap per VDD pin.	Power supply pins CML/analog 2.5-V mode, connect to 2.5V ±5% 3.3-V mode, connect 0.1-µF cap to each VDD pin
24	VIN		In 3.3V mode, 3.3V supply should be connected to VIN pin only. TI recommendation is to connect one 10uF and one 1uF decoupling capacitors.	In 3.3-V mode, feed 3.3 V ±10% to VIN In 2.5-V mode, leave floating.
50	SCL		2k pull-up to 3.3V on SCL. I recommend adding a 0 ohm series resistor so the I2C network and pull-up can be disconnected from the pin when using pin control mode.	ENSMB master or slave mode SMBUS clock input pin is enabled (slave mode) SMBUS clock output when loading configuration from EEPROM (master mode)
49	SDA		2k pull-up to 3.3V on SDA. I recommend adding a 0 ohm series resistor so the I2C network and pull-up can be disconnected from the pin when using pin control mode.	ENSMB master or slave mode The SMBus bidirectional SDA pin is enabled. Data input or open-drain (pulldown only) output.
54,53,47,46	AD0-AD3	Pin mode selected by default. Address is configurable via resistor straps when using SMBus slave mode.		ENSMB Master or Slave mode SMBus slave address inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.

26	READ_EN	Left floating. Pin is unused when using pin mode or SMBus slave mode.		ENSMB = FLOAT (SMBUS master mode) When using an external EEPROM, a transition from high to low starts the load from the external EEPROM
21	MODE	Pulled low by default. 10GE mode is selected.		0: SATA/SAS, PCIe GEN 1/2 and 10GE FLOAT: AUTO (PCIe GEN 1/2 or GEN 3) 1: 10-KR
22	INPUT_EN	Pulled high by default. Fanout is enabled. If you wish to disable fanout, pull this pin low.		0: Normal operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 Ω. 20 kΩ to GND: Reserved FLOAT: AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable 1: Normal operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 Ω.
23	SEL0	Left floating to select S_INA0. Fanout enables bout S_OUTA0 and S_OUTB0.		Select pin for lane 0. 0: selects input S_INB0±, output S_OUTB0±. 20 kΩ to GND: Selects input S_INB0±, output S_OUTA0±. FLOAT: selects input S_INA0±, output S_OUTB0±. 1: Selects input S_INA0±, output S_OUTA0±.
26	SEL1	Left floating. Port 1 is unused.		Select pin for lane 1. 0: Selects input S_INB1±, output S_OUTB1±. 20 kΩ to GND: Selects input S_INB1±, output S_OUTA1±. FLOAT: Selects input S_INA1±, output S_OUTB1±. 1: Selects input S_INA1±, output S_OUTA1±.
27	ALL_DONE	Left floating. SMBus master mode is unused.		Valid register load status output 0: External EEPROM load passed 1: External EEPROM load failed
20,19,46,47	EQ_D0, EQ_D1, EQ_S0, EQ_S1		Both pull-up and pull-down resistors are populated. This is not a valid configuration.	EQ_D[1:0] and EQ_S[1:0] control the level of equalization on the high-speed input pins. The inputs are organized into two sides. The D side is controlled with the EQ_D[1:0] pins and the S side is controlled with the EQ_S[1:0] pins. See Table 2.
49,50,53,54	DEM_S0, DEM_S1, DEM_D0, DEM_D1		Both pull-up and pull-down resistors are populated. This is not a valid configuration.	DEM_D[1:0] and DEM_S[1:0] control the level of VOD and de-emphasis on the high-speed output. The outputs are organized into two sides. The D side is controlled with the DEM_D[1:0] pins and the S side is controlled with the DEM_S[1:0] pins. See Table 3.

Comments