DATA BOOK PACKAGE OUTLINE

LEADFRAME EXAMPLE 4218497

DRAFTER:	T. LEQUANG	DATE:	10/08/2013				DIMENSIONS IN I	NS IN MILLIMETERS		
DESIGNER:		DATE:				🐌 Texas Instr	COD N	e identity Iumber		
CHECKER:	K. SINCERBOX & V. PAKU	DATE:	01/05/2017			SEMICONDUCTOR OPP	RATIONS	C	1295	
ENGINEER:	B. TAN	DATE:	01/26/2017	ePOD. RGH0016A / WQFN.						
APPROVED:	E. REY & D. CHIN	DATE:	01/26/2017	16 PIN, 0.5 MM PITCH						
RELEASED:	WDM	DATE:	01/27/2017			,				
TEMPLATE IN	IFO: EDGE# 4218519	DATE:	04/07/2016	SCALE NTS	A	421497	8	B	PAGE 1 OF 5	

RGH0016A



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



RGH0016A

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



 This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



REVISIONS								
REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER				
Α	RELEASE NEW DRAWING	2132285	09/16/2013	C. MANACK / T. LEQUANG				
В	ADD STAND-OFF & COPLANARITY; UPDATE PER CURRENT STANDARDS	2161107	01/27/2017	B. TAN / T. LEQUANG				

SCALE SIZE Δ 4214978 B 5 or 5	_					
		SCALE	size A	4214978	B	page 5 of 5