DS50PCI402 HSPICE Model
User Guide

1. Introduction

The DS50PCI402 is a low power, 4 lane bidirectional buffer/equalizer designed specifically for PCI Express Gen1 and Gen2 applications. The device performs both receive equalization and transmit de-emphasis, allowing maximum flexibility of physical placement within a system. The receiver is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium.

The receiver's continuous time linear equalizer (CTLE) provides a boost up to +26 dB at 2.5 GHz and is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium. The transmitter features a programmable output de-emphasis driver and allows amplitude voltage levels to be selected from 600 mVp-p to over 1200 mVp-p to suit multiple application scenarios. This Low Power Differential Signaling (LPDS) output driver is a power efficient implementation that maintains compatibility with AC coupled CML receiver.

The DS50PCI402 HSPICE model represents a single channel of the DS50PCI402.

This document lists the model kit contents, identifies simulator requirements, explains how to use the model and run a sample HSPICE simulation, overviews available signal conditioning settings and provides some expected results.

2. Model Kit Contents

-DS50PCI402_enc.sp
-example_sim.sp
-prbs.inc
-HSPICE Model User Guide.doc (this document)

The "ds50pci402_enc.sp" is the DS50PCI402 encrypted HSPICE model.

The "example_sim.sp" is an example simulation setup.

The "prbs7.inc" is a PRBS7 pattern generator.

3. Simulator Requirements

It is highly recommended to use HSPICE version 2008.09-SP1 or later for running simulations. In addition, HSPICE requires an "hspice3des" license token. It can be obtained from Synopsys at NO cost to user.

The included HSPICE Model is encrypted using "metaencrypt" utility from 2008.09-SP1 version of HSPICE.

4. Setting Signal Conditioning

The model has 21 logic inputs that can be set to either logic H or L by tying them to VCC or VEE respectively to get the desired setting.

4.1 Equalization

Equalization is controlled by the gst1, gst0, bst2, bst1, and bst0 pins. Theoretically all combinations are allowed, however the table shows the HSPICE channel model equalization gain settings correspondence to the available pin equalization settings.

If the pin equalization gain settings do not meet the needs or your application, please contact your sales contact at National Semiconductor.

External Device Pins (from Datasheet)		Internal Pins accessible in the HSPICE model (in decimal to be converted by user to binary)		
EQ1	EQ0	GST[1:0]	BST[2:0]	AC Gain (dB) 2.5 Ghz
F	F	0	0	0 (Bypass)
1	1	1	2	4.0
0	0	2	0	9.6
F	0	2	2	11.4
1	0	3	1	15.5
F	1	2	5	17.0
0	1	2	7	19.1
0	F	3	3	20.6
1	F	3	5	26.3

Table 1: Equalization Settings

4.2 De-emphasis and VOD control

De-emphasis is controlled by the 8 de_sel<7:0> pins in combination with the 7 vod_sel<6:0> pins and the rate_sel pin. This table does not look exactly like the device datasheet. Settings other then those listed here may not produce the results expected.

Internal Pins accessible in the HSPICE model			
rate_sel	de_sel[7:0]	vod_sel[6:0]	Peak Gain (dB)
0	0000 0001	000 1111	0 (Bypass)
1	0000 0001	000 1111	0 (Bypass)
0	0000 0011	000 1110	3.5
1	0000 0011	000 1110	3.5
0	0000 0101	000 1001	6
1	0000 0101	000 1001	6

Table 2: Compatibility De-Emphasis

Internal Pins accessible in the HSPICE model			
rate_sel	de_sel[7:0]	vod_sel[6:0]	Peak Gain (dB)
0	1000 1000	000 1111	6
1	1000 1000	000 1111	6
0	1001 0000	000 1111	9
1	1001 0000	000 1111	9
0	1010 0000	000 1111	12
1	1010 0000	000 1111	12
0	1001 0000	001 1111	9
1	1001 0000	001 1111	9
0	1010 0000	011 1111	12
1	1010 0000	011 1111	12

Table 3: Enhanced De-Emphasis

Please note that the example_sim.sp is configured for a VOD=1000mV and de-emphasis of 0dB, which is obtained by setting these model control pins:

de_sel[7:0] = 1'd = 00000001'b
vod_sel[6:0] = 15'd = 0001111'b
rate_sel = 0'd = 1'b

5.0 Expected Model Output

With the supplied files and settings, the differential output should have this output pattern.

Blue: DE = OFF
Green: DE = -3.5 dB
Yellow: DE = -6.0 dB