DS90UB933 Power On Sequence Design Key Points

- GPIO2 needs to be pulled low during PDB ramps up. A minimum 40kohms pull-down resistor is recommended.
- Power on sequence should follow TI datasheet strictly including PDB pin resistor and capacitor --- 10kohms and 1uF are recommended.

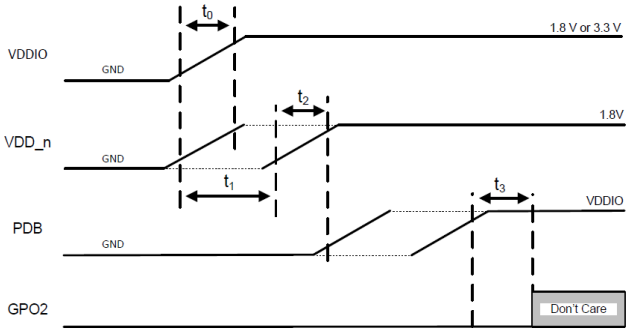

Table 8. Power-Up Sequencing Constraints for DS90UB933-Q1

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	Units
t_0	$V_{(VDDIO)}$ rise time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required	0.05		5	ms
t_1	$V_{(VDDIO)}$ to $V_{(VDD\_n)}$ delay	10% of rising edge ($V_{(VDDIO)}$) to 10% of rising edge ($V_{(VDD\_n)}$)	0			ms
t_2	$V_{(VDD\_n)}$ rise time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required. V_{PDB} < 10% of $V_{(VDDIO)}$	0.05		5	ms
t_3	PDB to GPO2 delay	90% of rising edge (PDB) to 10% of rising edge (GPO2)	1.3			ms

- For restart function, the VDDIO, VDD needs to be 0V before restart.
- After power up, toggle UB933 0x27 bit 5 can help restart internal PLL