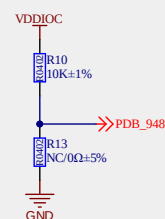
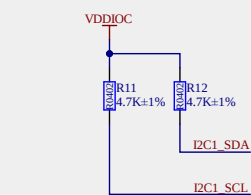
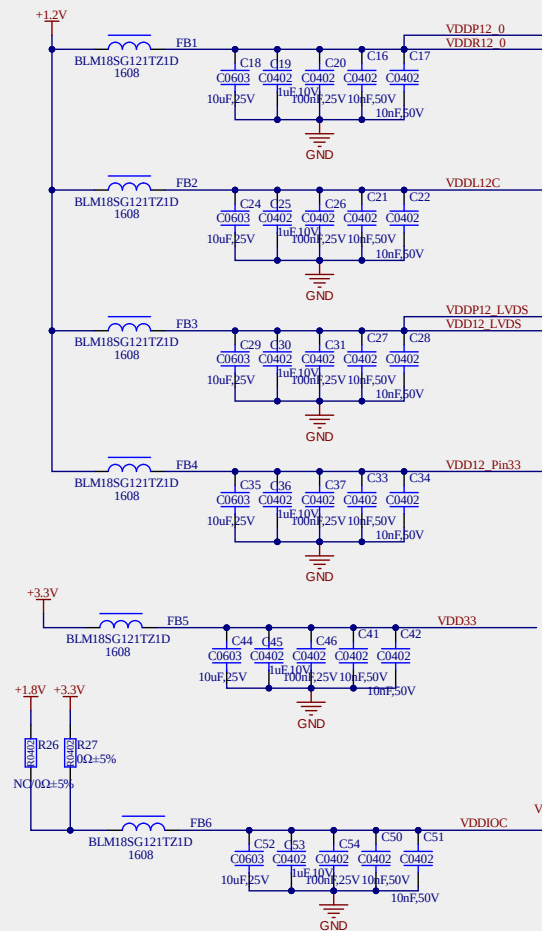
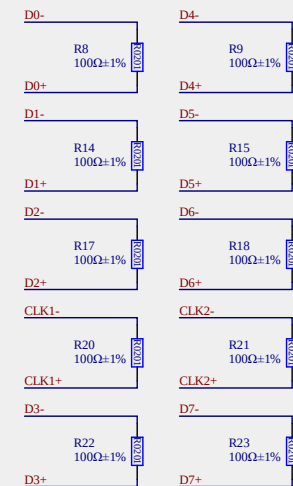
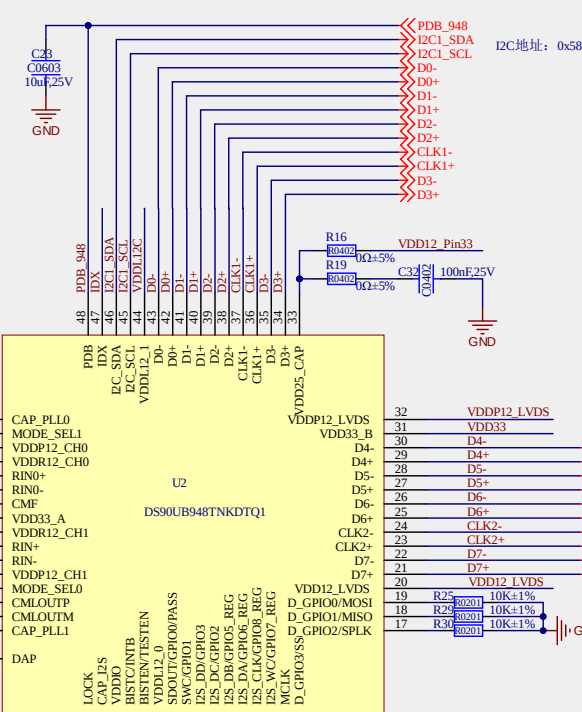
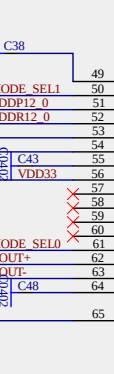
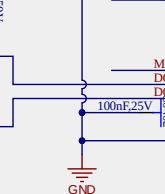
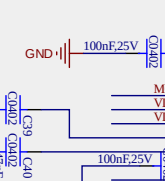
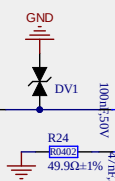
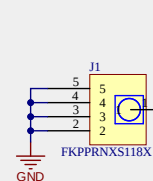


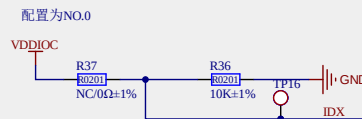
FPDLinkIII TO LVDS



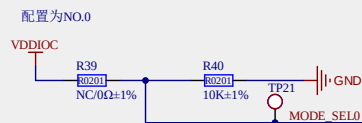
PDB = 1, device is enabled (normal operation)
PDB = 0, device is powered down



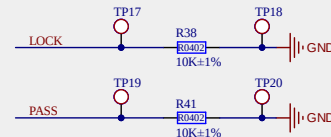
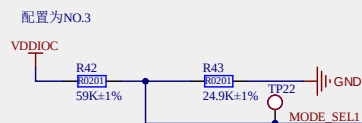
NO.	V _{IN} VOLTAGE V (V/TYP)	V _{IN} TARGET VOLTAGE VDC = 2.3 V	SUGGESTED STRAP RESISTORS (% tolerance)		PRIMARY ASSIGNED I ² C ADDRESS	
			R ₁ (Ω)	R ₂ (Ω)	I ² C-IT	I ² C-IT
0	0	0	Open	10	0x2C	0x00
1	0.189 × V _{DDIOH}	0.589	73.2	15	0x0E	0x0C
2	0.230 × V _{DDIOH}	0.757	66.5	20	0x00	0x60
3	0.205 × V _{DDIOH}	0.574	59	24.9	0x32	0x64
4	0.376 × V _{DDIOH}	1.241	49.9	30.1	0x34	0x69
5	0.405 × V _{DDIOH}	1.338	46.4	40.2	0x36	0x6C
6	0.556 × V _{DDIOH}	1.835	40.2	49.9	0x38	0x70



NO.	V _{IN} VOLTAGE	V _{OUT} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% tolerance)		MAP_SEL	OUTPUT_MOD E (10)	OUTPUT MODE
	V (V _{TPP})	VDD33+3.3 V	R1 (k Ω)	R2 (k Ω)			
	0	0	Open	0	0		Dual OLD output
1	0.168 V V_{DD33}	0.529	73.2	15	0	01	Dual SRAP output
2	0.220 V V_{DD33}	0.757	66.5	20	0	10	Single OLD output
3	0.266 V V_{DD33}	0.874	59	24.9	0	11	Replicate
4	0.379 V V_{DD33}	1.261	49.9	30.1	1	00	Dual OLD output
5	0.468 V V_{DD33}	1.538	46.4	40.9	1	01	Dual SRAP output
6	0.581 V V_{DD33}	1.856	40.8	49.9	1	10	Single SRAP output
7	0.804 V V_{DD33}	2.662	18.0	75	1	11	Replicate



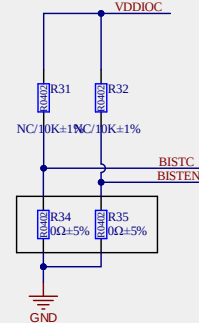
NO	V _{BIAS} VOLTAGE	V _{BIAS} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (% tolerance)	REPEAT R	MODE	HIGH-SPEED BACK CHANNEL	INPUT MODE
0	V (VTP)	VDIO3+3.3 V	R1 (KΩ)	R2 (KΩ)			
	0	0	0	0	0	5 Mbps	STP
1	0.550 × V _{DDIO3}	0.559	73.2	15	0	51 Mbps	STP
2	0.220 × V _{DDIO3}	0.757	66.5	20	0	10 Mbps	STP
3	0.206 × V _{DDIO3}	1.024	59	24.0	0	11 Mbps	COPE
4	0.376 × V _{DDIO3}	1.241	49.9	30.1	1	00 Mbps	STP
5	0.406 × V _{DDIO3}	1.538	46.4	40.2	1	51 Mbps	COPE
6	0.486 × V _{DDIO3}	1.835	40.2	49.9	1	10 Mbps	STP
7	0.566 × V _{DDIO3}	2.132	34.7	59	1	00 Mbps	COPE



LOCK=1:PLL acquired to the reference clock input
LOCK=0:PLL is unlocked

PASS=1:NO error detected

PASS=0:Error detected



BISTC=1,33MHz
BISTC=0,PCLK
BISTEN=1,mode is enabled
BISTEN=0,mode is disabled