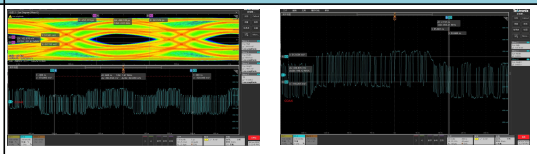
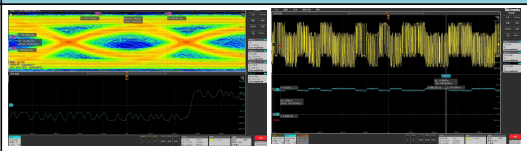
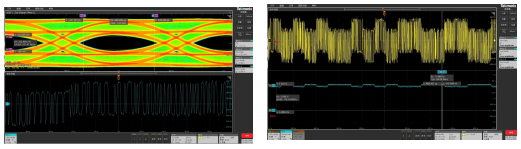
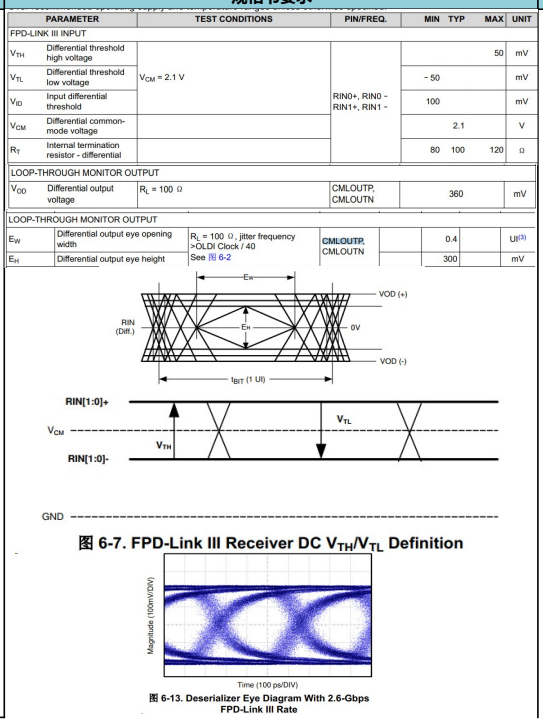
五、FPD LINK Ⅲ						
序号	输入电压/电流	测试点	整体波形(亮度100%)+电机转	测试结果	标准	判定
1	9V/2.3A	COAX		EW= EH= Vth= Vtl= Vcm=0V	≥0.4UI ≥70mV Vth≤50mV Vtl≥-50mV 0V	ok
序号	输入电压/电流	测试点	整体波形(亮度100%)+电机转	测试结果	标准	判定
2	9V/2.3A	RIN0-		EW= EH= Vth= Vtl= Vcm=0V	≥0.4UI ≥70mV Vth≤50mV Vtl≥-50mV 0V	ok
序号	输入电压/电流	测试点	整体波形(亮度100%)+电机转	测试结果	标准	判定
3	9V/2.3A	RIN0＋		EW= EH= Vth= Vtl= Vcm=0V	≥0.4UI ≥70mV Vth≤50mV Vtl≥-50mV 0V	ok
序号	输入电压/电流	测试点	整体波形(亮度100%)+电机转	测试结果	标准	判定
4	9V/2.3A	CMLOUTP CMLOUTN		EW= EH= Vth= Vtl= Vcm=0V	≥0.4UI ≥300mV Vth≤50mV Vtl≥-50mV 0V	ok
序号	电源网络	测试点	规格书要求	测试结果	标准	判定
7	NA	RIN± CMLOUTP CMLOUTN		NA	NA	

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III INPUT							
V_{TH}	Differential threshold high voltage	V_{CM} = 2.1 V	RIN0+, RIN0 - RIN1+, RIN1 -			50	mV
V_{TL}	Differential threshold low voltage			-50			mV
V_{ID}	Input differential threshold			100			mV
V_{CM}	Differential common-mode voltage				2.1		V
R_T	Internal termination resistor - differential			80	100	120	Ω
LOOP-THROUGH MONITOR OUTPUT							
V_{OD}	Differential output voltage	R_L = 100 Ω	CMLOUTP, CMLOUTN		360		mV
LOOP-THROUGH MONITOR OUTPUT							
E_W	Differential output eye opening width	R_L = 100 Ω, jitter frequency >OLDI Clock / 40 See 图 6-2	CMLOUTP, CMLOUTN		0.4		UI(3)
E_H	Differential output eye height				300		mV

图 6-7. FPD-Link III Receiver DC V_{TH}/V_{TL} Definition

图 6-13. Deserializer Eye Diagram With 2.6-Gbps FPD-Link III Rate