DS90UH941A-Q1 (PG1.0) vs DS90UH941AS-Q1 (PG2.1) Device Comparison

This document describes differences between DS90UH941A-Q1 (PG1.0) and DS90UH941AS-Q1 (PG2.1) devices.

Release	Date	Changes
1.0	06/07/2018	Initial version.
1.1	6/20/2018	Added Pin 40 recommendation difference.
1.2	07/09/2018	Added new part number for PG2.1
1.3	08/02/2020	Corrected 941AS info to PG2.1 and fixed typos in reg map

Device Identification: Top Mark

PDS90UH941A-Q1 PG1.0	PDS90UH941AS-Q1 PG2.1
UH941Q or PUH941AQ A0 xRCC TI YMS LLLL G4	UH941Q or PUH941AQ SL // Split lane operation TI YMS LLLL G4

\T/ = TI Logo

YM = Year/Month

LLLL = Lot Trace Code

S = Assembly Site Code

XXXX = Assembly details

Device Identification: I2C Registers

Register 0x0D[7:4] = 0001b - PDS90UH941A-Q1 (PG1.0)

Register 0x0D[7:4] = 0011b - PDS90UH941AS-Q1 (PG2.1)

1. Pin 40 Recommendation

PDS90UH941A-Q1 **PG1.0**	PDS90UH941AS-Q1 **PG2.1**
Pin 40 must be left floating.	Pin 40 may be tied to GND or left floating.

2. Feature Differences

The following table shows feature differences between PG1.0 and PG2.0 Si.

Feature	**PG1.0**	**PG2.1**
Dual DSI Aggregation – Left/Right	No	Yes
Dual DSI 2:2 Independent Mode	No	Yes
DSI Symmetric Splitting – Left/Right Mode	No	Yes
DSI Asymmetric Splitting Modes	No	Yes
DSI loosely packed 20-bit YCbCr 4:2:2 format	No	Yes
DSI packed 24-bit YCbCr 4:2:2 format	No	Yes
DSI packed 16-bit YCbCr 4:2:2 format	No	Yes
DSI packed 12-bit YCbCr 4:2:0 format	No	Yes
DSI packed 18-bit RGB666 format	No	Yes
DSI 16-bit RGB565 format	No	Yes

3. PG 1.0 Errata

All PG 1.0 Errata (See Appendix I) are fixed in PG2.1 Si.

4. Register Differences

The following table shows register differences between PG1.0 and PG2.0 Si.

Address	**Name**	**PG1.0**	**PG2.1**
0x0C[2]	GENERAL_STS: PCLK_DETECT	Always reads ‘0’	Default ‘0’
0x0D[7:4]	GPIO[0] Config: REV_ID	0001	0011
0x1A[0]	DATAPATH_CTL2: I2S_SURROUND	Default ‘0’	Default ‘1’

Address	Name	PG1.0	PG2.0
0x32	IMG_LINE_SIZE0	Not included	Included
0x33	IMG_LINE_SIZE1	Not included	Included
0x34	IMG_DELAY0	Not included	Included
0x35	IMG_DELAY1	Not included	Included
0x36	CROP_START_X0	Not included	Included
0x37	CROP_START_X1	Not included	Included
0x38	CROP_STOP_X0	Not included	Included
0x39	CROP_STOP_X1	Not included	Included
0x3A	CROP_START_Y0	Not included	Included
0x3B	CROP_START_Y1	Not included	Included
0x3C	CROP_STOP_Y0	Not included	Included
0x3D	CROP_STOP_Y1	Not included	Included
0x3E	SPLIT_CLK_CTL0	Not included	Included
0x3F	SPLIT_CLK_CTL1	Not included	Included
0x5C	FREQ_HYST	010	111
0x5B	RST_PLL_FREQ	1	0

Appendix I: PDS90UH941A-Q1 PG1.0 Prototype Device Errata

The list below describes known cases where the PDS90UH941A PG1.0 prototype silicon performs differently than the targeted behavior of the final production silicon. Recommended workarounds are provided where applicable.

Release	Date	Changes
1.0	05/01/2018	Initial release
1.1	06/08/2018	-Updated Errata #1 -Formatted Errata #4

Device Identification: Top Mark

DS90UH941A-Q1 PG1.0 Device Marking	PDS90UH941A-Q1 PG1.0 Device Marking
UH941AQ xxxxx TI YMS LLLL G4	PUH941AQ A0 xPCC TI YMS LLLL G4

\T/ = TI Logo

YM = Year/Month

LLLL = Lot Trace Code

S = Assembly Site Code

XXXX = Assembly details

Device Identification: I2C Registers

Register 0x0D[7:4] = 0001’b - PG1.0 Prototype

5. PLL lock range over temperature ramp is limited

Description: The voltage controlled oscillator (VCO) frequency in the phase locked loop (PLL) drifts when the ambient temperature around the device changes by ~60°C or more. With a large temperature shift, the loop filter voltage rails to a supply or ground and consequently causes loss of the PLL lock. At system level, the system display may exhibit distortions or flickering.

Workaround: The following programming sequence may be written as a part of the 941A initialization sequence as shown in Figures 2. **The workaround helps with -20°C → 80°C and 85°C → 25°C temperature ramps.**

- Step 1: SoC/MCU reads ambient temperature
  - When a system (i.e. a car) is started, read an external temperature sensor (on-board or on-chip on SoC) to determine the starting ambient temperature around the DS90UH941A-Q1 sub-system.
- Step 2: Based on ambient temperature, SoC/MCU programs the following sequence to the DS90UH941A-Q1 device registers as a part of the startup configuration.
  - Reg0x40=0x10
  - Reg0x41=0x4A
  - Reg0x42=0x3F
  - Reg0x41=0x4B
  - Reg0x42=0x89 if ambient temp < 60°C
    - (Reg0x42=0x8A if ambient temp is ≥ 60°C)
  - Reg0x41=0x49
  - Reg0x42=0x10
  - Reg0x42=0x00

  } Reset DSI PLL

  - Reg0x40=0x14
  - Reg0x41=0x4A
  - Reg0x42=0x3F
  - Reg0x41=0x4B

- Reg0x42=0x89 if ambient temp < 60°C
  - (Reg0x42=0x8A if ambient temp is ≥ 60°C)
- Reg0x41=0x49
- Reg0x42=0x10
- Reg0x42=0x00

} Reset FPD PLL

Note: This software workaround should be reprogrammed after any device reset.

Status: The workaround sequence is pre-programmed during production test. It reduces risk of failure during a cold-to-hot temperature ramp. If reducing the risk during a hot-to-cold temperature ramp is also important, then the full workaround, that involves measuring the ambient temperature, should be implemented.

The software workaround resets the input (DSI) PLL and the output (FPD) PLL at the end of their respective reconfiguration steps. If the Serializer had already established a lock with a companion Deserializer device, each of the PLL reset steps will cause a brief period of unlock in this link. The DSI PLL may be reset just before the FPD PLL reset step.

6. I2S clock required before enabling TDM-to-parallel conversion

Description: For the TDM- to-parallel conversion mode to be enabled, the I2S clock must be available and toggling prior to the register write enabling the TDM-to-parallel conversion.

Workaround: Provide the I2S clock prior to enabling the TDM-to-parallel conversion.

Status: The required recommendation will be included in the final revision of the DS90UH941A-Q1 datasheet.

7. RGB666 PACKED, RG565, 16-bit YCbCr 4:2:2 video formats not supported in dual DSI 3 lane mode

Description: When operating in Dual DSI 3 lane mode, RGB666 PACKED, RG565, and 16-bit YCbCr 4:2:2 video formats not supported.

Workaround: Not available.

Status: The limitation will be highlighted in the final revision of the DS90UH941A-Q1 datasheet.

8. HDCP Registers are reset by Digital RESET0

Description: The following is the list of registers and register bits that are reset with Digital RESET0:

Address (hex)	Bit(s)	Register Name (Bit name(s))
0xC0	7:0	HDCP_DBG
0xC2	7:0	HDCP_CFG
0xC3	7:0	HDCP_CTL
0xC6	7:0	ICR
0xC8	7:0	NVM_CTL
0xCE	7:0	BLUE_SCREEN

Workaround: If any of the affected registers are set to a value that differs from the default value, they would need to be set again after issuing a Digital RESET0.

Status: The required recommendations will be included in the final revision of the DS90UH941A-Q1 datasheet.

9. Device may fail to enter Dual lane mode when High-Speed Control channel is enabled

Description: For dual lane operation, if the High-Speed Control Channel (HSCC) is enabled, the Serializer may fail to detect capabilities and may not enter Dual mode as required.

Workaround: Force the back channel capabilities for Port 1 if HSCC mode is desired.

- Force the backchannel capability for Port1:
  - Set Reg0x1E=0x02 (Select Port1 in Port Select register)
  - Set Reg0x20=0x8F (Make Port1 Dual link capable in Deserializer Capabilities register)
  - Set Reg0x1E=0x01 (Select Port0 in Port Select register to restore the register default value)

- For forcing Dual Lane mode, use the following configuration:
  - Set Reg0x5B[2:0]=011b (Disable Auto-detect and Force Dual Link mode in DUAL_CTL1 register)

Any device configuration including this one should be written as a part of the 941A initialization sequence as shown in Figure 2.

Status: The required recommendations will be included in the final revision of the DS90UH941A-Q1 datasheet.

10. Frequency detection circuit may reset the FPD-Link III PLL during a temperature ramp

Description: When ambient temperature around the DS90UH941A-Q1 changes by more than 40°C, the frequency detection logic in the device can RESET the FPD-Link III PLL even though the input PCLK has not changed. This behavior may result in a loss of lock in the Deserializer and flicker on the system display.

Work-around: The following programming sequence is required for all systems. This should be written after the user register configuration of the DS90UH941A-Q1 and downstream Deserializer configuration.

- Disable the “Reset FPD-Link III PLL on Frequency Change” feature after the DS90UH941A-Q1 power-up
  - Set Reg0x5B[5]=0b (Disable PLL reset feature via RST_PLL_FREQ field in DUAL_CTL1 register)

Any device configuration including this one should be written as a part of the 941A initialization sequence as shown in Figures 2.

Status: The required recommendations will be included in the final revision of the DS90UH941A-Q1 datasheet.

11. Frequency detection circuit may cause change in Single / Dual mode during a temperature ramp

Description: When ambient temperature around the DS90UH941A-Q1 changes by more than 40°C and when PCLK is between 60 MHz and 78 MHz, the auto-detect feature can switch device configuration from Single-lane to Dual-lane mode (or vice-versa) even though the input PCLK has not changed. This causes a configuration change in Deserializer resulting in a momentary loss of lock that may result in display flicker.

Work-around: For input PCLK frequencies between 60 MHz and 78 MHz, TI recommends configuring the device to force Single or Dual Lane mode of operation.

- For forcing Single Lane mode, use the following configuration:
  - If the Deserializer is set in HSCC mode prior to forcing Single Lane mode, force the backchannel capability for Port1:
    - Set Reg0x1E=0x02 (Select Port1 in Port Select register)
    - Set Reg0x20=0x8F (Make Port1 Dual link capable in Deserializer Capabilities register)
    - Set Reg0x1E=0x01 (Select Port0 in Port Select register to restore the register default value)
  - Set Reg0x5B[2:0]=100b (Enable Auto-detect and disable Dual Link mode in DUAL_CTL1 register)

- For forcing Dual Lane mode, use the following configuration:
  - If the Deserializer is set in HSCC mode prior to forcing Dual Lane mode, force the backchannel capability for Port1:
    - Set Reg0x1E=0x02 (Select Port1 in Port Select register)
    - Set Reg0x20=0x8F (Make Port1 Dual link capable in Deserializer Capabilities register)
    - Set Reg0x1E=0x01 (Select Port0 in Port Select register to restore the register default value)
  - Set Reg0x5B[2:0]=011b (Disable Auto-detect and Force Dual Link mode in DUAL_CTL1 register)

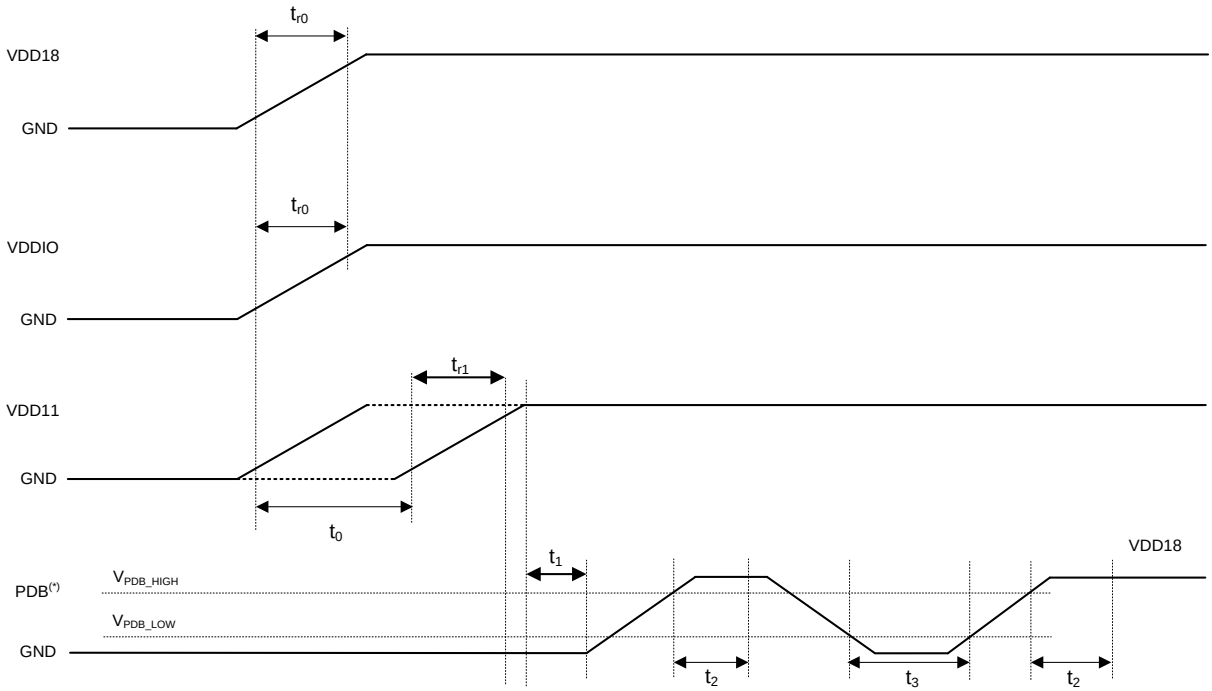
Any device configuration including this one should be written as a part of the 941A initialization sequence as shown in Figures 2.

Status: The required recommendations will be included in the final revision of the DS90UH941A-Q1 datasheet.

12. A stable DSI Clock required before DSI PLL comes out of reset

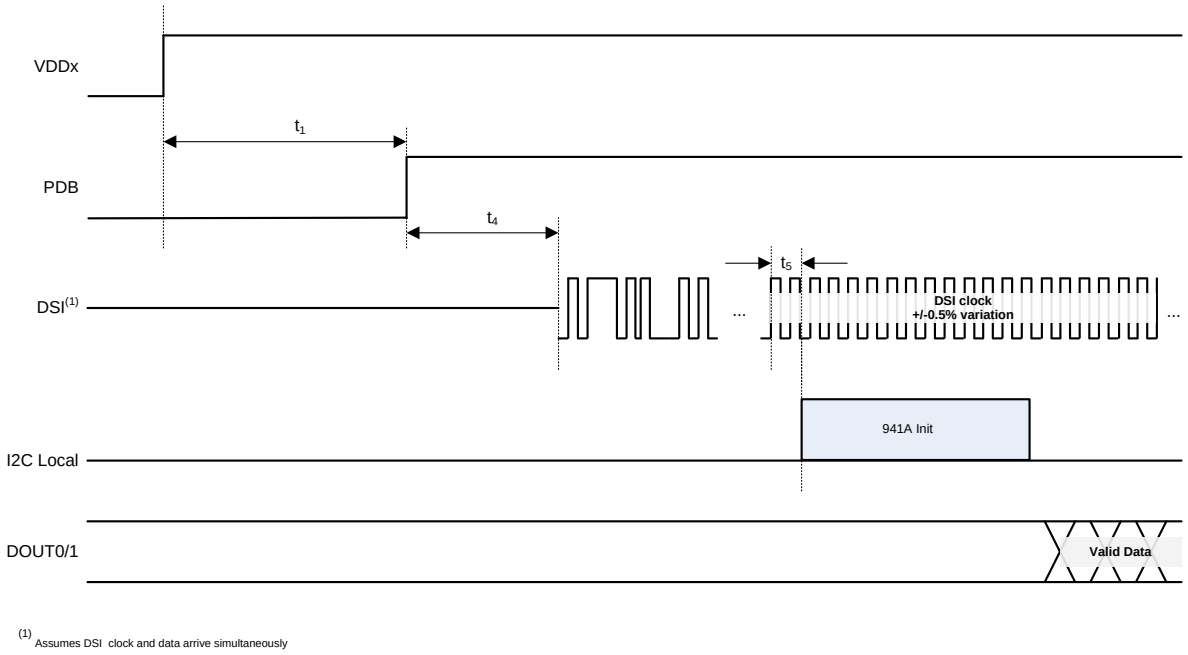
Description: In rare instances, the system display can show a pixelated mixed-color screen at power up if the DS90UH941A device is brought out of reset while the input DSI clock is still unstable. Note this symptom has a very low occurrence rate (in the region of ~1/1000 power cycles).

Workaround: Initialize the device after DSI CLK has stabilized as shown in Figure 2.



(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

Figure 1. Power Supply Sequencing Diagram



(1) Assumes DSI clock and data arrive simultaneously

Figure 2. Initialization Sequencing Diagram

Symbol	Description	Test Conditions	Min	Typ	Max	Units
tr0	VDDIO, VDD18 Rise time	These time constants are specified for rise time of power supply voltage ramp (10% - 90%)	0.2		1.5	ms
tr1	VDD11 Rise time		0.05		1.5	ms
t0	VDD11 Delay time	VDD18 and VDDIO need to ramp-up before VDD11.	0			ms
t1	PDB delay time	PDB should be released after all supplies are stable.	0			ms
t2	I2C Ready time	Starting from PDB high, the local I2C access is available after this time.	2			ms
t3	Hard Reset time	PDB negative pulse width required for the device reset.	2			ms
t4	PDB to DSI delay time	DSI needs to be applied after PDB release.	0			ms
t5	DSI Clock Stable to 941A Init delay time	DSI Clock must be within 0.5% of the target frequency and stable.	1			µs

Table 1. Timing Parameters

Status: The required recommendations will be included in the final revision of the DS90UH941A-Q1 datasheet.