**i.MX6D MIPI-CSI2 interface fail to lock DS90UR910 deserializer**

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# **Overview**

SanSan board with i.MX6D is not able to receive video input signals via MIPI-CSI2 from DS90UR910.

## **Board Setup**

There are mainly three board:

1. Video input source (YAMAHA YGV642)
   1. This board will feed 800x480, 60 fps RGB24 video input
2. Serializer (DS90UR905) board provided by Sansan
3. Sansan Board contains
   1. DS90UR910-Q1 10 to 75 MHz 24-bit Color FPD-Link II to CSI-2 Converter

* Video input source is connected with Serializer(DS90UR905) board.
* Serializer(DS90UR905) board is connected with Sansan board (contains DS90UR910-Q1 10 to 75 MHz 24-bit Color FPD-Link II to CSI-2 Converter).

# **Issue observed**

## **Issue**

* The serializer (DS90URE905 chip) board is receiving input signals (RGB24) and giving output signals on its output DOUT+/- pins.
* Though DS90UR910 on SanSan board receiving input signals on RIN+/- pins, it is not giving output on CLK+/- and DATA1-2+/- pins.
* On SanSan board, from i.MX6D side, MIPI-CSI2 DPHY is not able to receive and lock CLOCK with DS90UR910.
* On SanSan board, from DS90UR910 side, DS90UR910 is not providing output on CLK+/- and DATA1+/-, DATA2+/-.

# **Debug status**

## **Power measurement on DS90UR910**

We have measured power on following power pins of DS90UR910 and power is 1.77V on each pin.

1. VDDL
2. VDDP
3. VDDA
4. VDDIO
5. VDDCSI

## **Configuration of DS90UR910**

* Controlling of EQ and CONFIG strapped control inputs pins according to **Table 1. DS90UR910-Q1 Configuration Modes (pg-14) and Table 2. Receiver Equalization Configuration(pg-15)**
  + We are overriding EQ and CONFIG strapped control inputs of DS90UR910 with register settings.
  + We are setting “USEREG” field of Register CONFIG1 (0x01) to value ‘1’.
* MODE field of Register CONFIG1(0x01) set to “00”
  + We have also tried with setting this value to “01”
* Receive equalization control: EQ field of Register EQ Control (0x03).
  + Currently set value is “Approximately 3 dB”
  + Though, we have tried all possible 8 combinations.

## **Status pins of DS90UR910**

* LOCK pin status output
  + Status: Always remains LOW
* PASS pin normal mode status output pin
  + Status: Always remains LOW

## **Nitrogen6x Video Input Source**

* + We have replaced SanSan’s Video Input source board.
  + Instead, we used Boundary Device Nitrogen6x board as Video input source to feed 800x480 video RGB24 to Serializer (DS90UR905) board.

# **Result**

## **Status of DS90UR910**

* Sometimes, we seeing pulse signal on the LOCK pin of the DS90UR910 chip
* Below image shows LOCK signal observed on the pin 24 of DS90UR910 (sometimes)

|  |
| --- |
|  |

* The PASS pin remains always LOW.
* No signals are observed on the CLK+/-, DATA0+/- and DATA1+/- output pins.
* The significance of these pins is as follows: **Pin Functions (continued) (pg-4)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin | Pin  no. | Sign-al type | Description | Our observation |
| LOCK | 24 | Outp-ut | LVCMOS, LOCK status output;  LOCK = 1, PLL acquired lock to the reference clock input; DPHY outputs are active  LOCK = 0, PLL is unlocked | Sometimes pulse signals seen but most of the time remains LOW. |
| PASS | 25 | Outp-ut | LVCMOS, normal mode status output pin (BISTEN = 0);  PASS = 1: No fault detected on input display timing,  PASS = 0: Indicates an error condition or corruption in display timing. Fault condition occurs if:  1) DE length value mismatch measured once in succession,  2) VSync length value mismatch measured twice in succession,  BIST mode status output pin (BISTEN = 1);  PASS = 1: No error detected,  PASS = 0: Error detected. | The PASS line remains low  (i.e PASS = 0) |

## **Status of MIPI-CSI2 DPHY (i.MX6D)**

* The MIPI interface is not able to acquire a lock on the sensor clock and the MIPI-DPHY Status register (0x021DC014) always shows a value=0x200.

# **Community Help**

* We have raised following question on TI community:
  + <https://e2e.ti.com/support/interface/high_speed_interface/f/138/t/663610>.