Peter

1. 4 units from 20 units, screen went dark after 2 days or 2 weeks running, playing image pattern;
   a. Does the issue fail consistently with these 4 units and passing consistently with the other 16 units?
      PW: To my understanding, all the failure was seen in one test. Since some units took 2 weeks to appear the issue, they can not repeat it for diff times to study the regularity.

      If yes, have they tried to swap between the failing and passing unit, does the issue follow the unit or the board?

      PW: It is on product line, swapping device is not an easy thing, they have not done.

2. When the problem was happened, they pulled out all the statues register, listed as below:

	sn65dsi86 registers								
Sample Unit	0xf0	0xf1	0xf2	0xf3	0xf4	0xf5	0xf6	0xf7	0xf8
1	0x00	0x20	0x00	0x00	0x01	0x00	0x41	0x00	0x01
2	0x00	0x03	0x00	0x00	0x01	0x00	0x02	0x00	0x01
3	0x00	0x00	0x00	0x00	0x01	0x00	0x40	0x00	0x01
4	0x00	0x24	0x00	0x00	0x41	0x00	0x41	0x01	0x01

   a. Please clear the flags by writing 0xFF to these registers, and then read back the status flags. We need to make sure these errors are real
      i. After they clear the register and still see consistent error at register 0xF1h, they can try to change the RX EQ setting at register 0x11h to see if helps
      ii. Please also check DSI interface to make sure the setup and hold timing meets the DSI86 timing requirement as specified in the datasheet
      iii. For error at register 0xF6h and F7h, please use the attached spreadsheet and the panel EDID info to verify register 0x20h to 0x3Ah is programming correctly to match the panel EDID info

iv. Since 0xF8 shows link training to be passing, the DP interface looks to be solid even though lane 0 eye height is worse. They can compensate for the lane 0 eye height drop by changing the lane 0 VOD in Table 28

3. For schematic review
   a. EDP_HPD missing recommended 51k 1% resistor
4. Please send the actual layout file for review as it is difficult to review in the pdf format
5. For the scope capture, what is channel 1 and 2?
   PW: Channel 1 and 2 are similar with Channel 3, only Channels 0 looks diff.

   DL: I am referring to the power sequence scope capture, what is channel 1 and 2 in the scope capture?

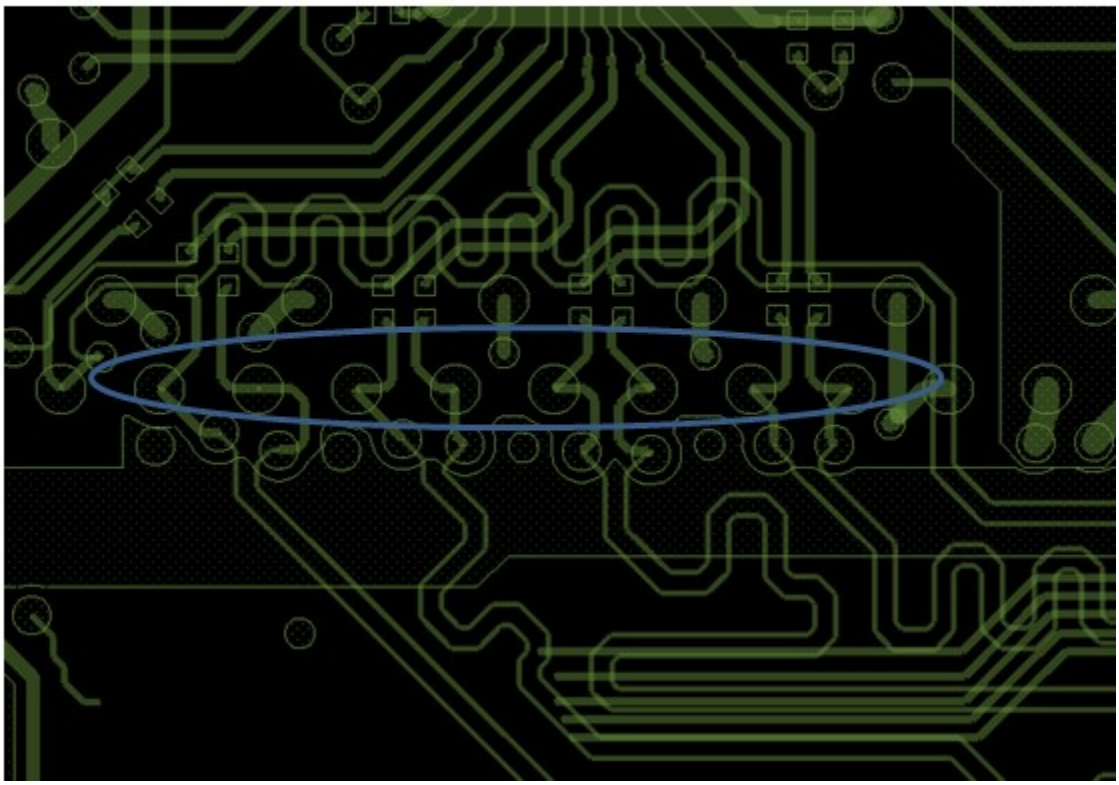
6. Please dump out the register when DSI86 is in working condition

Two things I noticed when looking at their layout.

Why do they rout the trace as circled below?

Please note our recommendation

The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on reflection and EMI.



Second thing I noticed is the inter-pair skew on the DSI interface. The DSI86 samples data on rising and falling edge of DSI clock. Any variation in length between CLK and DATA lanes will impact setup and hold requirement. My recommendation is to match lane length as close to each as possible. DSI_A data/clock should be within 5 mils of each other. DSI_B data/clock should be within 5 mils of each other.

Customer needs to understand the inter-pair skew from DSI source to DSI 86 input. For a 4k2k 60MHz 18bpp, the DSI clock will be around 700MHz. The entire inter-pair skew needs to be less than 66ps.

Thanks

David