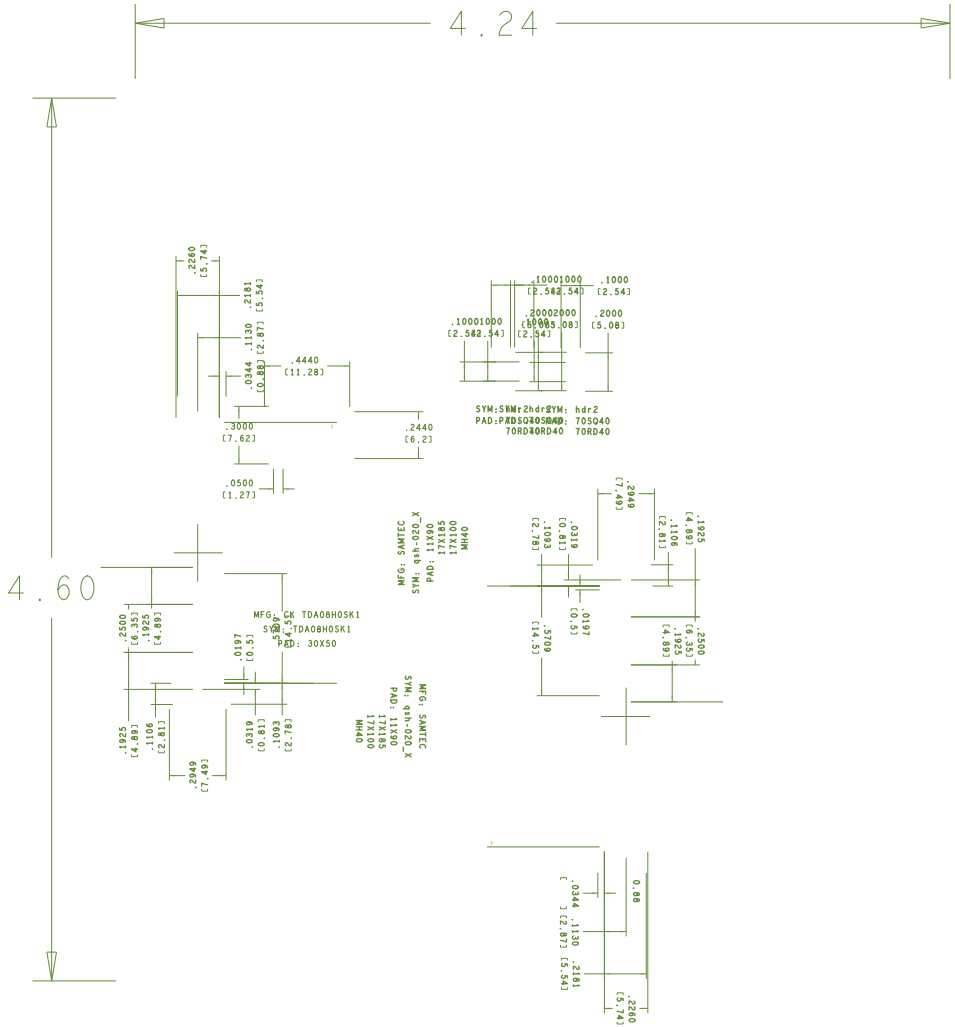
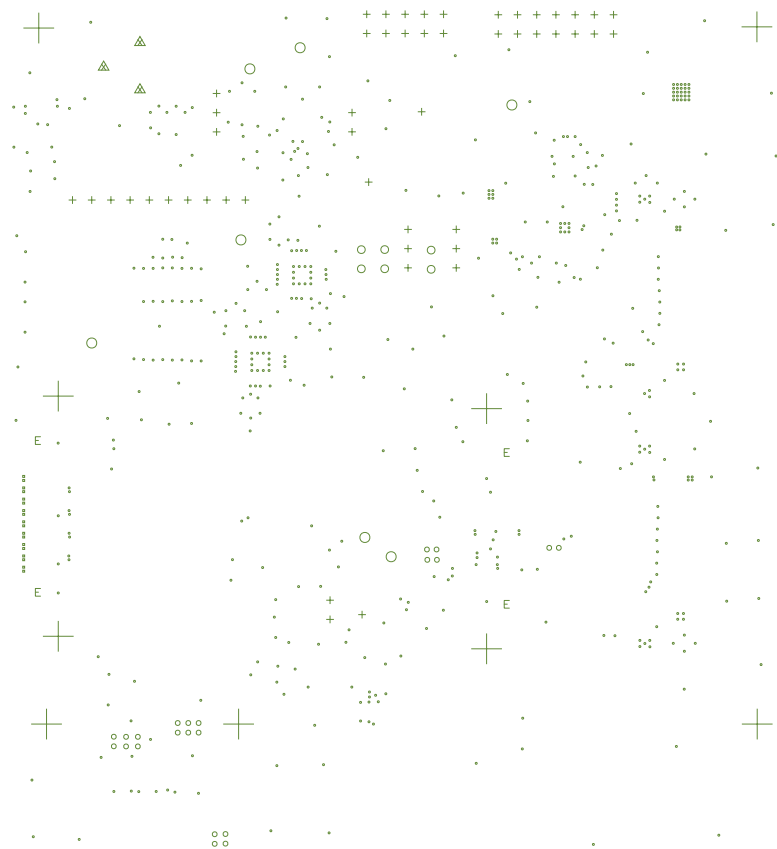




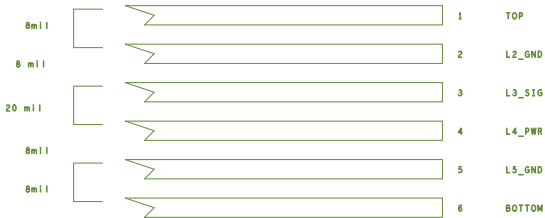
4.24



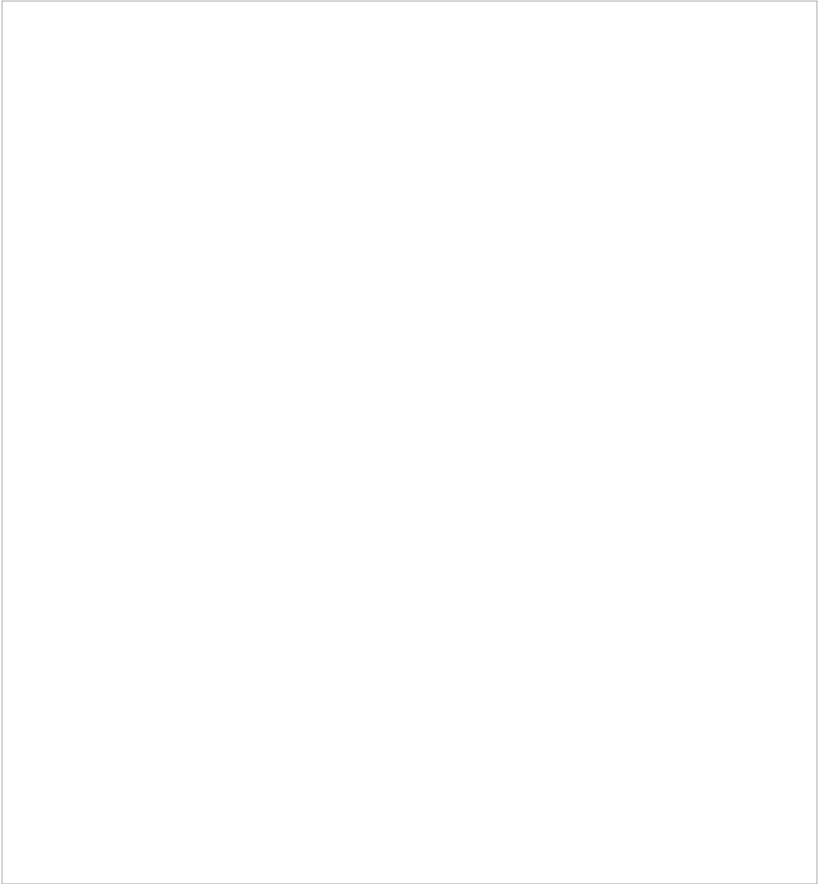


DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
	5.0	+3.0/-3.0	PLATED	55
	6.0	+3.0/-3.0	PLATED	60
.	8.0	+3.0/-3.0	PLATED	501
o	16.0	+3.0/-3.0	PLATED	26
+	38.0	+3.0/-3.0	PLATED	51
o	40.0	+3.0/-3.0	PLATED	6
o	43.0	+3.0/-3.0	PLATED	3
o	52.0	+3.0/-3.0	PLATED	7
△	120.0	+3.0/-3.0	PLATED	2
△	140.0	+3.0/-3.0	PLATED	1
+	160.0	+3.0/-3.0	PLATED	9
	33.465	+3.0/-3.0	NON-PLATED	2
	39.37	+3.0/-3.0	NON-PLATED	1
E	40.0	+3.0/-3.0	NON-PLATED	4
	51.181	+3.0/-3.0	NON-PLATED	1
	63.386	+3.0/-3.0	NON-PLATED	4

ART FILM - NOTES



ART FILM - NOTES



GENERAL NOTES. UNLESS OTHERWISE SPECIFIED

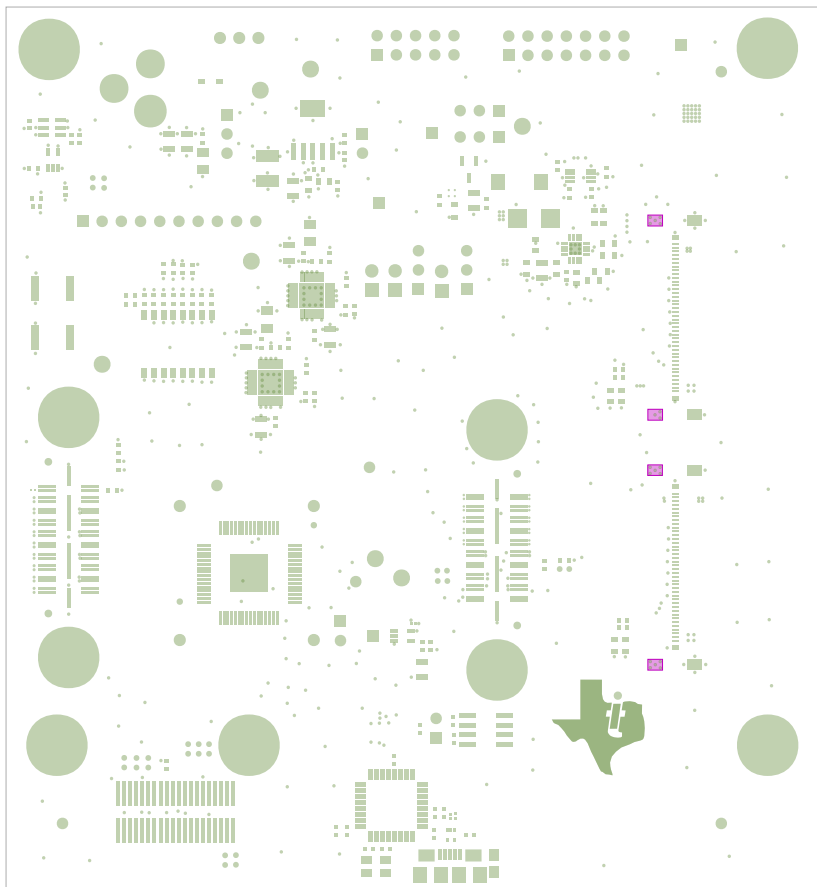
1. ALL FABRICATION ITEMS MUST MEET OR EXCEED BEST INDUSTRY PRACTICE : IPC-A-600C (Commercial std.)
2. LAMINATE MATERIAL : FR4 POLYCLAD 370 or EQUIVALENT
3. COPPER WEIGHT : 1oz START INTERNAL, 1/2oz START EXTERNAL
4. FINISHED BOARD THICKNESS : .062 +/- 10%
5. MAXIMUM WARP AND TWIST TO BE : .005 INCH PER INCH
6. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH. THERE MUST BE 1MIL OR GREATER PLATING ON EACH SIDE OF THE BARREL WHEN VIEWED IN THE CROSS SECTION
7. MINIMUM ANNULAR RING OF PLATED-THRU HOLES TO BE .002 INCH
8. MINIMUM ALLOWABLE LINE REDUCTION TO BE 20% OR .002 WHICHEVER IS GREATER
9. 0.003 AND 0.005 SIGNAL LINES ON LAYER 1 & 3 & 6 TO BE IMPEDANCE CONTROLLED 100 OHMS DIFFERENTIAL +/- 10%
10. 0.014 SIGNAL LINES ON LAYER 1 & 3 & 6 TO BE IMPEDANCE CONTROLLED 50 OHMS +/- 10%
11. DIELECTRIC CONSTANTS ARE CORE : 4.1
PREPREG : 4.1
12. Via's in SMT device pads to be filled with Non Conductive Epoxy. ANY VOID IN THE FILL MATERIAL MUST NOT BE GREATER THAN 25% OF THE FINISHED HOLE DIAMETER
13. A CROSS SECTION MOUNT AND DIGITAL PHOTO'S OF VIA'S TO BE PROVIDED
14. USE THE (DRPP) DUTCH REVERSE PLATING PROCESS
15. VIAS will be tented.
16. ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER.

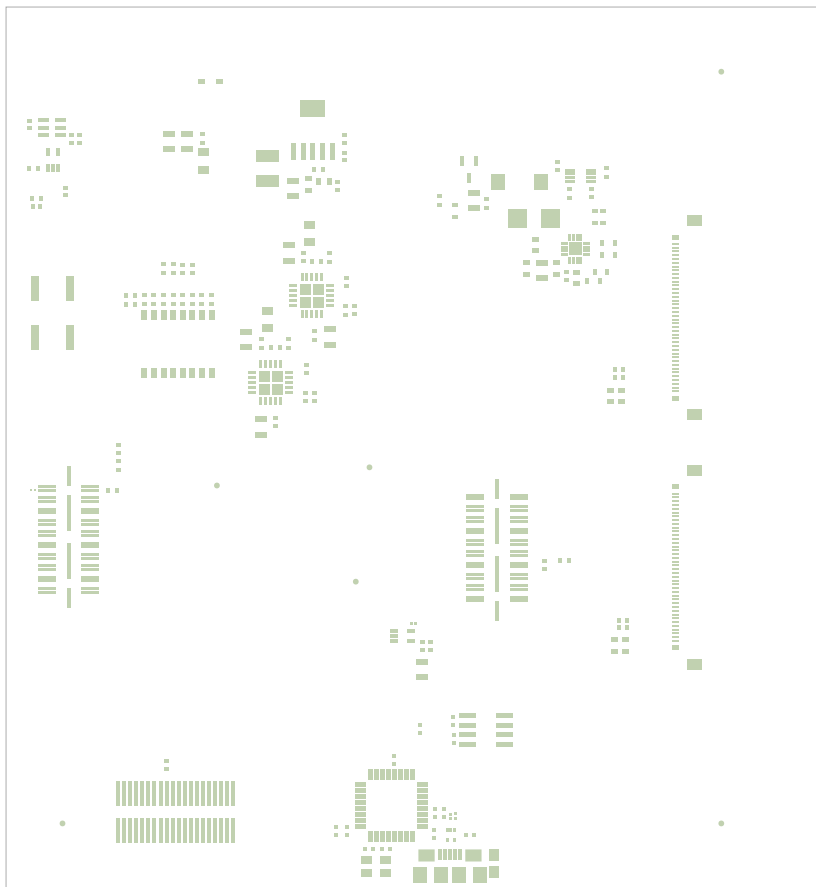
PROCESS NOTES

1. CIRCUITRY ON OUTER LAYERS TO BE PLATED WITH : NICKEL GOLD
2. SOLDERMASK BOTH SIDES PER ARTWORK : BLUE LPI
3. SILKSCREEN BOTH SIDES PER ARTWORK : COLOR = WHITE

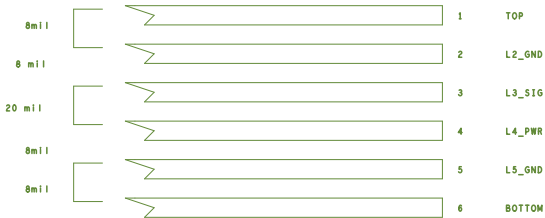
Layout Notes

1. For all differential pairs(DSI and LVDS) in this design follow the guidelines decribed below
 - Route together with controlled differential 100ohm impedance and controlled single 50ohm impedance.
 - Keep away from other high speed signals especially all FlatA/FlatB* signals.
 - Keep lengths within 5mil of each other.
 - Keep traces on layers adjacent to the ground plane.
 - Keep number of VIAS to minimum.
 - If VIAS used make it symetrical through all signals.
 - Keep diff pairs separated at least by x3 of the trace width
 - NO STUBS on the signal path, components should be placed such that the signals can routed in pass-thru manner
2. Bypass caps (C1 to C8 and C56 to C60) and FB1 should be placed close to U1 (SN65DSI85)
3. Place R105 and R104 as near as possible to REFCLK terninal on U1
4. R104 and R105 have a shared footprint node.
5. Bypass caps (C12 to C16) and FB2 should be placed close to J2
6. Bypass caps (C17 to C21) and FB3 should be placed close to J5
7. Caps C22 and C23 should be placed close to U3
8. R67 to R693 should be placed close to U5
9. Caps C28, C29 and C30 should be placed close to U6
10. Place TP3, TP5, LP4, LP5 as convenient for oscilloscope probe grounds





ART FILM - anotation



ART FILM - anotation

