LVDS Interface LSI

LVDS Splitter for Automotive

BU92RTF82-M

General Description

BU92RTF82-M LVDS splitter has 8 bits LVDS receiver and 8 bits LVDS transmitter, can split 56 bits (2 channels of R/G/B 24 bits and DE, HSYNC, VSYNC, Control Data) of LVDS serial data. Maximum data bit rate is 0.945 Gbps each lane. BU92RTF82-M has reduced swing mode to be able to except further low power and low EMI.

Flexible Input / Output mode is suitable for a variety of application interface.

Features

- AEC-Q100 Qualified *(Note 1)*
- LVDS Receiver Support Wide Frequency Range from 20 MHz up to 150 MHz (☆) *(Note 2)*
- LVDS Transmitter Support Wide Frequency Range from 20 MHz up to 135 MHz (☆) *(Note 2)*
- Support Reduced Swing LVDS Output for Low EMI
- Support SSCG (Spread Spectrum Clock Generator)
- Support AGING Function
- Support SPI Slave Function (☆) *(Note 2)*
- Support SPI Master Function (☆) *(Note 2)*
- Support 64Mbit External Flash Memory
- Support Internal OSC (Oscillator) (☆) *(Note 2)*
- Integrated Termination Resistor in LVDS Receiver
- Flexible Input / Output Mode
- Support Fail Detect Function
- Support CRC (Cyclic Redundancy Check) Function
- Support OSD (On-Screen Display) Gen2 Function
- Support IMC (Image Comparison) Function
- Support BDP (Blind Data Packet) Function

(Note 1) Grade2

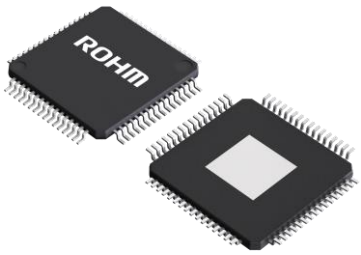
(Note 2) (☆): Special Characteristics

Key Specifications

- Supply Voltage Range: VDDIO 3.0 V to 3.6 V
  LVDSVDD 3.0 V to 3.6 V
  VDD15 1.35 V to 1.65 V
- LVDS Input Frequency 20 MHz to 150 MHz
- LVDS Output Frequency 20 MHz to 135 MHz
- Operating Temperature Range -40 °C to +105 °C

Package

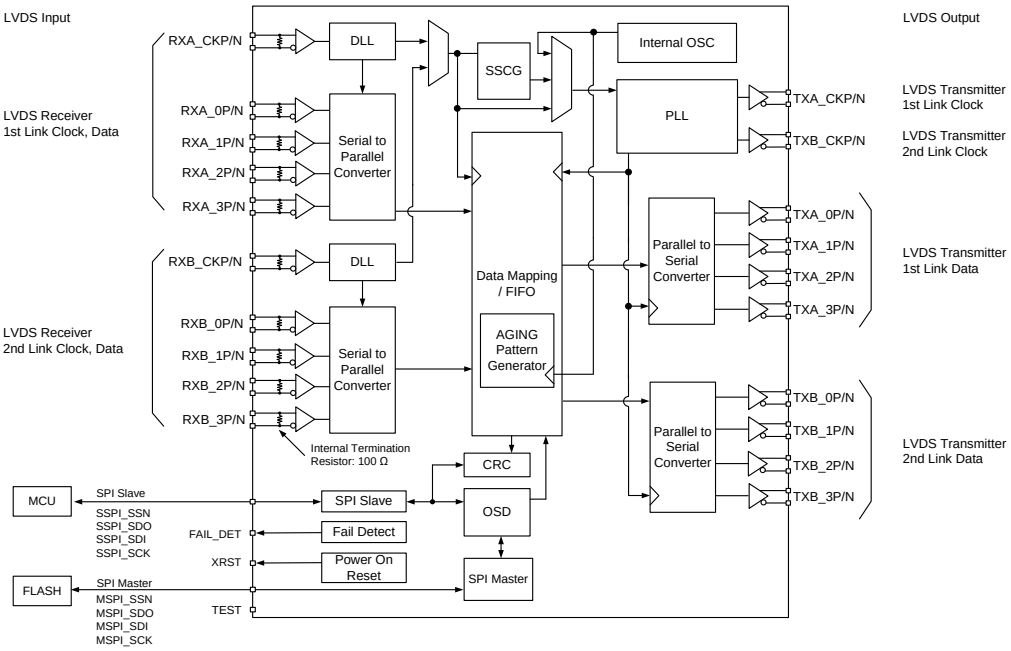
	W (Typ) x D (Typ) x H (Max)
HTQFP64AV	12.00 mm x 12.00 mm x 1.00 mm



Applications

- Car Navigation System
- CID (Center Information Display)
- HUD (Head Up Display)

Block Diagram



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Support Input / Output Mode

This product supports various input / output mode.
Pin configuration can be set by register of “LVRX_CH_SWAP”, “LVRX_FLIPMODE”, “LVTX_CH_SWAP”, “LVTX_FLIPMODE” (refer to Table 12 and Table 13).

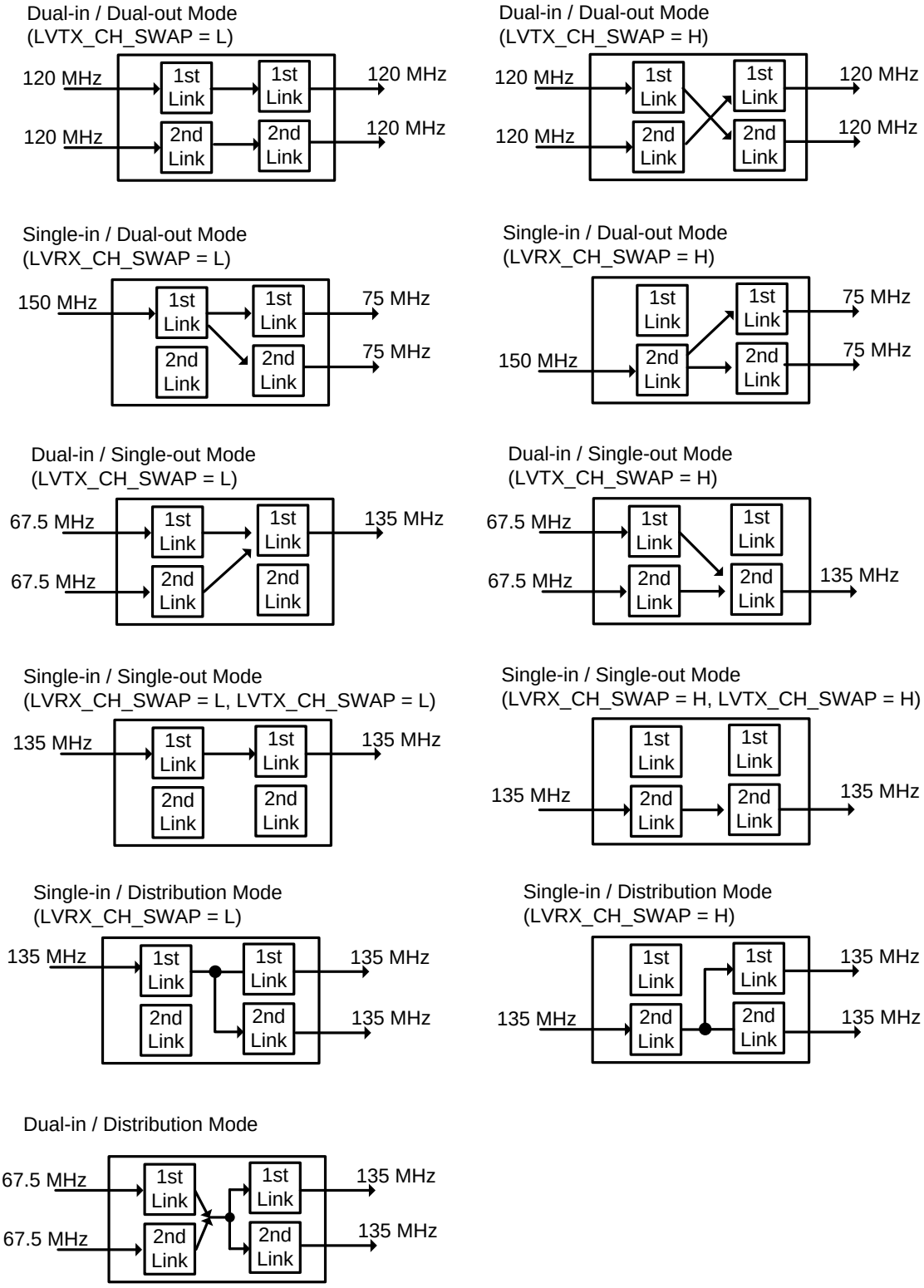


Figure 1. Input / Output Mode Example

LVDS Receiver Pins Status in Each Input / Output Mode

Input / Output Mode		Dual-in / Dual-out Dual-in / Single-out Dual-in / Distribution		Single-in / Dual-out Single-in / Single-out Single-in / Distribution	
Register: LVRX_SINGLE		L		H	
Register: LVRX_CH_SWAP		L	H	L	H
LVDS Receiver 1st Link	RXA_0N	Valid	Valid	Valid	Unused *(Note 3)*
	RXA_0P				
	RXA_1N	Valid	Valid	Valid	
	RXA_1P				
	RXA_2N	DE Required	Valid	DE Required	
	RXA_2P				
	RXA_CKN	Required	Required	Required	
	RXA_CKP				
	RXA_3N	Valid	Valid	Valid	
	RXA_3P				
LVDS Receiver 2nd Link	RXB_0N	Valid	Valid	Unused *(Note 3)*	Valid
	RXB_0P				
	RXB_1N	Valid	Valid		Valid
	RXB_1P				
	RXB_2N	Valid	DE Required		DE Required
	RXB_2P				
	RXB_CKN	Required	Required		Required
	RXB_CKP				
	RXB_3N	Valid	Valid		Valid
	RXB_3P				

(Note 3) LVDS receiver pins unused are recommended to connect to the LVDSVDD pin.

Pin Configuration

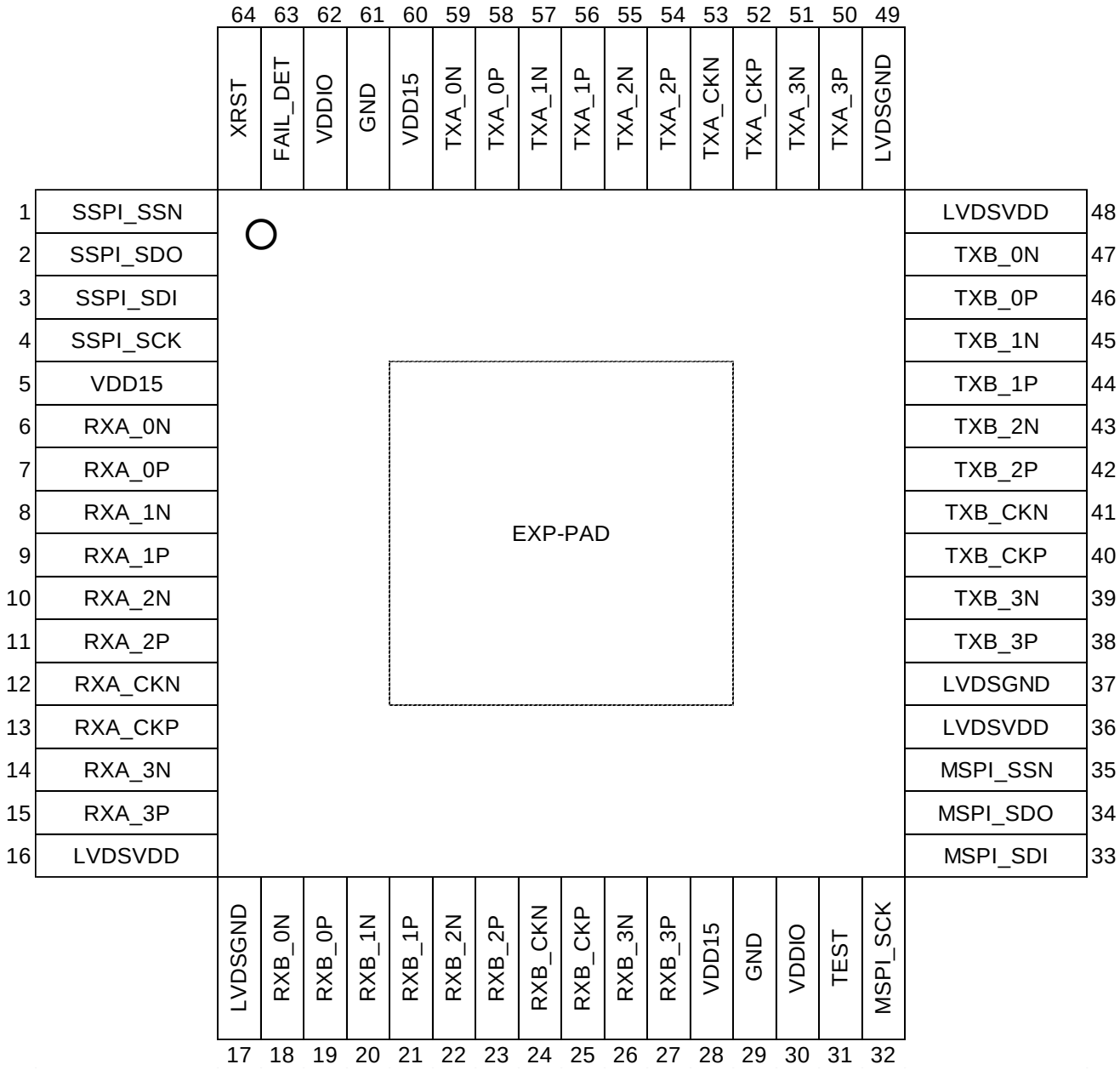


Figure 2. Pin Configuration (TOP VIEW)

Pin Descriptions

LVDS Receiver Pins

Pin No.	Pin Name	Type	Descriptions
6	RXA_0N	LVDS IN	LVDS receiver 1st link data
7	RXA_0P	LVDS IN	
8	RXA_1N	LVDS IN	
9	RXA_1P	LVDS IN	
10	RXA_2N	LVDS IN	
11	RXA_2P	LVDS IN	
14	RXA_3N	LVDS IN	
15	RXA_3P	LVDS IN	
12	RXA_CKN	LVDS IN	LVDS receiver 1st link clock
13	RXA_CKP	LVDS IN	
18	RXB_0N	LVDS IN	LVDS receiver 2nd link data
19	RXB_0P	LVDS IN	
20	RXB_1N	LVDS IN	
21	RXB_1P	LVDS IN	
22	RXB_2N	LVDS IN	
23	RXB_2P	LVDS IN	
26	RXB_3N	LVDS IN	
27	RXB_3P	LVDS IN	
24	RXB_CKN	LVDS IN	LVDS receiver 2nd link clock
25	RXB_CKP	LVDS IN	

LVDS Transmitter Pins

Pin No.	Pin Name	Type	Descriptions
59	TXA_0N	LVDS OUT	LVDS transmitter 1st link data
58	TXA_0P	LVDS OUT	
57	TXA_1N	LVDS OUT	
56	TXA_1P	LVDS OUT	
55	TXA_2N	LVDS OUT	
54	TXA_2P	LVDS OUT	
51	TXA_3N	LVDS OUT	
50	TXA_3P	LVDS OUT	
53	TXA_CKN	LVDS OUT	LVDS transmitter 1st link clock
52	TXA_CKP	LVDS OUT	
47	TXB_0N	LVDS OUT	LVDS transmitter 2nd link data
46	TXB_0P	LVDS OUT	
45	TXB_1N	LVDS OUT	
44	TXB_1P	LVDS OUT	
43	TXB_2N	LVDS OUT	
42	TXB_2P	LVDS OUT	
39	TXB_3N	LVDS OUT	
38	TXB_3P	LVDS OUT	
41	TXB_CKN	LVDS OUT	LVDS transmitter 2nd link clock
40	TXB_CKP	LVDS OUT	

Pin Descriptions - continued

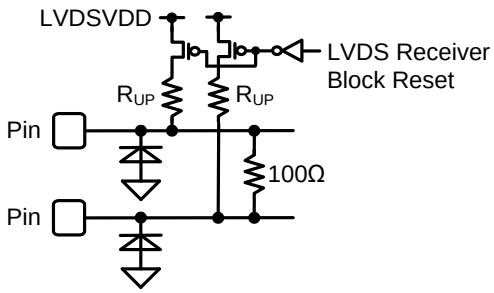
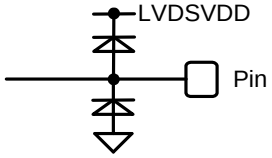
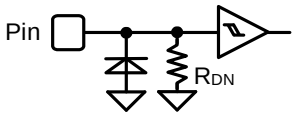
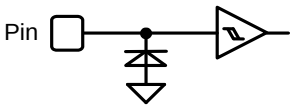
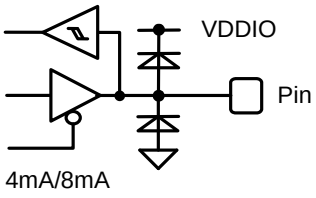
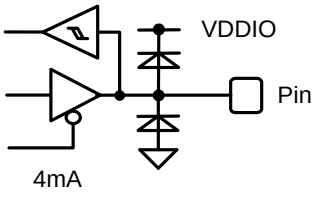
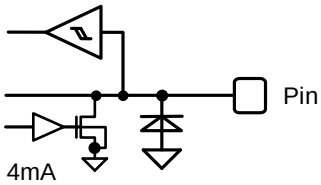
Others Pins

Pin No.	Pin Name	Type	Descriptions
1	SSPI_SSN	LVCMOS IN	SPI Slave SPI chip select signal
2	SSPI_SDO	LVCMOS IN/OUT	SPI Slave SPI output data signal
3	SSPI_SDI	LVCMOS IN	SPI Slave SPI input data signal
4	SSPI_SCK	LVCMOS IN	SPI Slave SPI clock signal
31	TEST	LVCMOS IN	Test mode enable with internal pull down resistor Connect GND directly L: Normal operation H: Vendor test mode
32	MSPI_SCK	LVCMOS IN/OUT	SPI Master SPI clock signal
33	MSPI_SDI	LVCMOS IN/OUT	SPI Master SPI input data signal
34	MSPI_SDO	LVCMOS IN/OUT	SPI Master SPI output data signal
35	MSPI_SSN	LVCMOS IN/OUT	SPI Master SPI chip select signal
63	FAIL_DET	LVCMOS IN/OUT	Fail mode detect signal L: Fail H: Normal
64	XRST	LVCMOS IN/OUT	Power down L: Power down (All LVDS output signals are Hi-Z) H: Normal operation
	EXP-PAD	-	Must be tied to ground

Power and Ground Pins

Pin No.	Pin Name	Type	Descriptions
29,61	GND	Ground	Ground for I/O
17,37,49	LVDSGND	Ground	Ground for LVDS
30,62	VDDIO	Power	Power supply for I/O (3.3 V)
5,28,60	VDD15	Power	Power supply for Digital (1.5 V)
16,36,48	LVDSVDD	Power	Power supply for LVDS (3.3 V)

I/O Equivalence Circuit

Type	Circuit Type	Applied Pins
LVDS IN		RXA_0P/N, RXA_1P/N, RXA_2P/N, RXA_3P/N, RXA_CKP/N, RXB_0P/N, RXB_1P/N, RXB_2P/N, RXB_3P/N, RXB_CKP/N
LVDS OUT		TXA_0P/N, TXA_1P/N, TXA_2P/N, TXA_3P/N, TXA_CKP/N, TXB_0P/N, TXB_1P/N, TXB_2P/N, TXB_3P/N, TXB_CKP/N
LVCMOS IN		TEST
LVCMOS IN		SSPI_SSN, SSPI_SDI, SSPI_SCK
LVCMOS IN/OUT		SSPI_SDO, MSPI_SSN, MSPI_SDO, MSPI_SDI, MSPI_SCK
LVCMOS IN/OUT		FAIL_DET
LVCMOS IN/OUT		XRST

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage1 (1.5V)	VDD_{15}	-0.3 to + 2.1	V	For VDD15
Supply Voltage2 (3.3V)	VDD_{33}	-0.3 to + 4.5	V	For VDDIO, LVDSVDD
Input Voltage	V_{IN}	-0.3 to VDD_{33} + 0.3	V	VDD_{33} + 0.3 < 4.5 V
Storage Temperature Range	Tstg	-55 to + 125	°C	
Maximum Junction Temperature	Tjmax	125	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
HTQFP64AV				
Junction to Ambient	θ_{JA}	51.9	24.7	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	6.0	5.0	°C/W

(Note 4) Based on JESD51-2A(Still-Air), using a BU92RTF82-M Chip.
(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 6) Using a PCB board based on JESD51-3.
(Note 7) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 8)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 8) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter		Symbol	Rating			Unit	Conditions
			Min	Typ	Max		
Power Supply Voltage1		VDD_{15}	1.35	1.50	1.65	V	For VDD15
Power Supply Voltage2		VDD_{33}	3.0	3.3	3.6	V	For VDDIO, LVDSVDD
Operating Temperature Range		Tj	-40	+25	+105	°C	
Operating Frequency SSCG Disabled	Dual-in / Dual-out	f_{IN}	20	-	120	MHz	
		f_{OUT}	20	-	120	MHz	
	Single-in / Dual-out	f_{IN}	40	-	150	MHz	
		f_{OUT}	20	-	75	MHz	
	Dual-in / Single-out Dual-in / Distribution	f_{IN}	20	-	67.5	MHz	
		f_{OUT}	40	-	135	MHz	
	Single-in / Distribution	f_{IN}	20	-	135	MHz	
		f_{OUT}	20	-	135	MHz	
	Single-in / Single-out	f_{IN}	20	-	135	MHz	
		f_{OUT}	20	-	135	MHz	
Operating Frequency SSCG Enabled*(Note 9)*	Dual-in / Dual-out	f_{IN}	20	-	120	MHz	
		f_{OUT}	20	-	120	MHz	*(Note 10)*
	Single-in / Dual-out	f_{IN}	40	-	150	MHz	
		f_{OUT}	20	-	75	MHz	*(Note 10)*
	Dual-in / Single-out Dual-in / Distribution	f_{IN}	20	-	67.5	MHz	
		f_{OUT}	40	-	135	MHz	*(Note 10)*
	Single-in / Distribution	f_{IN}	20	-	120	MHz	
		f_{OUT}	20	-	120	MHz	*(Note 10)*
	Single-in / Single-out	f_{IN}	20	-	120	MHz	
		f_{OUT}	20	-	120	MHz	*(Note 10)*

(Note 9) Valid range of operating frequency depends on internal SSCG parameter settings
(Note 10) Averaged frequency of modulated output clocks.

Electrical Characteristics

DC Characteristics

Table 1. LVCMOS DC Specifications

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
High Level Input Voltage	V_{IH}	VDDIO x 0.7	-	VDDIO	V	All LVCMOS IN Pins
Low Level Input Voltage	V_{IL}	GND	-	VDDIO x 0.3	V	All LVCMOS IN Pins
Hysteresis Voltage	V_H	-	600	-	mV	*(Note 11)*
Input Leakage Current	I_{IZ}	-10	-	+10	µA	0 V ≤ V_{IN} ≤ VDDIO (Except the TEST Pin)
Pull Down Resistor	R_{DN}	35	50	65	kΩ	The TEST Pin
High Level Output Voltage	V_{OH}	VDDIO - 0.4	-	-	V	I_{OH} = -4 mA / -8 mA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 4 mA / 8 mA

(Note 11) This spec is for schmitt trigger type cell.

Table 2. LVDS Receiver DC Specifications

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Differential Input Voltage	V_{ID}	100	-	600	mV	
Differential Input “H” Threshold	V_{TH}	-	-	+50	mV	
Differential Input “L” Threshold	V_{TL}	-50	-	-	mV	
Differential Input Common Mode Voltage	V_{CM}	$\|V_{ID}\|$ / 2	1.2	2.4 - $\|V_{ID}\|$ / 2	V	
Internal Termination Resistor	R_{TERM}	90	100	110	Ω	Tj = 25 °C
Pull Up Resistor	R_{UP}	200	300	400	kΩ	*(Note 12)*
Differential Input Leakage Current	I_{RXIZ}	-20	-	+20	µA	*(Note 12)*

(Note 12) Value of each LVDS receiver input pin.
Pull up resistor becomes the half value on the IC for the internal termination resistor.
Differential input leak current becomes the double current value on the IC for the internal termination resistor.

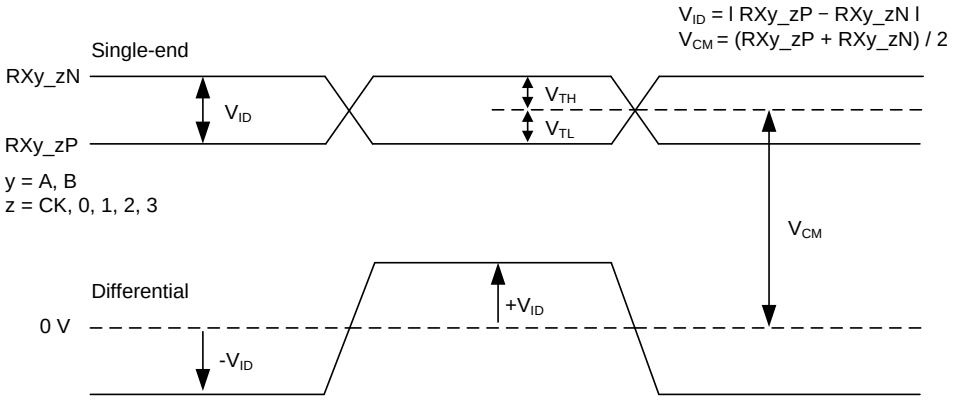


Figure 3. LVDS Receiver DC Characteristics Definition

DC Characteristics - continued

Table 3. LVDS Transmitter DC Specifications

Parameter	Symbol	Limit			Unit	Conditions	
		Min	Typ	Max			
Differential Output Voltage	V_{OD}	250	350	450	mV	R_L = 100 Ω (Refer to Figure 8)	Register: LVTX_VOD = HH
		100	200	300			Register: LVTX_VOD = LL
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	-	-	35	mV	R_L = 100 Ω (Refer to Figure 8)	
Common Voltage	V_{OC}	1.125	1.250	1.375	V	R_L = 100 Ω (Refer to Figure 8)	
Change in V_{OC} Between Complementary Output States	ΔV_{OC}	-	-	35	mV		
Output Tri-state Current	I_{OZ}	-10	-	+10	µA	XRST = L, LVDS Transmitter Pin Force = 0 V to LVDSVDD	

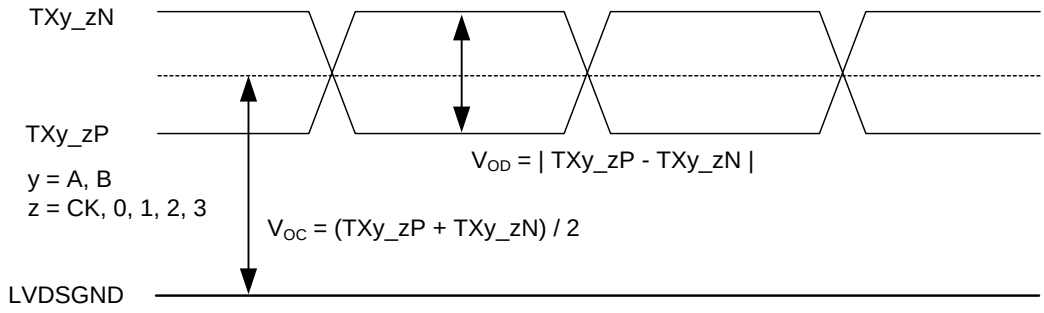


Figure 4. LVDS Transmitter DC Characteristics

Electrical Characteristics - continued

LVDS AC Characteristics

Table 4. LVDS Receiver Switching Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
LVDS Input Clock Frequency (☆)	f_{IN}	20	-	150	MHz	*(Note 13)*
LVDS Input Clock Period	t_{RCIP}	6.66	-	50	ns	
Differential Input Clock High Time	t_{RCIH}	$2\frac{t_{RCIP}}{7}$	-	$5\frac{t_{RCIP}}{7}$	ns	(Figure 5)
Differential Input Clock Low Time	t_{RCIL}	$2\frac{t_{RCIP}}{7}$	-	$5\frac{t_{RCIP}}{7}$	ns	(Figure 5)
Receiver Skew Margin	t_{SK}	0	-	0.60	ns	f_{IN} = 65 MHz
		0	-	0.50	ns	f_{IN} = 75 MHz
		0	-	0.25	ns	f_{IN} = 112 MHz
		0	-	0.22	ns	f_{IN} = 135 MHz
		0	-	0.15	ns	f_{IN} = 150 MHz
Input Data Position 1	t_{RIP1}	$-t_{SK}$	0	$+t_{SK}$	ns	(Figure 6)
Input Data Position 0	t_{RIP0}	$\frac{t_{RCIP}}{7} - t_{SK}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{SK}$	ns	(Figure 6)
Input Data Position 6	t_{RIP6}	$2\frac{t_{RCIP}}{7} - t_{SK}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{SK}$	ns	(Figure 6)
Input Data Position 5	t_{RIP5}	$3\frac{t_{RCIP}}{7} - t_{SK}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{SK}$	ns	(Figure 6)
Input Data Position 4	t_{RIP4}	$4\frac{t_{RCIP}}{7} - t_{SK}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{SK}$	ns	(Figure 6)
Input Data Position 3	t_{RIP3}	$5\frac{t_{RCIP}}{7} - t_{SK}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{SK}$	ns	(Figure 6)
Input Data Position 2	t_{RIP2}	$6\frac{t_{RCIP}}{7} - t_{SK}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{SK}$	ns	(Figure 6)
Input Modulation Frequency	f_{IMOD}	30	-	300	kHz	
Input Modulation Ratio	r_{IMOD}	-3.0	-	+3.0	%	
Skew Time of RXA_CK and RXB_CK	t_{CK12}	$-0.3 \times t_{RCIP}$	-	$+0.3 \times t_{RCIP}$	ns	(Figure 7)
DE Input Period	t_{DEINT}	$4t_{RCIP}$	$t_{RCIP} \times (2n)$ n = Integer	-	ns	(Figure 11)
DE Input High Time	t_{DEH}	$2t_{RCIP}$	-	-	ns	
DE Input Low Time	t_{DEL}	$2t_{RCIP}$	-	-	ns	

(Note 13) (☆): Special Characteristics

LVDS AC Characteristics - continued

Table 5. LVDS Transmitter Switching Characteristics (R_L = 100 Ω, C_L = 5 pF)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
LVDS Output Clock Frequency (☆)	f_{OUT}	20	-	135	MHz	*(Note 14)*
LVDS Output Clock Period	t_{TCOP}	7.4	-	50	ns	
Differential Output Setup Time	t_{TSUP}	-	-	170	ps	f_{OUT} = 135 MHz
Differential Output Hold Time	t_{THLD}	-	-	170	ps	f_{OUT} = 135 MHz
LVDS Transition Time	t_{LVT}	-	-	0.5	ns	(Figure 8)
Output Data Position 1	t_{TOP1}	$-t_{THLD}$	0	$+t_{TSUP}$	ns	(Figure 9)
Output Data Position 0	t_{TOP0}	$\frac{t_{TCOP}}{7} - t_{THLD}$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + t_{TSUP}$	ns	(Figure 9)
Output Data Position 6	t_{TOP6}	$2\frac{t_{TCOP}}{7} - t_{THLD}$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + t_{TSUP}$	ns	(Figure 9)
Output Data Position 5	t_{TOP5}	$3\frac{t_{TCOP}}{7} - t_{THLD}$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + t_{TSUP}$	ns	(Figure 9)
Output Data Position 4	t_{TOP4}	$4\frac{t_{TCOP}}{7} - t_{THLD}$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + t_{TSUP}$	ns	(Figure 9)
Output Data Position 3	t_{TOP3}	$5\frac{t_{TCOP}}{7} - t_{THLD}$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + t_{TSUP}$	ns	(Figure 9)
Output Data Position 2	t_{TOP2}	$6\frac{t_{TCOP}}{7} - t_{THLD}$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + t_{TSUP}$	ns	(Figure 9)
PLL Lock Up Time	t_{PLL}	-	-	100	µs	(Figure 10)

(Note 14) (☆): Special Characteristics

Electrical Characteristics - continued

LVDS AC Timing Diagrams

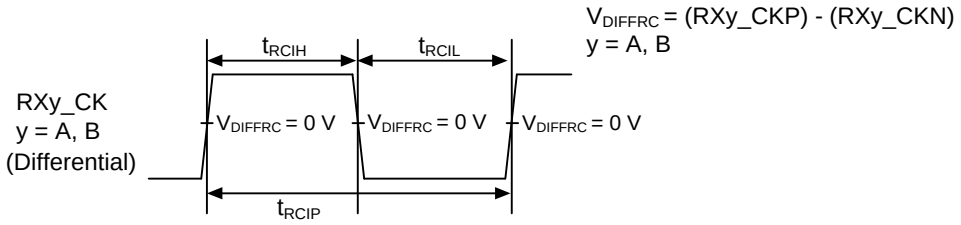


Figure 5. Differential Input Clock

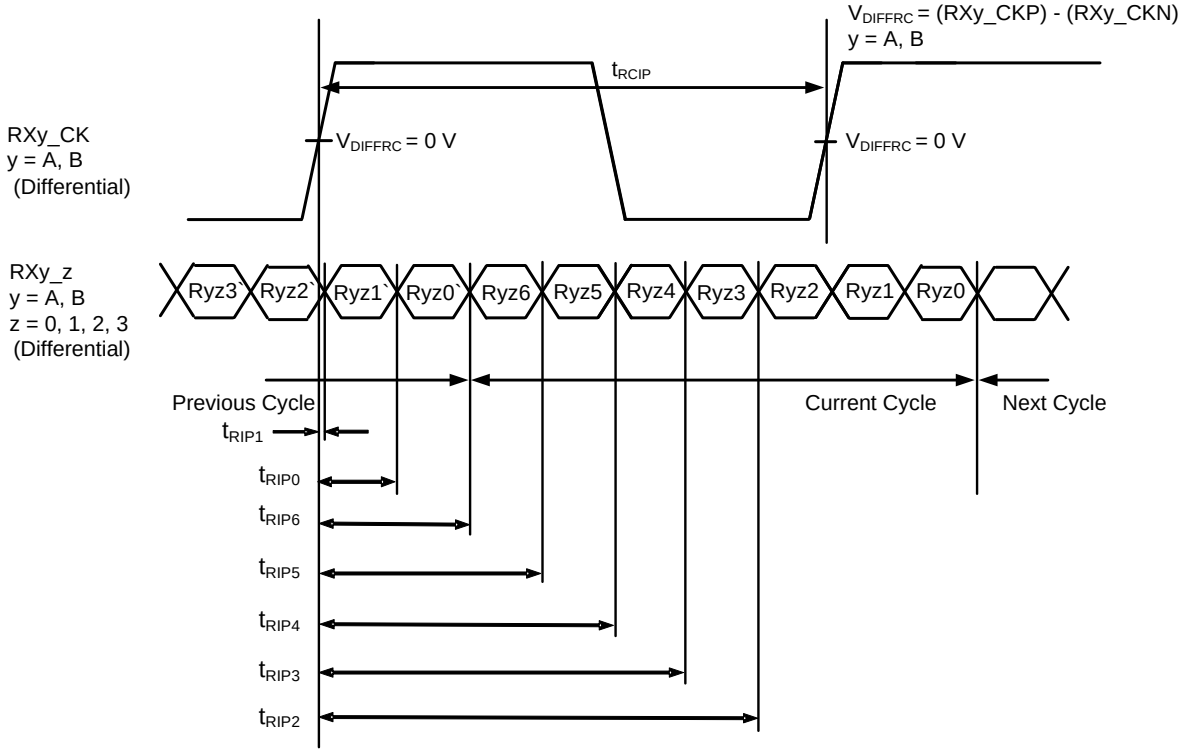


Figure 6. LVDS Receiver AC Timing Diagrams (1)

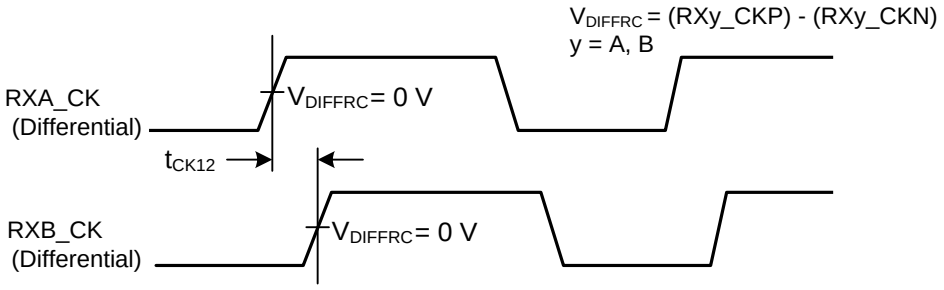


Figure 7. LVDS Receiver AC Timing Diagrams (2)

LVDS AC Timing Diagrams - continued

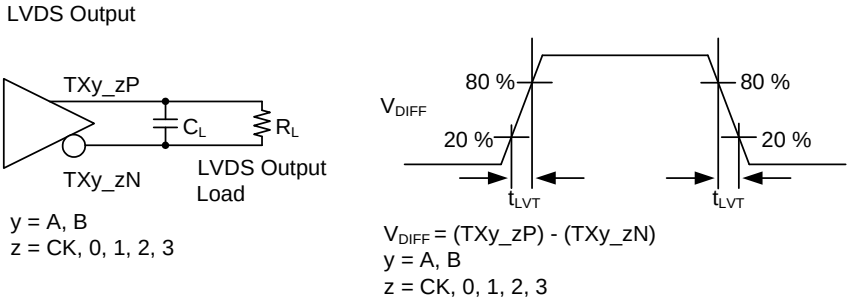


Figure 8. LVDS Transmitter AC Timing Diagrams (1)

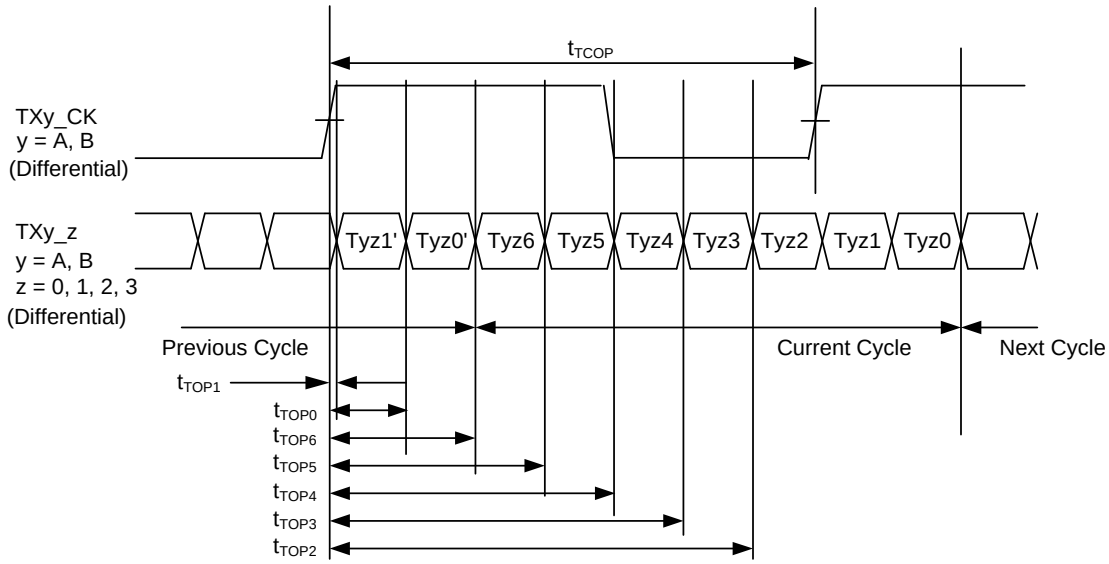


Figure 9. LVDS Transmitter AC Timing Diagrams (2)

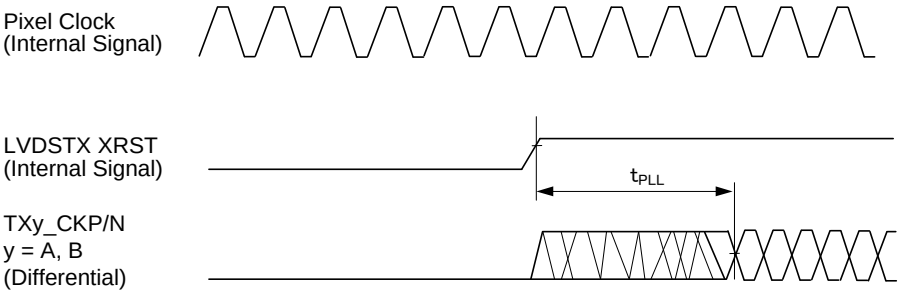


Figure 10. PLL Lock Up Time

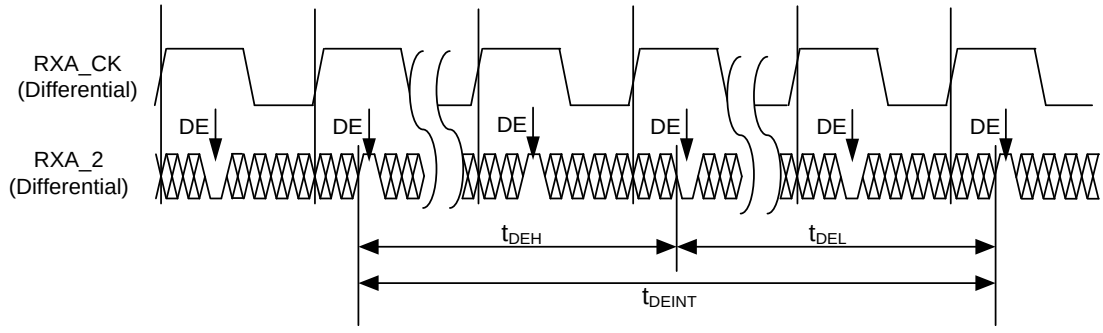


Figure 11. DE Input Timing

Electrical Characteristics - continued

Spread Spectrum Clock Generator (SSCG) Specification

Table 6. SSCG Specification

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Clock Frequency1 (LVDS)	f_{IN_LV1}	40	-	150	MHz	Single-in Mode
Input Clock Frequency2 (LVDS)	f_{IN_LV2}	20	-	120	MHz	Dual-in Mode
Input Clock Frequency (SSCG)	f_{IN_SS}	20	-	120	MHz	In Single-in Mode: $f_{IN\_SS} = 1/2 \times f_{IN\_LV1}$ In Dual-in Mode: $f_{IN\_SS} = f_{IN\_LV2}$
Output Modulation Frequency	f_{OMOD}	30	-	300	kHz	
Output Modulation Ratio *(Note 15)*	r_{OMOD}	-3.0	-	+3.0	%	
SSCG PLL Lock Up Time	t_{PLL_SS}	-	-	100	µs	

(Note 15) The output modulation ratio of up to 3% includes input modulation ratio.

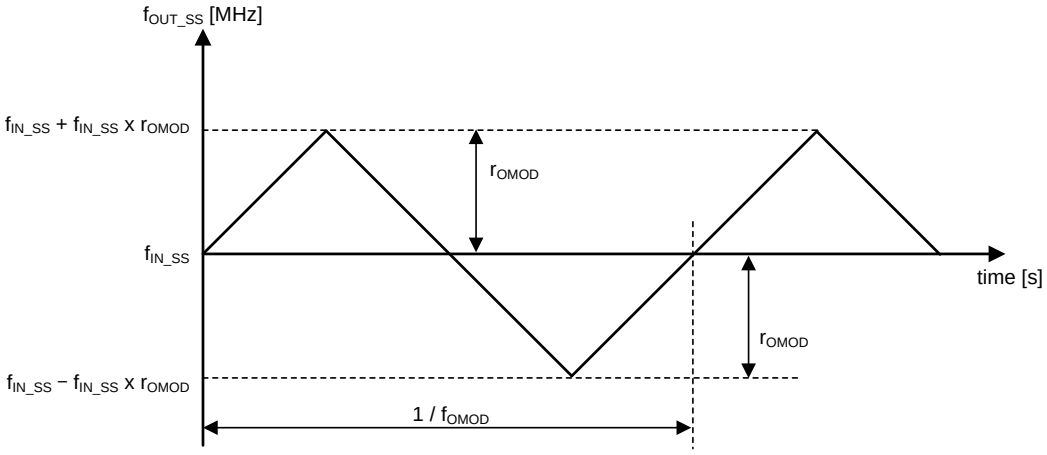


Figure 12. SSCG Profile

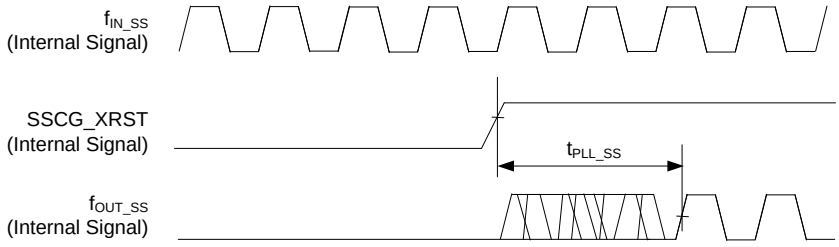


Figure 13. SSCG Lock Up Time

Electrical Characteristics - continued

Internal OSC (Oscillator) Specification

Table 7. Internal OSC Specification

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Clock Frequency*(Note 16)*	f_{OUT1}	27	30	33	MHz	-
	f_{OUT2}	36	40	44	MHz	-
	f_{OUT3}	45	50	55	MHz	-
	f_{OUT4}	54	60	66	MHz	(Default)
	f_{OUT5}	63	70	77	MHz	-
	f_{OUT6}	72	80	88	MHz	-
Power On Settling Time	t_{STABLE}	-	-	100	µs	-

(Note 16) Set it on the parameter of Flash Memory.

SPI Specification

Table 8. SPI AC Characteristics

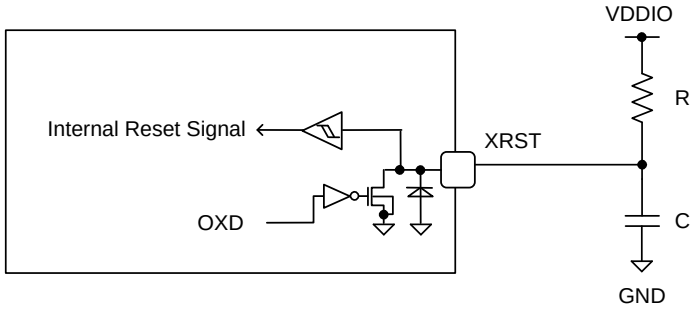
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
SPI Master Clock Frequency	f_{SMC}	2.8	-	44.0	MHz	-
SPI Slave Clock Frequency	f_{SSC}	-	-	20.0	MHz	-

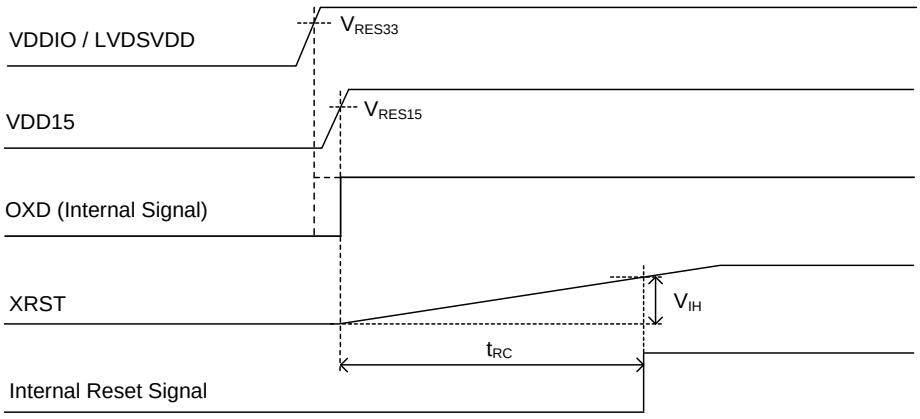
Electrical Characteristics - continued

Voltage Detector Specification

Table 9. Voltage Detector DC Specification

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Detect Voltage for VDD_{15}	V_{DET15}	0.50	0.70	0.90	V	-
Release Voltage for VDD_{15}	V_{RES15}	0.70	0.90	1.10	V	-
Hysteresis for VDD_{15}	V_{HYS15}	-	0.20	-	V	$V_{HYS15} = V_{RES15} - V_{DET15}$
Detect Voltage for VDD_{33}	V_{DET33}	1.45	1.65	1.85	V	-
Release Voltage for VDD_{33}	V_{RES33}	1.70	1.90	2.10	V	-
Hysteresis for VDD_{33}	V_{HYS33}	-	0.25	-	V	$V_{HYS33} = V_{RES33} - V_{DET33}$





t_{RC} : Depend on external R,C value.
V_{IH} : I/O high level input voltage.

Figure 14. Reset Signal Release Timing

Table 10. Voltage Detector External RC Value

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
RC Time Constant*(Note 17)*	t_{RC}	1	-	-	ms	-
External Resistor	R	10.0	-	20.0	kΩ	-
External Capacitor	C	0.1	-	5.0	μF	-

(Note 17) In case of VDD_{15} and VDD_{33} rise slowly, please consider the t_{RC} value. ($t_{RC} >> t_{VDD33\_R}, t_{VDD15\_R}$)

Electrical Characteristics - continued

Supply Current (OSD Gen2 Function is Disable)

Table 11-1. VDD_{33} Supply Current (R_L = 100 Ω, C_L = 5 pF)

Parameter	Symbol	Limit			Unit	Conditions		
		Min	Typ	Max				
VDD_{33} Supply Current Worst Case Pattern	I_{TCCW33}	-	116	150	mA	Dual-in / Dual-out	VOD = 200 mV	f_{IN} = 120 MHz f_{OUT} = 120 MHz
		-	90	130	mA	Single-in / Dual-out		f_{IN} = 150 MHz f_{OUT} = 75 MHz
		-	86	120	mA	Dual-in / Single-out		f_{IN} = 67.5 MHz f_{OUT} = 135 MHz
		-	118	150	mA	Single-in / Distribution		f_{IN} = 135 MHz f_{OUT} = 135 MHz
		-	81	120	mA	Single-in / Single-out		f_{IN} = 135 MHz f_{OUT} = 135 MHz
		-	146	180	mA	Dual-in / Dual-out	VOD = 350 mV	f_{IN} = 120 MHz f_{OUT} = 120 MHz
		-	120	160	mA	Single-in / Dual-out		f_{IN} = 150 MHz f_{OUT} = 75 MHz
		-	100	140	mA	Dual-in / Single-out		f_{IN} = 67.5 MHz f_{OUT} = 135 MHz
		-	148	180	mA	Single-in / Distribution		f_{IN} = 135 MHz f_{OUT} = 135 MHz
		-	95	140	mA	Single-in / Single-out		f_{IN} = 135 MHz f_{OUT} = 135 MHz
Power Down Current	I_{TCCS33}	-	1.8	-	mA	XRST = L		

Table 11-2. VDD_{15} Supply Current (R_L = 100 Ω, C_L = 5 pF)

Parameter	Symbol	Limit			Unit	Conditions		
		Min	Typ	Max				
VDD_{15} Supply Current Worst Case Pattern	I_{TCCW15}	-	125	150	mA	Dual-in / Dual-out	VOD = 200 mV or 350 mV	f_{IN} = 120 MHz f_{OUT} = 120 MHz
		-	92	115	mA	Single-in / Dual-out		f_{IN} = 150 MHz f_{OUT} = 75 MHz
		-	94	115	mA	Dual-in / Single-out		f_{IN} = 67.5 MHz f_{OUT} = 135 MHz
		-	87	110	mA	Single-in / Distribution		f_{IN} = 135 MHz f_{OUT} = 135 MHz
		-	87	110	mA	Single-in / Single-out		f_{IN} = 135 MHz f_{OUT} = 135 MHz
Power Down Current	I_{TCCS15}	-	10	-	mA	XRST = L		

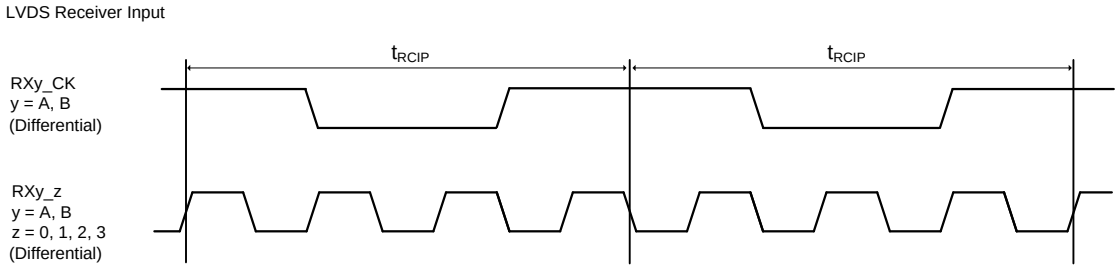
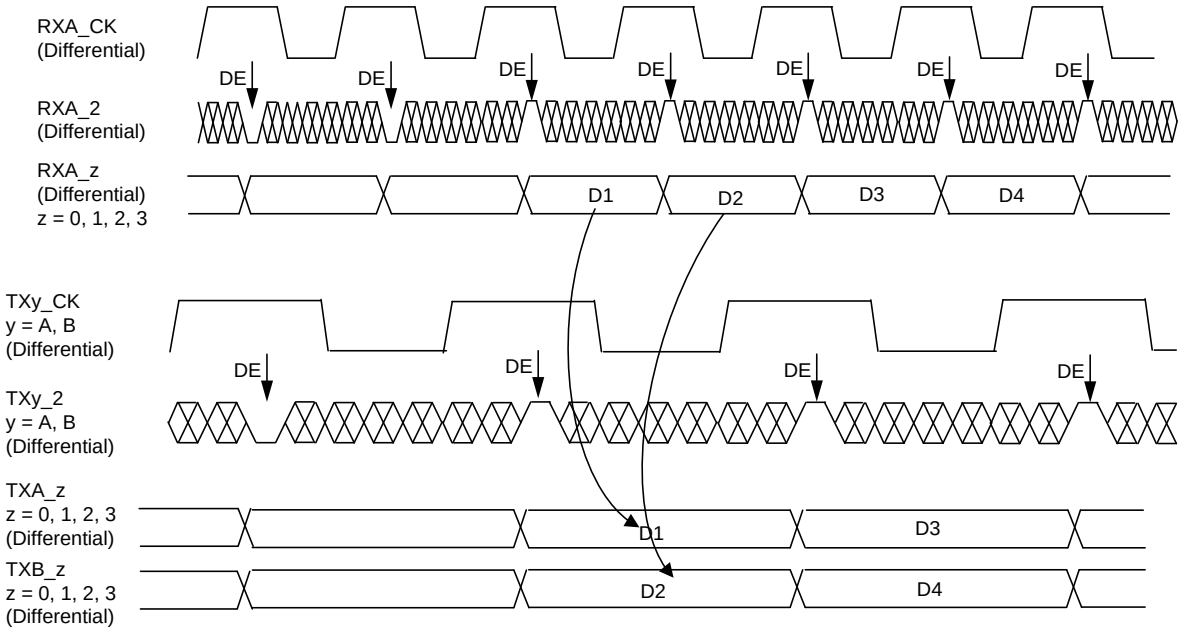


Figure 15. Worst Case Pattern (Maximum Power Condition)

Assignment from Single Data to Dual Data



(Note 18) Regardless of the data latency

Figure 16. Assignment from Single Data to Dual Data

LVDS In / Out Mode Data Mapping

Figure 17-1 to 17-5 show LVDS in / out mode data mapping.
Data of data11 level can be set by register LVTX_CTRL_LEVEL.

Dual-in / Dual-out Mode (LVRX_SINGLE = L / LVTX_SINGLE = L)

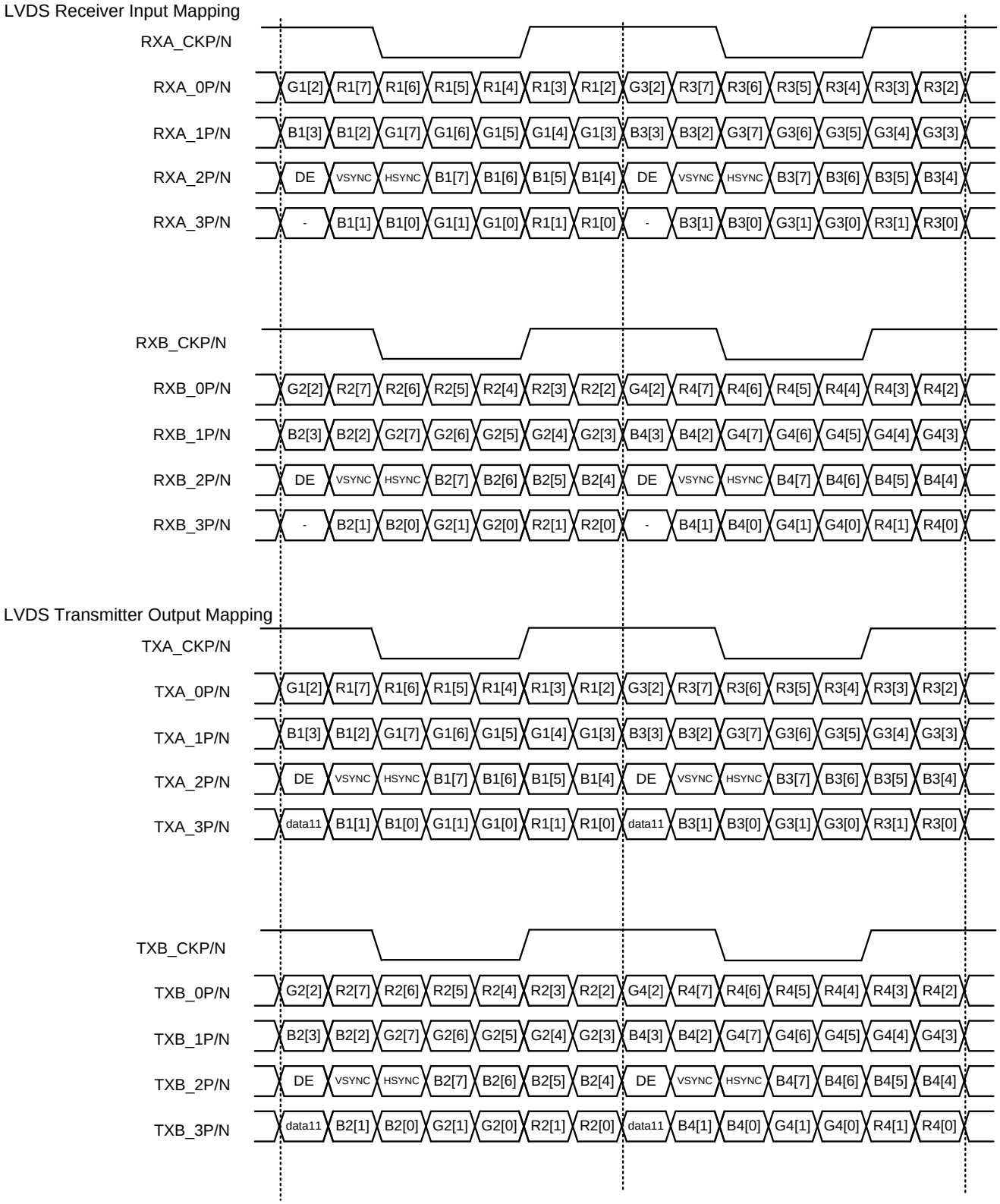
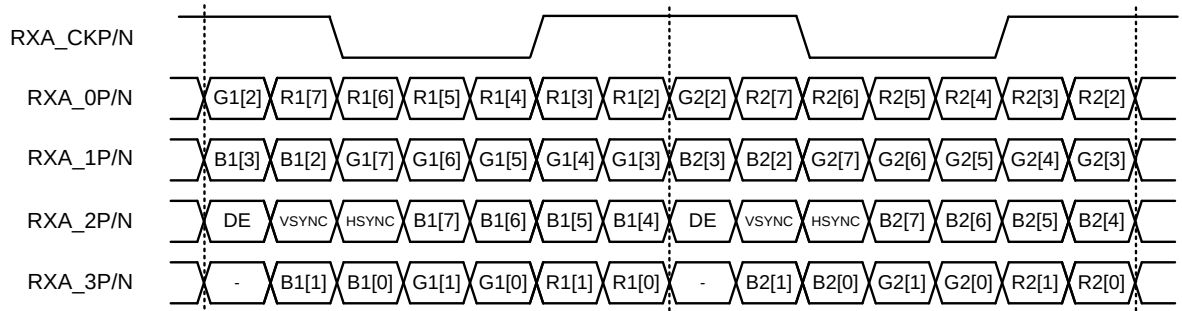


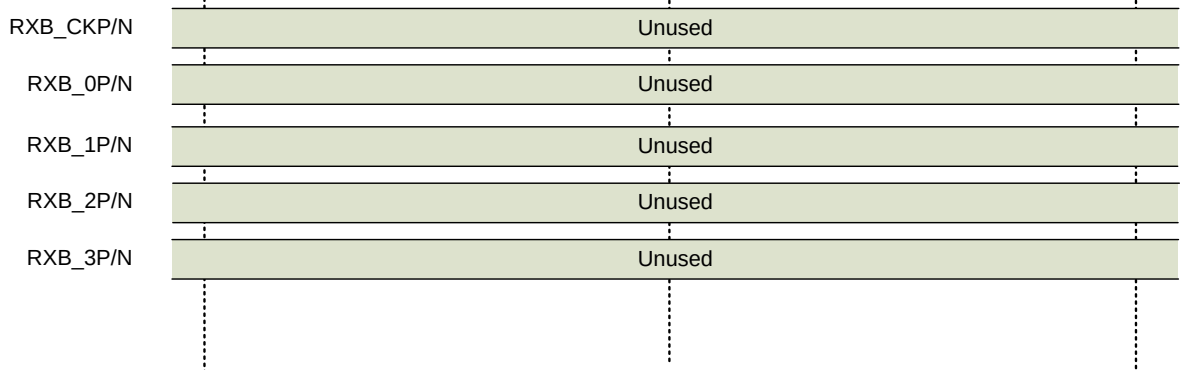
Figure 17-1. Data Mapping for Dual-in / Dual-out Mode

LVDS In / Out Mode Data Mapping - continued

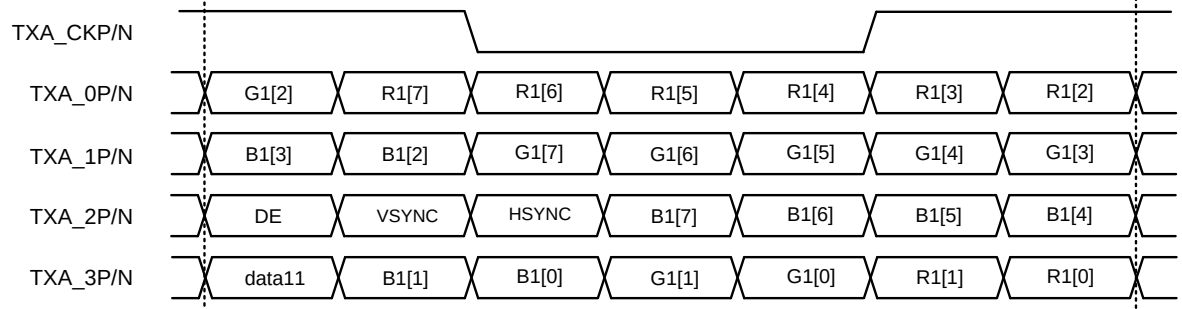
Single-in / Dual-out Mode (LVRX_SINGLE = H / LVTX_SINGLE = L)

LVDS Receiver Input Mapping





LVDS Transmitter Output Mapping



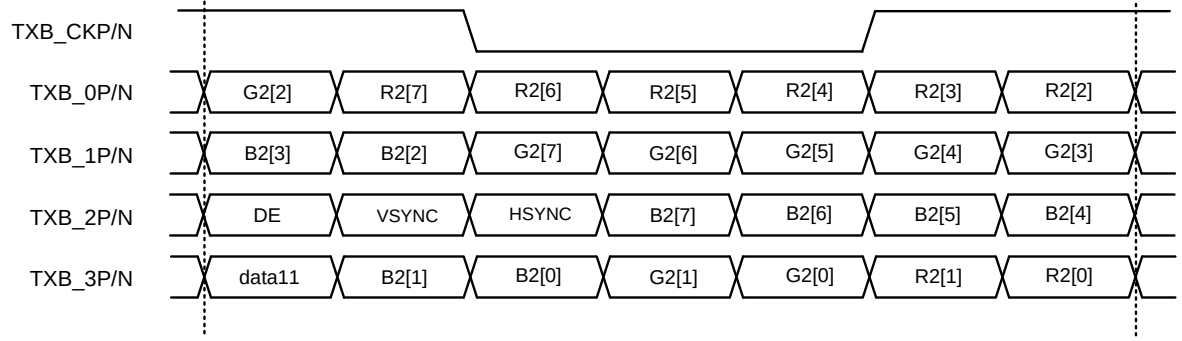


Figure 17-2. Data Mapping for Single-in / Dual-out Mode

LVDS In / Out Mode Data Mapping - continued

Dual-in / Single-out Mode (LVRX_SINGLE = L / LVTX_SINGLE = H / LVTX_SINGLE_DIST = L)

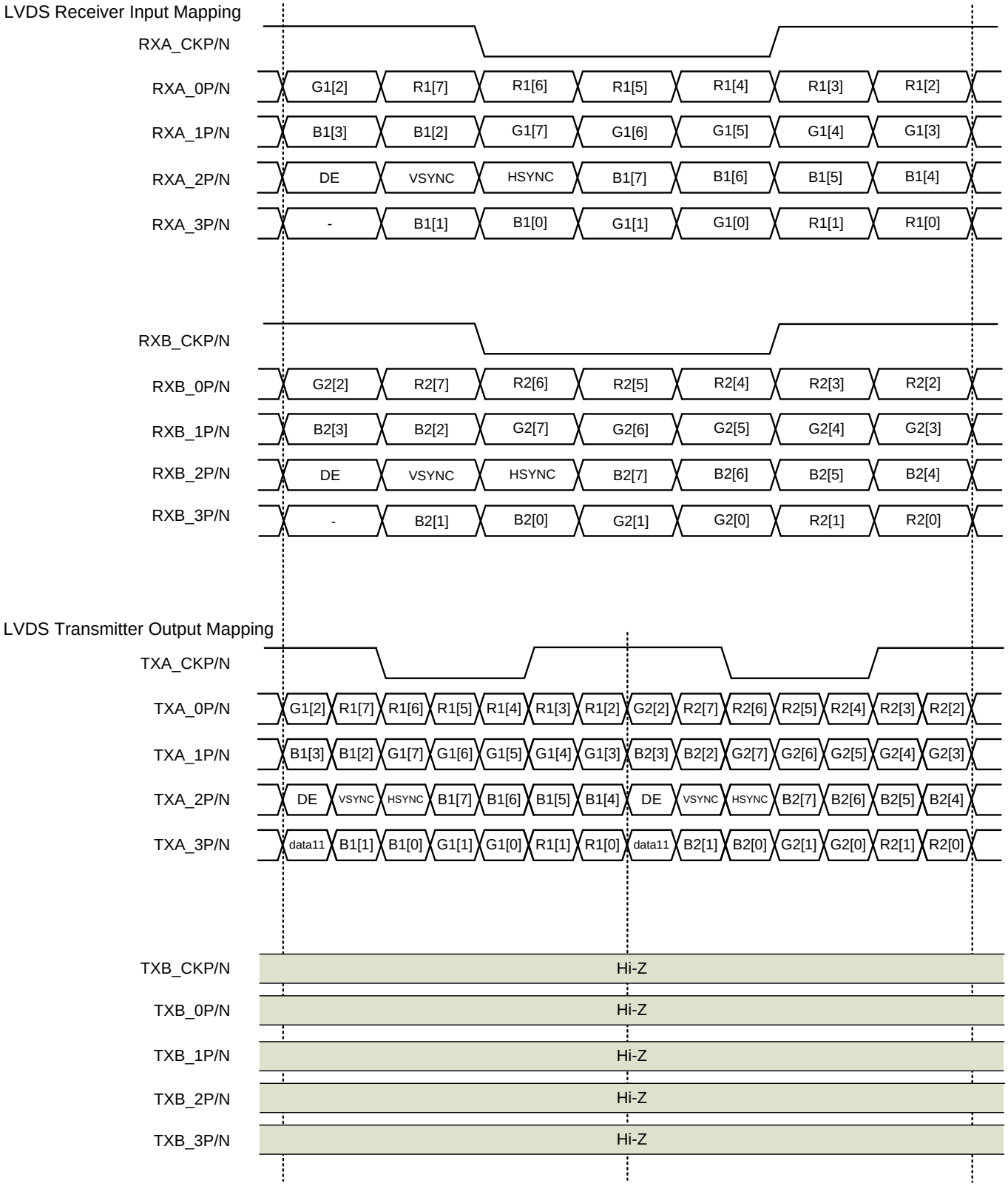


Figure 17-3. Data Mapping for Dual-in / Single-out Mode

LVDS In / Out Mode Data Mapping - continued

Single-in / Distribution Mode (LVRX_SINGLE = H / LVTX_SINGLE = H / LVTX_SINGLE_DIST = H)

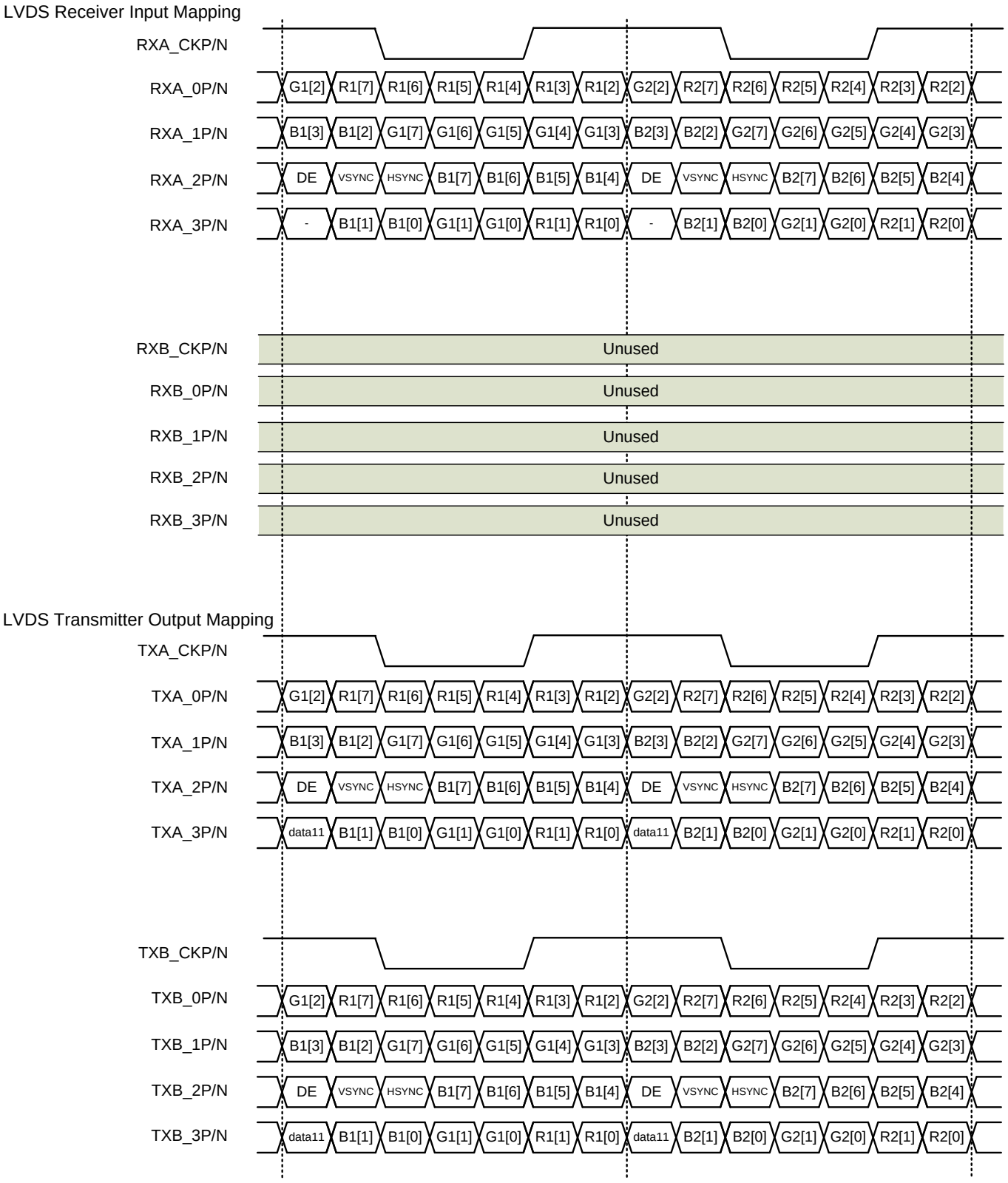


Figure 17-4. Data Mapping for Single-in / Distribution

LVDS In / Out Mode Data Mapping - continued

Single-in / Single-out Mode (LVRX_SINGLE = H / LVTX_SINGLE = H / LVTX_SINGLE_DIST = L)

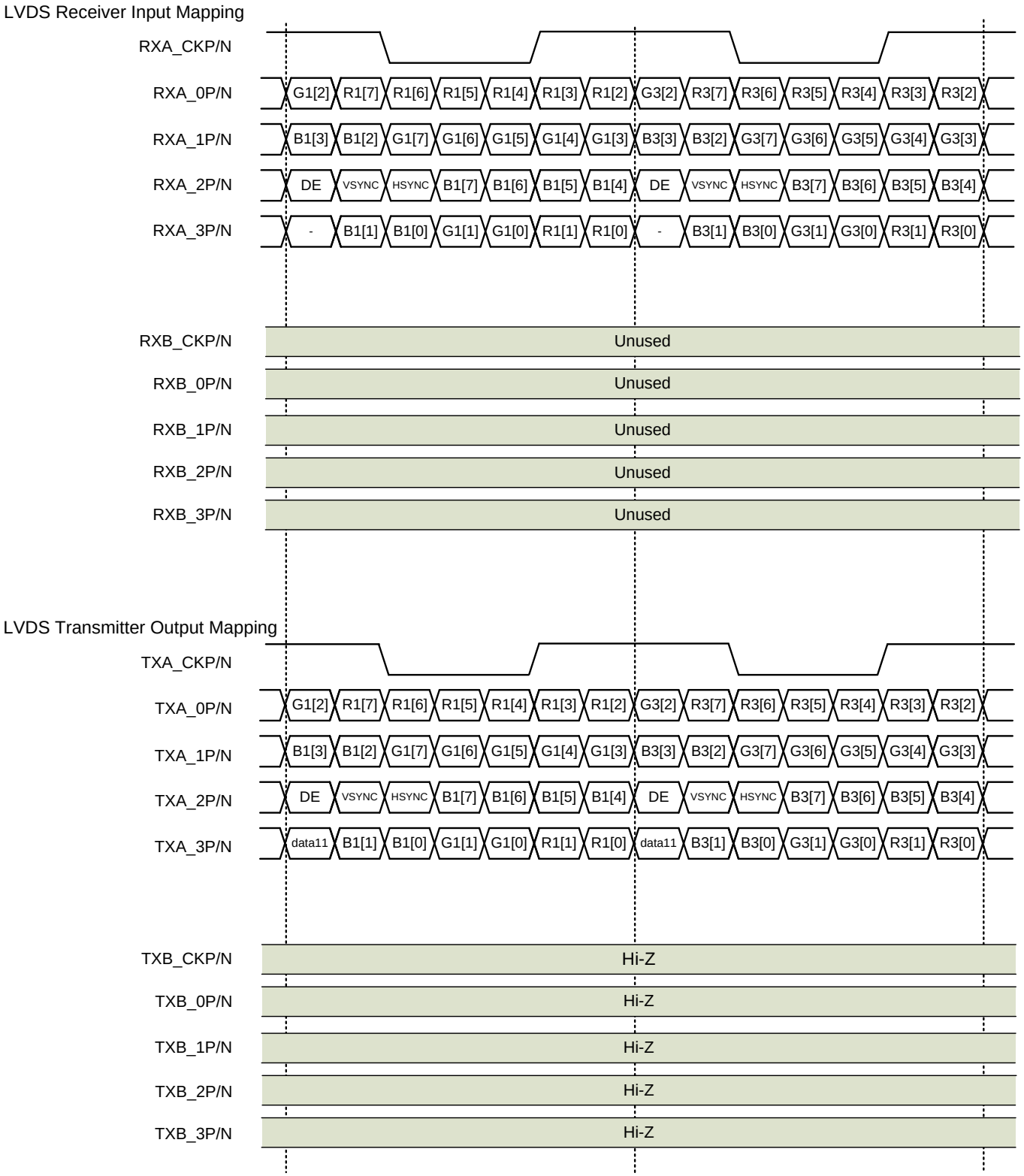


Figure 17-5. Data Mapping for Single-in / Single-out Mode (Select LVDS Receiver 1st Link Data)

LVDS Receiver Pin Function

Table 12 and Table 13 show the LVDS receiver pin functions of Single-in mode and Dual-in mode.

LVDS Receiver Single-in Mode

Table 12-1. LVDS Receiver Pin Function of Single-in Mode (LVRX_6BIT = L)

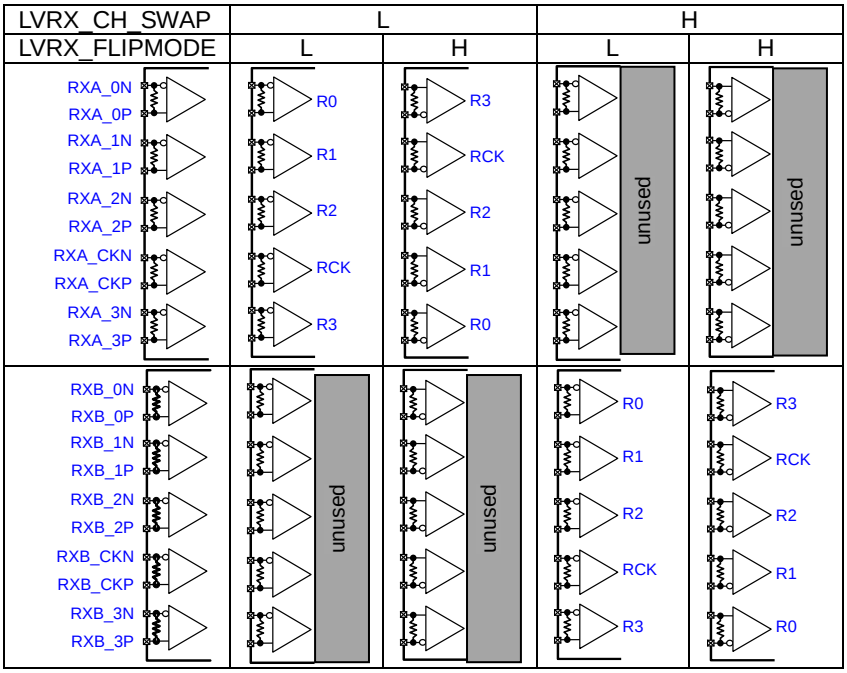
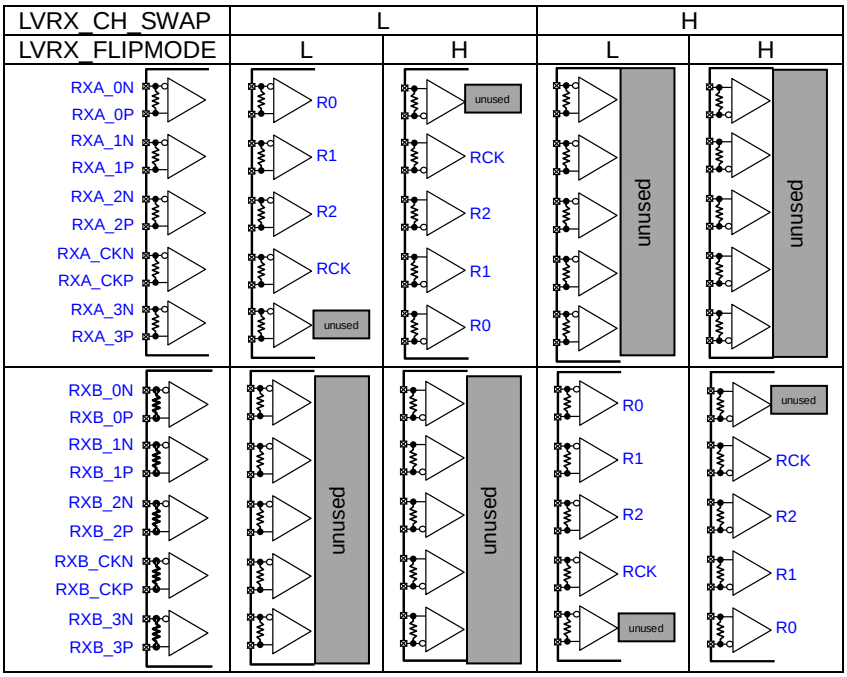


Table 12-2. LVDS Receiver Pin Function of Single-in Mode (LVRX_6BIT = H)



LVDS Receiver Pin Function - continued

LVDS Receiver Dual-in Mode

Table 13-1. LVDS Receiver Pin Function of Dual-in Mode (LVRX_6BIT = L)

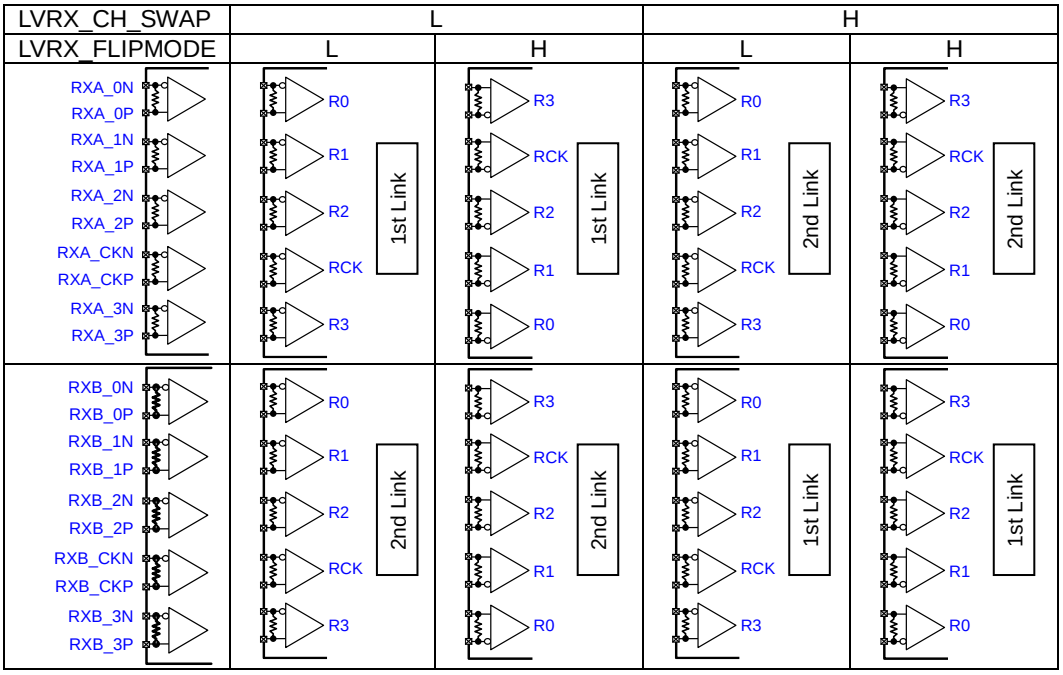
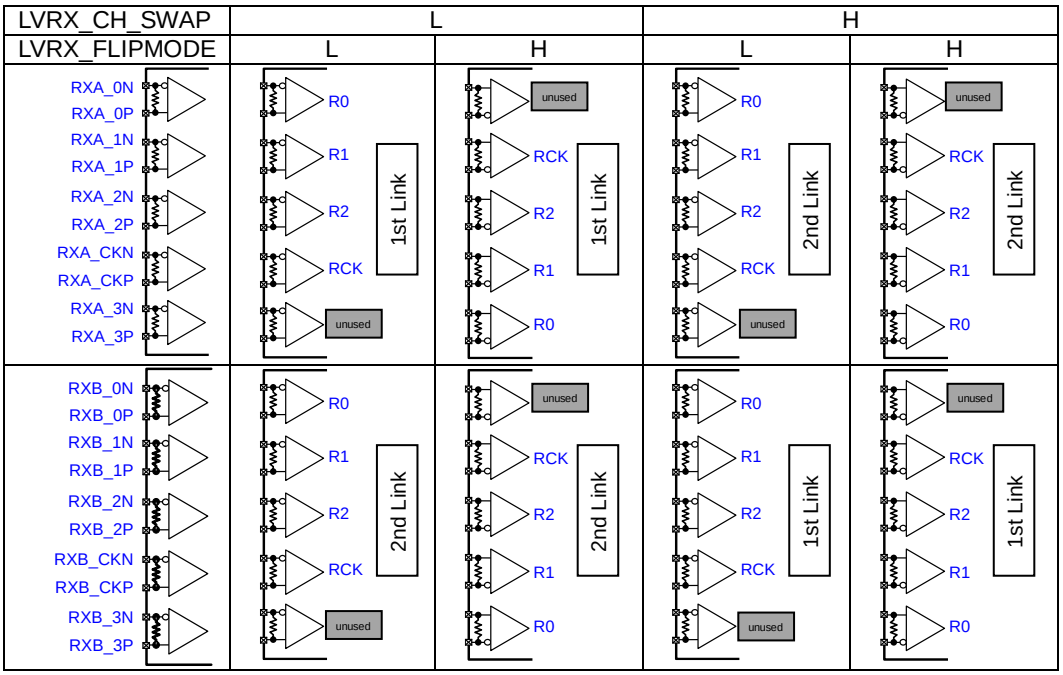


Table 13-2. LVDS Receiver Pin Function of Dual-in Mode (LVRX_6BIT = H)



LVDS Transmitter Pin Function

Table 14 and Table 15 show the LVDS transmitter pin functions of Single-out mode and Dual-out mode.

LVDS Transmitter Single-out Mode

Table 14-1. LVDS Transmitter Pin Function of Single-out Mode (LVTX_6BIT = L)

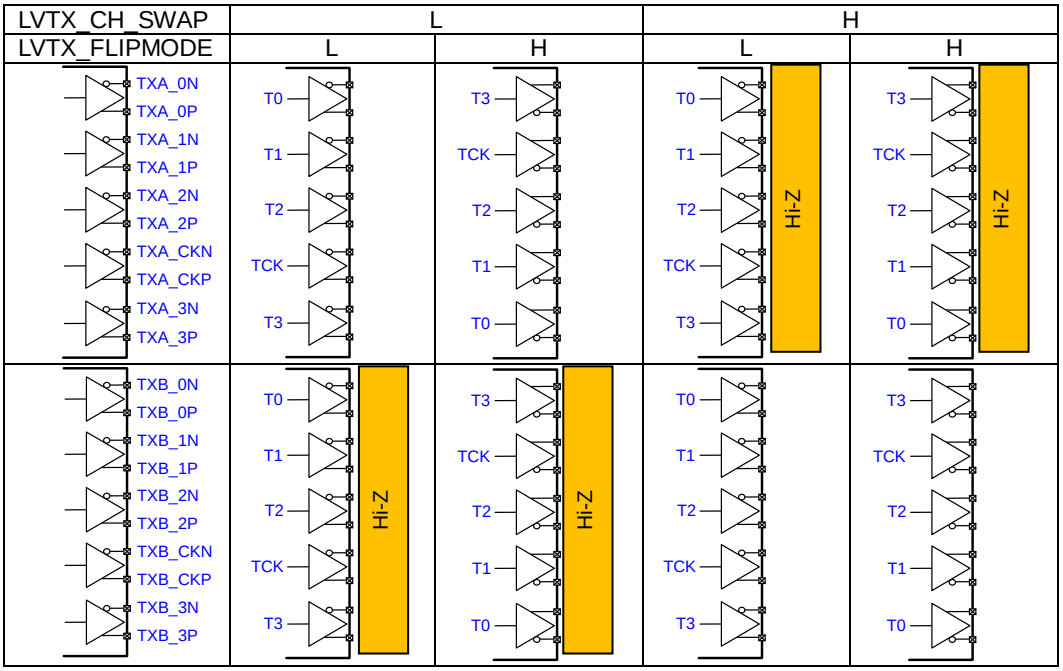
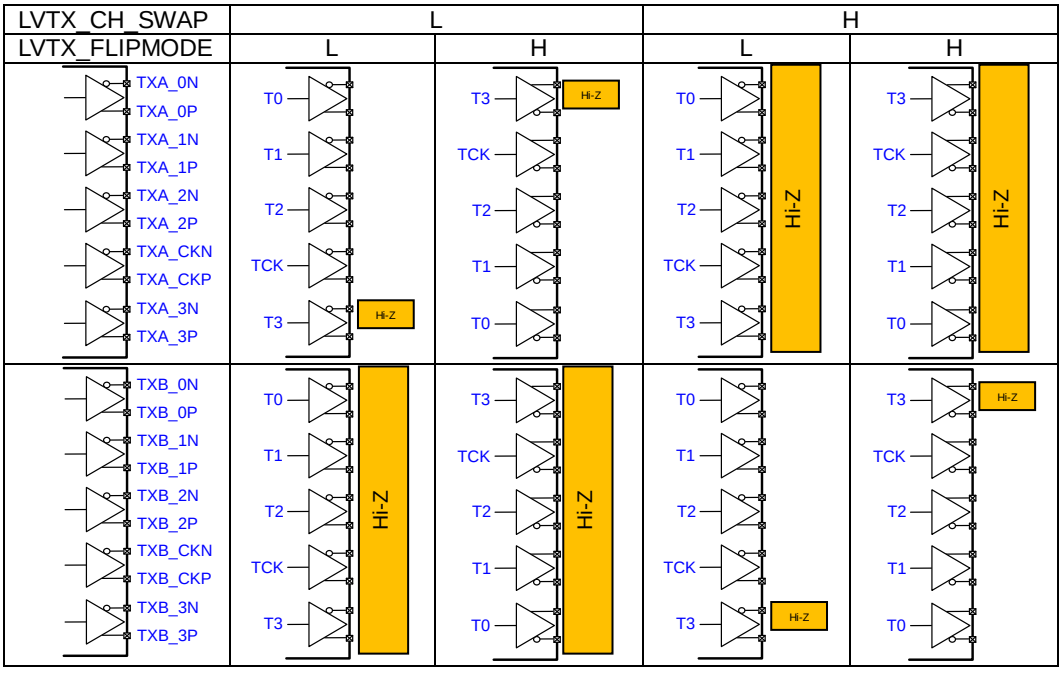


Table 14-2. LVDS Transmitter Pin Function of Single-out Mode (LVTX_6BIT = H)



LVDS Transmitter Pin Function - continued

LVDS Transmitter Dual-out Mode

Table 15-1. LVDS Transmitter Pin Function of Dual-out Mode (LVTX_6BIT = L)

LVTX_CH_SWAP	L		H	
LVTX_FLIPMODE	L	H	L	H
TXA_0N TXA_0P TXA_1N TXA_1P TXA_2N TXA_2P TXA_CKN TXA_CKP TXA_3N TXA_3P	1st Link: T0, T1, T2, TCK, T3	1st Link: T3, TCK, T2, T1, T0	2nd Link: T0, T1, T2, TCK, T3	2nd Link: T3, TCK, T2, T1, T0
TXB_0N TXB_0P TXB_1N TXB_1P TXB_2N TXB_2P TXB_CKN TXB_CKP TXB_3N TXB_3P	2nd Link: T0, T1, T2, TCK, T3	2nd Link: T3, TCK, T2, T1, T0	1st Link: T0, T1, T2, TCK, T3	1st Link: T3, TCK, T2, T1, T0

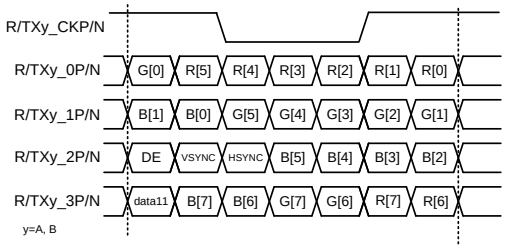
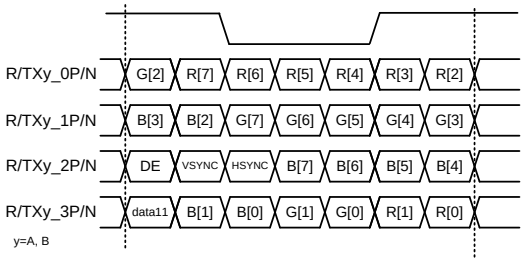
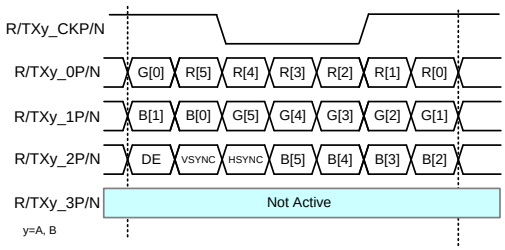
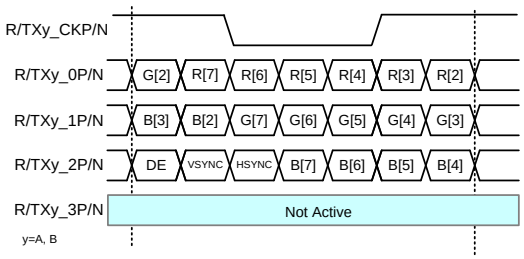
Table 15-2. LVDS Transmitter Pin Function of Dual-out Mode (LVTX_6BIT = H)

LVTX_CH_SWAP	L		H	
LVTX_FLIPMODE	L	H	L	H
TXA_0N TXA_0P TXA_1N TXA_1P TXA_2N TXA_2P TXA_CKN TXA_CKP TXA_3N TXA_3P	1st Link: T0, T1, T2, TCK, T3 (Hi-Z)	1st Link: T3 (Hi-Z), TCK, T2, T1, T0	2nd Link: T0, T1, T2, TCK, T3 (Hi-Z)	2nd Link: T3 (Hi-Z), TCK, T2, T1, T0
TXB_0N TXB_0P TXB_1N TXB_1P TXB_2N TXB_2P TXB_CKN TXB_CKP TXB_3N TXB_3P	2nd Link: T0, T1, T2, TCK, T3 (Hi-Z)	2nd Link: T3 (Hi-Z), TCK, T2, T1, T0	1st Link: T0, T1, T2, TCK, T3 (Hi-Z)	1st Link: T3 (Hi-Z), TCK, T2, T1, T0

LVDS Mapping Function

Table 16 shows the LVDS Mapping (VESA / JEIDA) Control.
Data of data11 level can be set by register LVTX_CTRL_LEVEL.

Table 16. LVDS Mapping Mode (VESA / JEIDA)

Register: LVRX_MAP_SEL LVTX_MAP_SEL		L	H
Mapping		VESA	JEIDA
Register: LVRX_6BIT LVTX_6BIT	L		
	H		

Timing Chart

Power On/Off Sequence

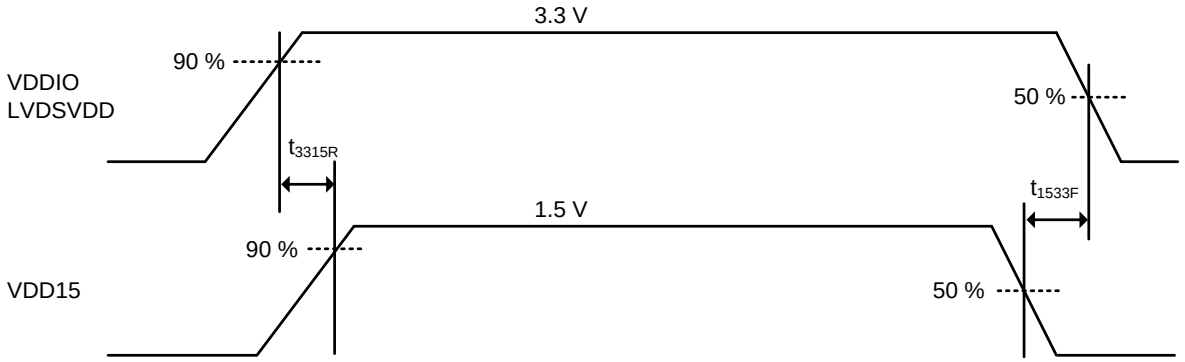


Figure 18. Power Supply Sequence

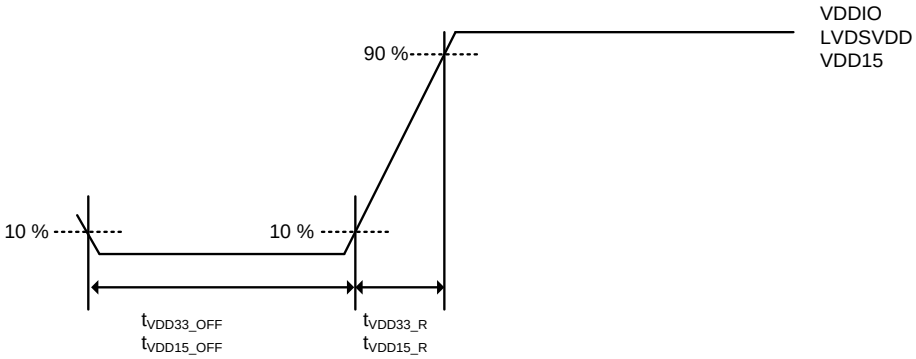


Figure 19. Power Supply Rise and Fall Timing

Table 17. Power Supply Timing

Parameter	Symbol	Min	Typ	Max	Unit
VDD_{33} to VDD_{15} Rise Delay Time*(Note 19)*	t_{3315R}	0	-	-	µs
VDD_{15} to VDD_{33} Fall Delay Time*(Note 19)*	t_{1533F}	0	-	-	µs
VDD_{33} Rise Time*(Note 19)* (*Note 20*)	t_{VDD33_R}	-	-	50	ms
VDD_{15} Rise Time*(Note 20)*	t_{VDD15_R}	-	-	50	ms
VDD_{33} Off Time*(Note 19)*	t_{VDD33_OFF}	100	-	-	ms
VDD_{15} Off Time	t_{VDD15_OFF}	100	-	-	ms

(Note 19) VDD_{33}: VDDIO, LVDSVDD

(Note 20) In case of VDD_{15} and VDD_{33} rise slowly, please consider the t_{RC} value described on “Voltage Detector Specification”. (t_{RC} >> t_{VDD33_R}, t_{VDD15_R})

AGING Function

AGING pattern, sequence can be set by register setting in IC.

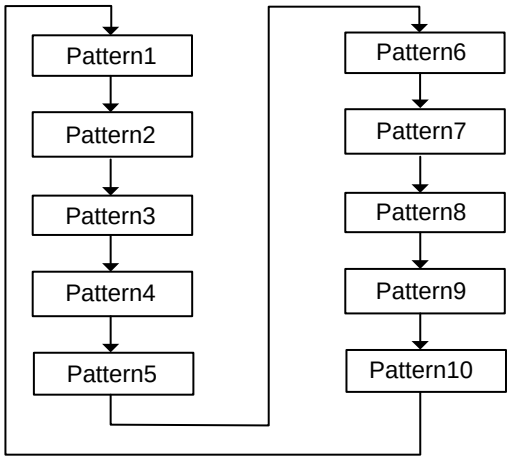


Figure 20. AGING Mode Pattern Sequence

Table 18. AGING Mode Pattern Example

White	Black	Red	Green	Blue	Cyan
Magenta	Yellow	V Gray	V Gray Red	V Gray Green	V Gray Blue
H Color Bar (H Gray)	Outer Frame	Gray (127/255 Level)	H Gray	H Gray Red	H Gray Green
H Gray Blue	V Gray	V Gray Red	V Gray Green	V Gray Blue	Chess Pattern
Sub-pixel Check (Zoom)	2line Sub-pixel Check (Zoom)	2line +1 Sub-pixel Check (Zoom)	Pixel Check (Zoom)	V Color Bar (V Gray)	V Color Bar
Crosstalk Check1	Crosstalk Check2	H Linear Gradient Grey	Orientation Test	V Flicker Test	H Flicker Test

Fail Detect Function

This product supports Fail Detect Function.
"Detect Item" in the table shows fail condition which outputs to the FAIL_DET pin. (L: Fail Condition / H: Normal Condition).
The setting of each item is selected by register setting *(Note 21)*.
(Note 21) About the details for fail detect function, please refer to BU92RTF82_Application_Note.pdf

Table 19. Fail Detect Items

No.	Fail Category	Enable Control Register	Detect Item
(1)	System Fail	SYSTEM FAIL_EN	LVDS Input Clock Frequency, HS, VS, DE Term
(2)	ROM Fail	ROM_FAIL_EN	Flash Access Abort Error, SPI Master Checksum Error
(3)	SPI Fail	SPI_FAIL_EN	SPI Slave Timeout
(4)	Image Error	CRC_FAIL_EN FSAFETY_IRQ_EN	I-CRC Error *(Note 22)*, RGB-Sigma *(Note 22)*, Pixel Count *(Note 22)*
(5)	Full-Frame CRC *(Note 23)*	CRC_FAIL_EN FSAFETY_IRQ_EN	Frame CRC
	Frame Stop *(Note 23)*	CRC_FAIL_EN FSAFETY_IRQ_EN	Frame Stop
(6)	BDP *(Note 24)*	FSAFETY_IRQ_EN	BDP Command Error
(7)	IMC/OSD	FSAFETY_IRQ_EN	IMC, OSD Error

(Note 22) About the details for I-CRC, RGB-Sigma, Pixel Count function, please refer to UG301_Ver1.0_ImageChecker_Specifications.pdf
(Note 23) About the details for full-frame CRC, frame stop function, please refer to BU92RTF82_Application_Note.pdf
(Note 24) About the details for BDP function, please refer to UG401_BDP_Specifications.pdf.

CRC Function

This product supports CRC (Cyclic Redundancy Check) using CRC-16.
It is only performed on active pixels, and is calculated for each RGB color.
CRC verification area can be set by register setting in the IC.

This CRC-16 is generated per component, based on the following polynomial.
CRC-16 = $X^{16} + X^{15} + X^2 + 1$

User can read CRC value by SPI access, or send CRC expectation value by BDP function.

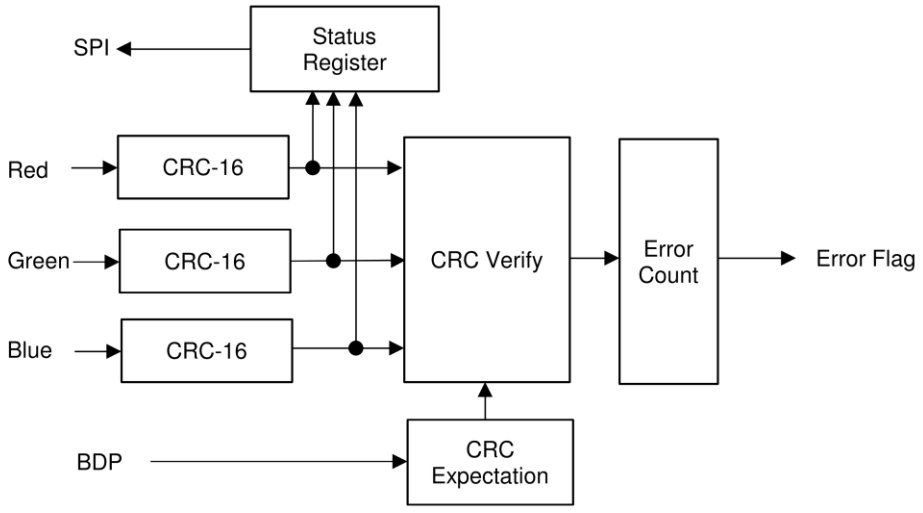


Figure 21. CRC Function

OSD Gen2 Function

OSD (On-Screen Display) Gen2 is the displaying character function.
The character size and position is selectable by register setting.

Table 20. OSD Gen2 Features

Character Font Example	
Max Characters Count	32
Character Size	M x N Dot (M,N: Every Character from 30 pixels to 255 pixels)

IMC (Image Comparison) Function

IMC detects the abnormality of the image data from input video interface by comparing the image data with the character data of OSD.
Detecting the mismatch of pixels, the IRQ (Interrupt request) is generated.

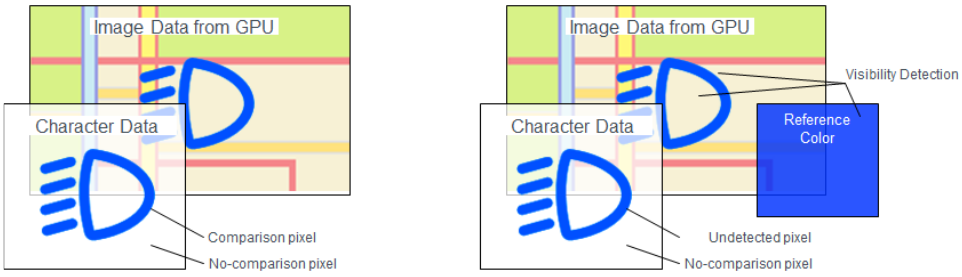


Figure 22. IMC (Image Comparison) Function

Application Examples

Dual-in / Dual-out Mode

LVDS Receiver: Dual Input (8 bits), LVDS Transmitter: Dual Output (8 bits)
VDD15 = 1.5 V, LVDSVDD = VDDIO = 3.3 V

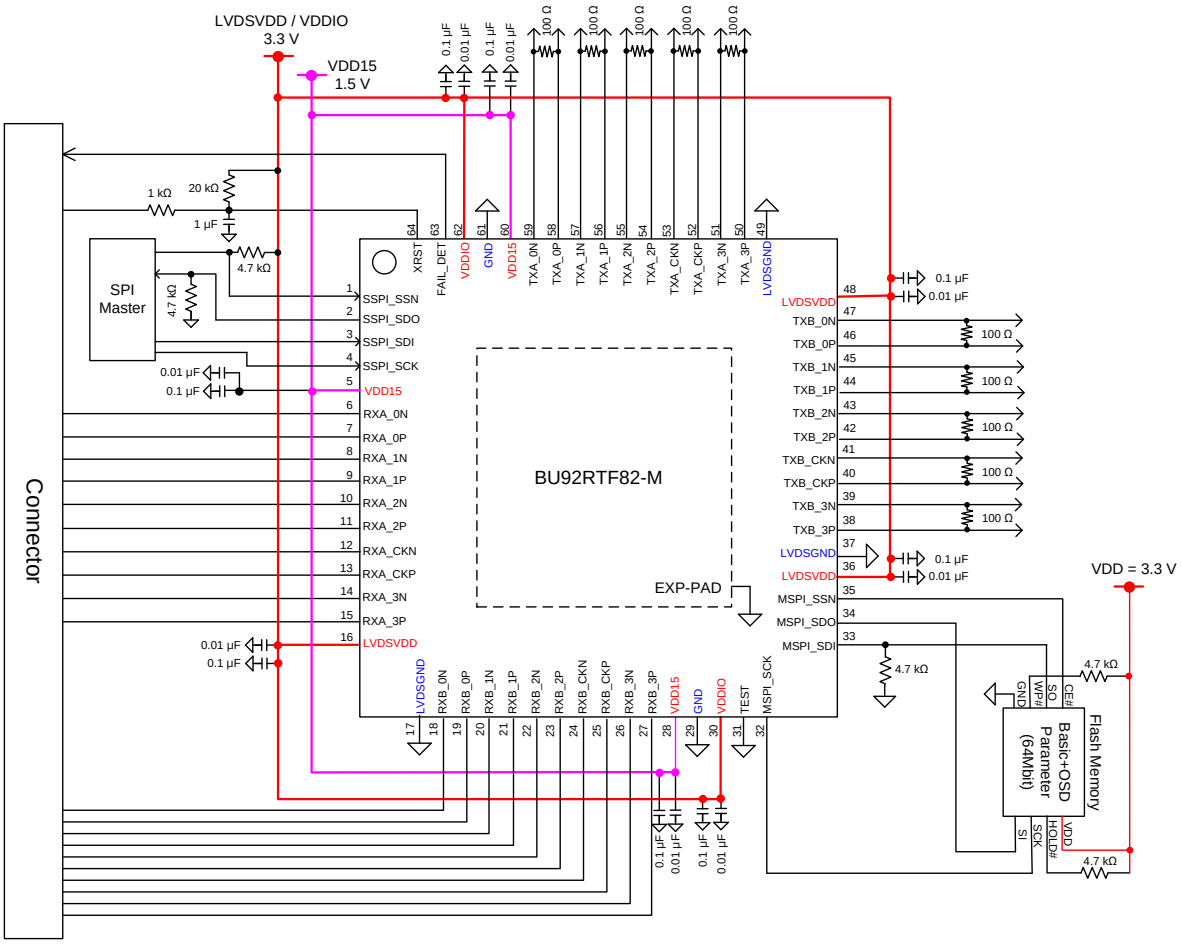


Figure 23. Application Example
(Dual-in / Dual-out Mode)

Application Examples - continued

Single-in / Dual-out Mode

LVDS Receiver: Single Input (8 bits), LVDS Transmitter: Dual Output (8 bits)
VDD15 = 1.5 V, LVDSVDD = VDDIO = 3.3 V

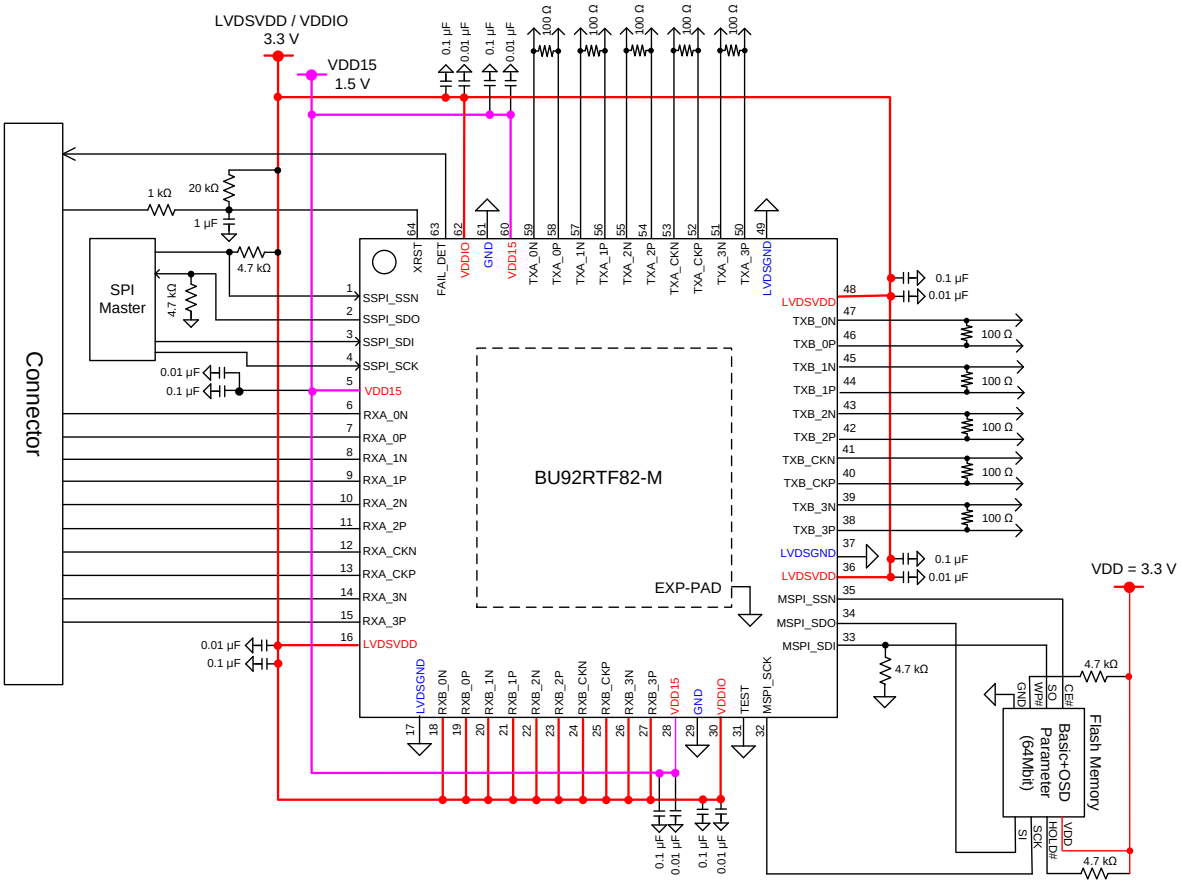


Figure 24. Application Example
(Single-in / Dual-out Mode)

Application Examples - continued

Single-in / Single-out Mode

LVDS Receiver: Single Input (6 bits), LVDS Transmitter: Single Output (6 bits)
LVRX_CH_SWAP = H, LVTX_CH_SWAP = H
VDD15 = 1.5 V, LVDSVDD = VDDIO = 3.3 V

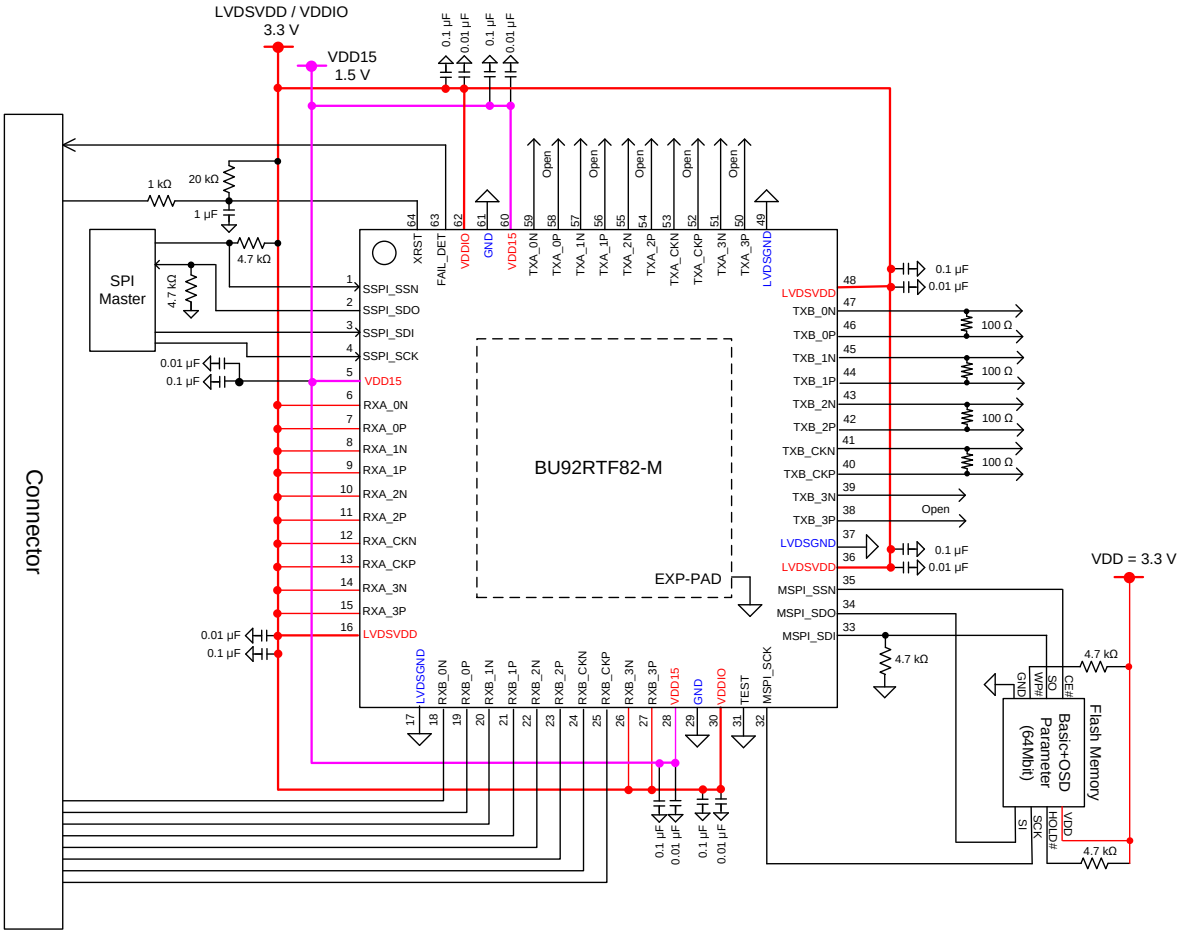


Figure 25. Application Example
(Single-in / Single-out Mode)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

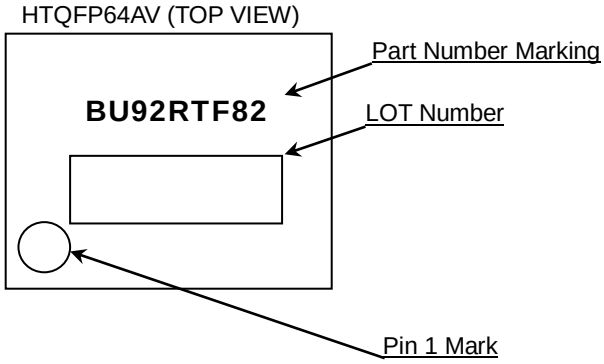
11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

B U 9 2 R T F 8 2	-	ME2

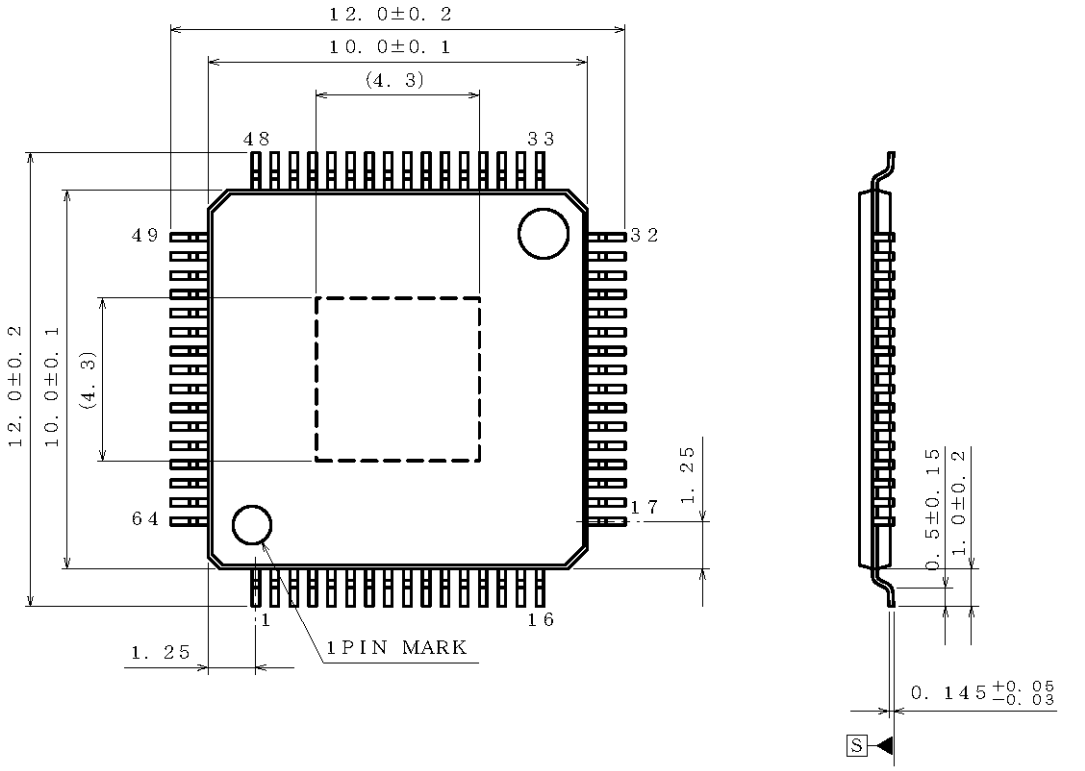
Product Rank
M: For Automotive
Packaging and Forming Specification
E2: Embossed Tape and Reel

Marking Diagram



Physical Dimension and Packing Information

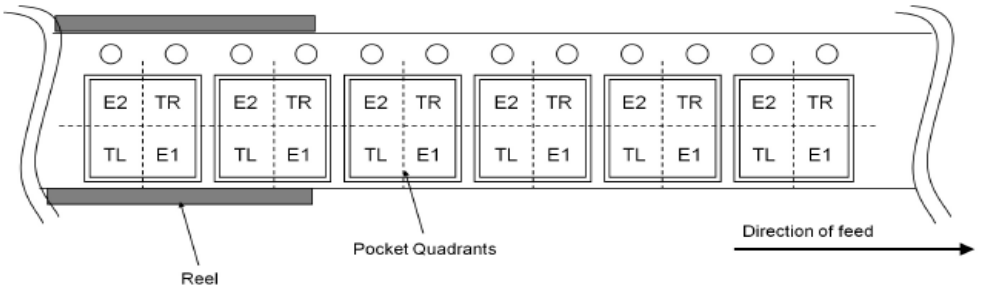
Package Name	HTQFP64AV



(UNIT : mm)
PKG : HTQFP64AV
Drawing No. EX285-5001

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
05.Mar.2019	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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