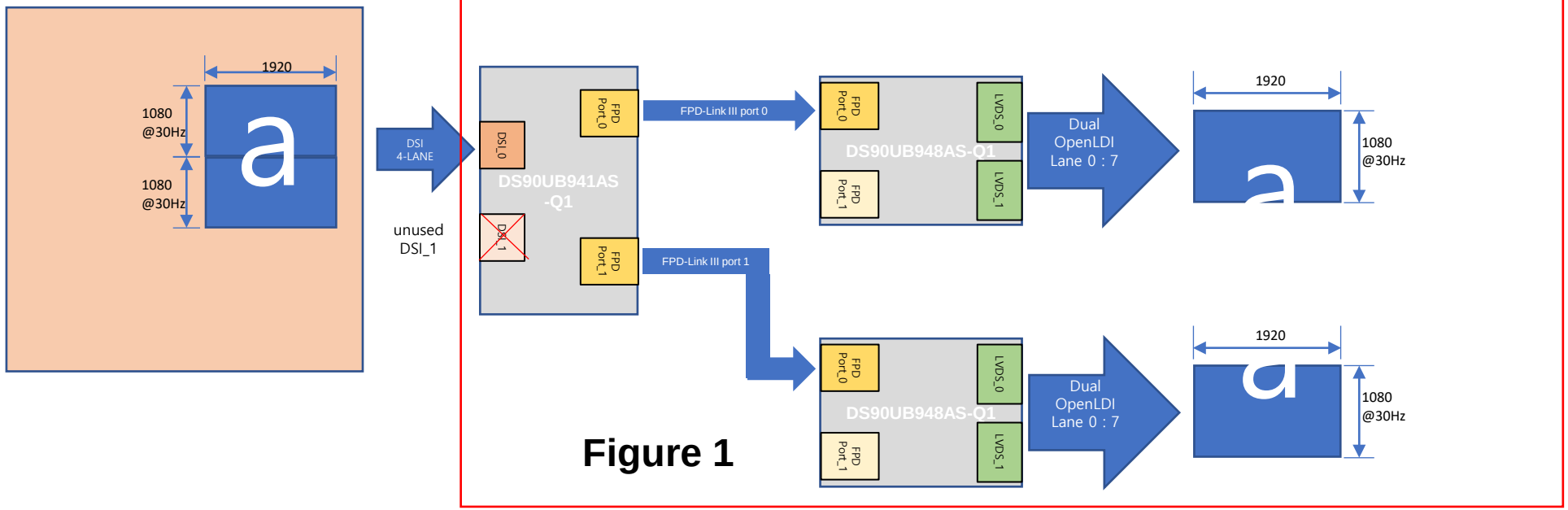

Figure 1

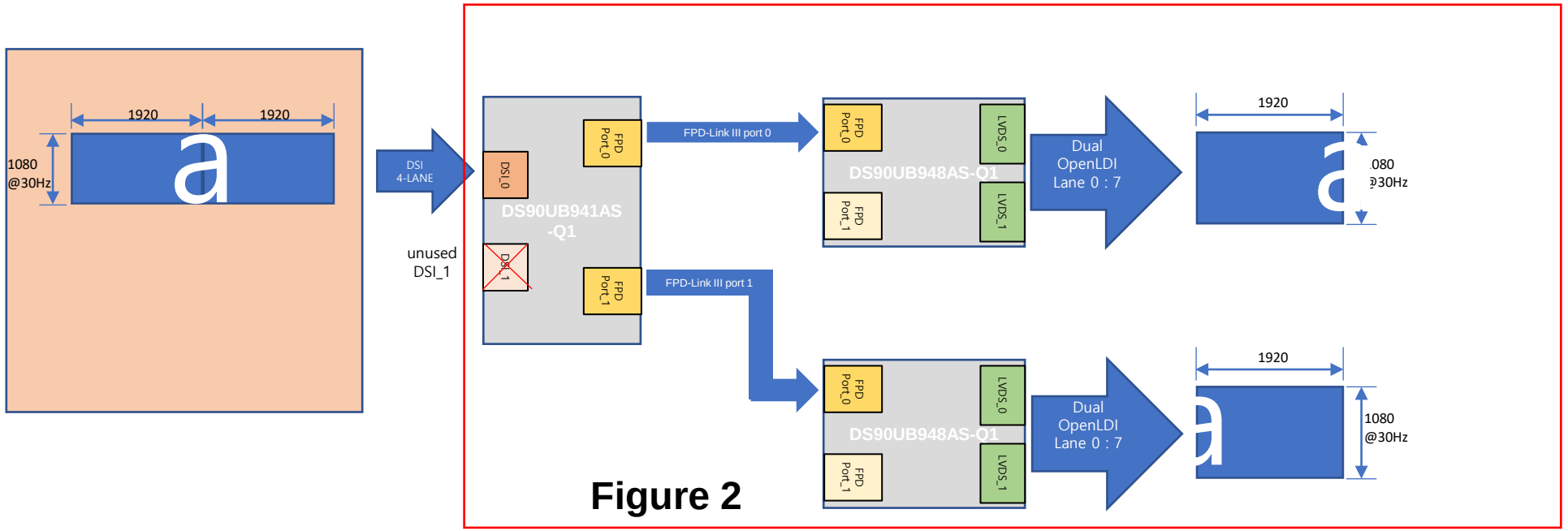

Figure 2

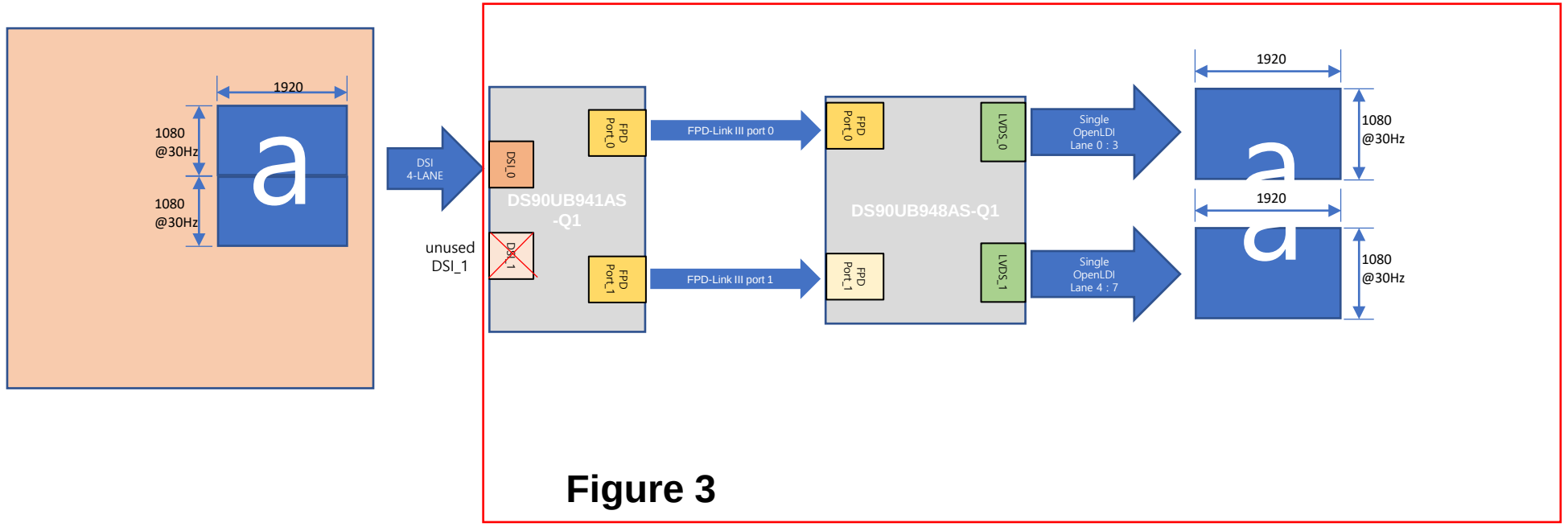

Figure 3

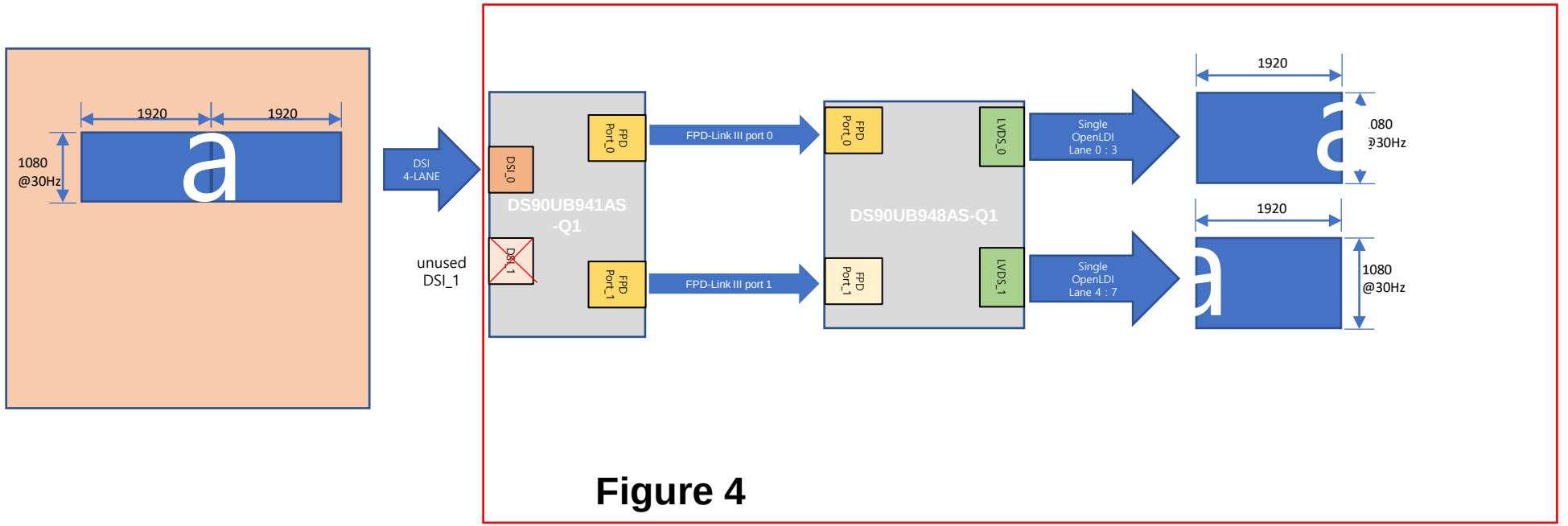

Figure 4

1 Features

- AEC-Q100 qualified for automotive applications with the following results:
  - Device temperature grade 2: −40℃ to +105℃ ambient operating temperature
- Supports pixel clock frequency up to 210 MHz for 3K (2880x1620) at 30Hz, QXGA (2048x1536), 2K (2880x1080), WUXGA (1920x1200), or 1080p60 (1920x1080) resolutions with 24-bit color depth
- MIPI D-PHY / Display Serial Interface (DSI) receiver provides a high-bandwidth interface to video processor or FPGA
  - Dual DSI input ports with up to 4 data lanes each
  - Up to 1.5 Gbps per lane
  - Superframe with symmetric and asymmetric unpacking capability
  - ECC and CRC generation
  - Virtual channel capability
- Single and dual FPD-Link III outputs
  - Single link: up to 105MHz pixel clock
  - Dual link: up to 210MHz pixel clock
- Functional Safety-Capable
  - Documentation available to aid ISO 26262 system design
- Symmetric and asymmetric video splitting
- Integrated HDCP v1.4 cipher engine with on-chip key storage

Figure 5