85 Mhz 6/8-Bits LVDS Receiver

EP102C

User Guide

V0.2

Revised: Oct. 27, 2010

Original Release Date: Aug. 02, 2010

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Aug/06/2010	Ether Lai	Revise Electrical Characteristic and Package Information from EP102
0.2	Oct/27/2010	Ether Lai	Change the minimum supported bandwidth;

Section 1 Introduction

1.1 Overview

EP102C is a 6/8-bit LVDS receiver capable of receiving LVDS inputs at 85 Mhz clock rate. The chip converts the LVDS differential inputs into 18/24-bits RGB data outputs and 3 control outputs (Vsync, Hsync & DE). In 18-bit RGB applications, the 6-bit data can be output left or right justified from the 8-bit data output pins.

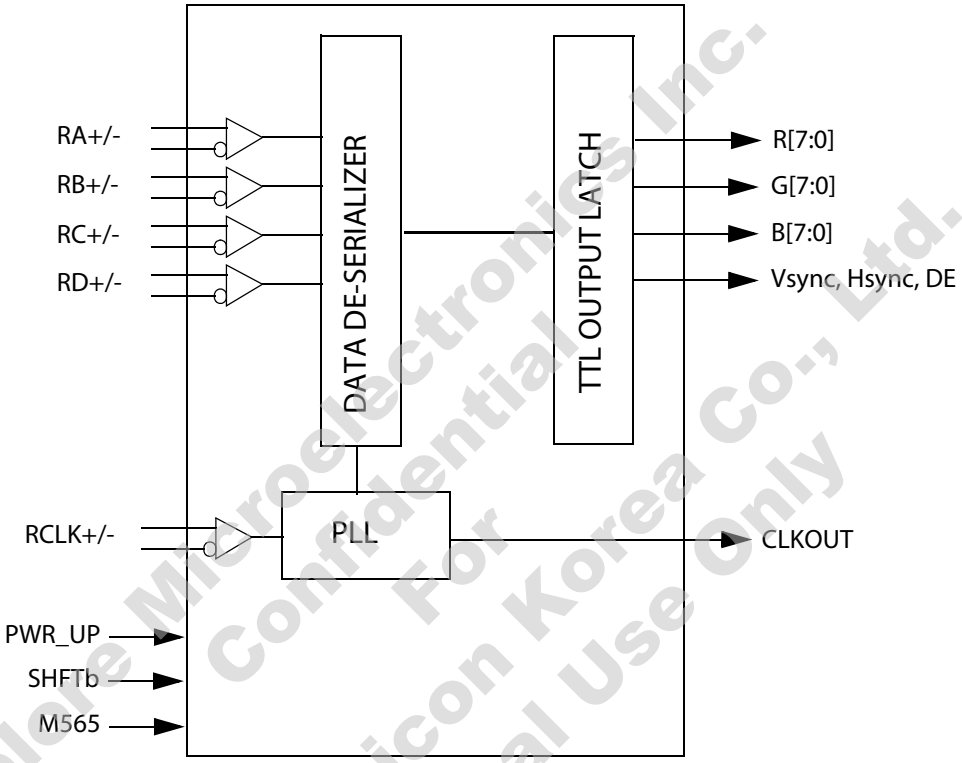
1.2 Features

- Wide operating frequency range: 28 ~85 Mhz pixel rate
- Wide channel skew tolerance: 1/3 bit time
- Selectable left or right justified in 6-bit data output.
- No external components required
- Power Down Mode
- Single Power Supply (3.3V)
- Low profile 56 Lead TSSOP Package (Pb-free)

Section 2 Overview

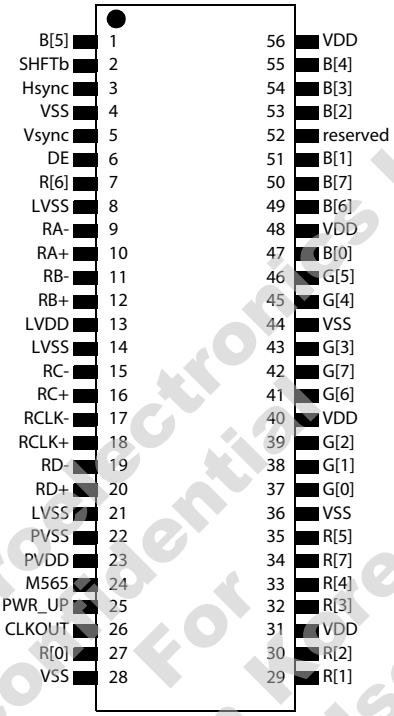
2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram

Figure 2-2 Pin Diagram



2.3 Pin Description

Table 2-1 Digital I/O Pins

NAME	IN/OUT	DESCRIPTION
R[7:0]	OUT	RGB Data Outputs
G[7:0]		
B[7:0]		
Vsync	OUT	Vertical Sync Output
Hsync	OUT	Horizontal Sync Output
DE	OUT	DE Output
CLKOUT	OUT	Data Clock Output.
PWR_UP	IN	H : Normal Operation L : Power Down Mode (Internal Logics return to reset state)
SHFTb	IN	H or Open : 6-bit RGB data is right justified. MSB appears at R/G/B[5]. LSB appears at R/G/B[0]. L : 6-bit RGB data is left justified. MSB appears at R/G/B[7]. LSB appears at R/G/B[2]. R/G/B[1:0] are output as 0. Note: In 8-bit applications, this pin should be tied High or left unconnected.
M565	IN	H : LSB of R/B inputs are replaced with R/B[5] inputs L : LSB of R/B inputs stay unchanged Note: In 8-bit applications, this pin should be tied Low.
reserved	IN	Reserved for testing. Should be tied low or left unconnected in normal operation. It is recommended to tie this pin to LOW state.

Table 2-2 LVDS Input Pins

NAME	IN/OUT	DESCRIPTION
RA-, RA+	IN	LVDS differential data input. The 100Ω termination resistor shall be placed between the differential plus and differential minus input.
RB-, RB+		
RC-, RC+		
RD-, RD+		
RCLK-, RCLK+	IN	LVDS differential clock input. The 100Ω termination resistor shall be placed between RCLK+ and RCLK-.

Table 2-3 Power and Ground Pins

NAME	IN/OUT	DESCRIPTION
VDD	PWR	Digital VDD, 3.3 V
VSS	GND	Digital Ground
LVDD	PWR	Analog VDD, 3.3 V
LVSS	GND	Analog Ground
PVDD	PWR	PLL VDD, 3.3 V
PVSS	GND	PLL Ground

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc[1]	Supply Voltage	-0.3	3.3	4.0	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O[2]	Output Voltage	-0.3		V_{cc} + 0.3	V
V_{ID}	LVDS Driver Input Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature	-40		125	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		56.82		°C/W

NOTES:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0		3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	-40	25	85	°C

CMOS/TTL DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		0.8 Vcc		Vcc	V
V_{IL}	Low-level Input Voltage		GND		0.2 Vcc	V
V_{OH}	High-level Output Voltage	I_{OH} = -2 mA	Vcc - 0.6			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2 mA			0.4	V
I_{INC}	Input Current	0 <= V_{IN} <= Vcc			+/- 10	uA

LVDS Receiver DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{OC} = 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{OC} = 1.2V	-100			mV
I_{INL}	Input Current	V_{IN} = 2.0V/ 0V, V_{DD} = 2.75V			+/- 20	uA

Supply Current (under normal operating conditions unless otherwise specified)

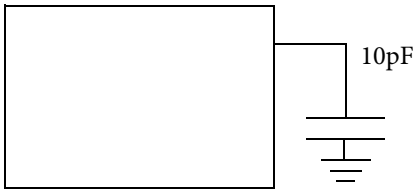
Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{RCCG}	Receiver Supply Current	C_L = 10 pF, 256 Grayscale Pattern Vcc = 3.3V	F = 85 MHz		55		mA
		C_L = 10 pF, Worst Case Pattern[1] Vcc = 3.3V	F = 85 MHz		87		mA
I_{RCCZ}	Receiver Power Down Current	PWR_UP = 0			650		uA

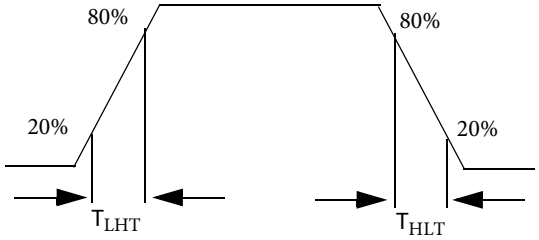
NOTES:

1. Black and White checkboard pattern, each checker is 1 pixels wide.

AC Specifications (under normal operating conditions unless otherwise specified)

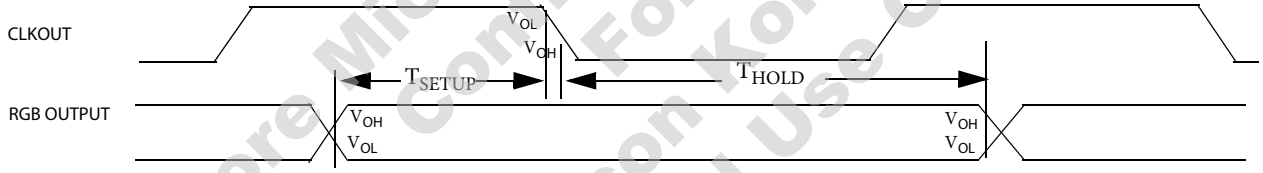
Digital Output Transition





Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{LHT}	TTL Low to High Transition Time (V_{CC} = 3.3V)	CLKOUT Pin		940		ps
		Other Output Pins		1.22		ns
T_{HLT}	TTL High to Low Transition Time (V_{CC} = 3.3V)	CLKOUT Pin		1.12		ps
		Other Output Pins		1.12		ns

Data Output Timing

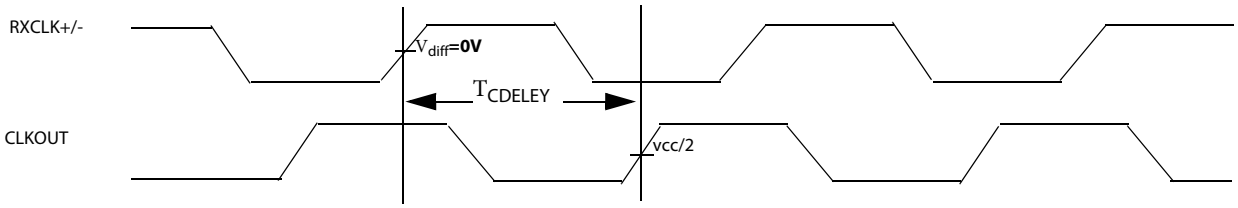


Symbol	Parameter	Conditions		Min	Typ	Max	Units
T_{SETUP}	Setup time[1]	V_{CC} = 3.3V	CLK=85MHz	5.6	6.6		ns
T_{HOLD}	Hold time[1]	V_{CC} = 3.3V	CLK=85MHz	4.32	4.6		ns

NOTES:

1. The data is triggered out at clock rising edge; In next stage, the data is expected to be latched at clock falling edge.

T_{CDELAY}



Symbol	Parameter	Conditions		Min	Typ	Max	Units
T_{CDELAY}	RXCLK+/- TO CLKOUT DELAY[1]	V_{CC} = 3.3V	CLK=75MHz	69.3		73.3	ns

NOTES:

1. In normal operation, the RXCLK+/- shall be stopped for 10ms while the frequency of the input clock is changed.

LVDS Receiver AC Specifications (Vcc = 3.3V and normal operating conditions)

Symbol	Parameter	Min	Typ	Max	Units
T_{must}	Mode Unstable Silent Time	10			ms
$t_{RI}CLK$	Input CLK period	11.8		35.7	ns
$t_{RI}0$	Input Data Position 0 ($t_{RI}CLK$ = 11.8ns)	-0.35	0	+0.35	ns
$t_{RI}1$	Input Data Position 1 ($t_{RI}CLK$ = 11.8ns)	$\frac{t_{RI}CLK}{7}$ - 0.35	$\frac{t_{RI}CLK}{7}$	$\frac{t_{RI}CLK}{7}$ + 0.35	ns
$t_{RI}2$	Input Data Position 2 ($t_{RI}CLK$ = 11.8ns)	$2\frac{t_{RI}CLK}{7}$ - 0.35	$2\frac{t_{RI}CLK}{7}$	$2\frac{t_{RI}CLK}{7}$ + 0.35	ns
$t_{RI}3$	Input Data Position 3 ($t_{RI}CLK$ = 11.8ns)	$3\frac{t_{RI}CLK}{7}$ - 0.35	$3\frac{t_{RI}CLK}{7}$	$3\frac{t_{RI}CLK}{7}$ + 0.35	ns
$t_{RI}4$	Input Data Position 4 ($t_{RI}CLK$ = 11.8ns)	$4\frac{t_{RI}CLK}{7}$ - 0.35	$4\frac{t_{RI}CLK}{7}$	$4\frac{t_{RI}CLK}{7}$ + 0.35	ns
$t_{RI}5$	Input Data Position 5 ($t_{RI}CLK$ = 11.8ns)	$5\frac{t_{RI}CLK}{7}$ - 0.35	$5\frac{t_{RI}CLK}{7}$	$5\frac{t_{RI}CLK}{7}$ + 0.35	ns
$t_{RI}6$	Input Data Position 6 ($t_{RI}CLK$ = 11.8ns)	$6\frac{t_{RI}CLK}{7}$ - 0.35	$6\frac{t_{RI}CLK}{7}$	$6\frac{t_{RI}CLK}{7}$ + 0.35	ns

Figure 2-3 Mode Unstable Silent Time

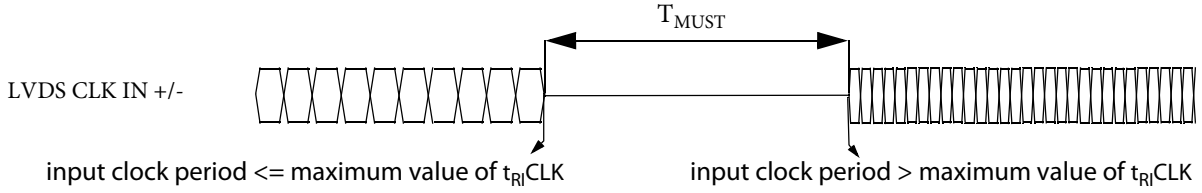
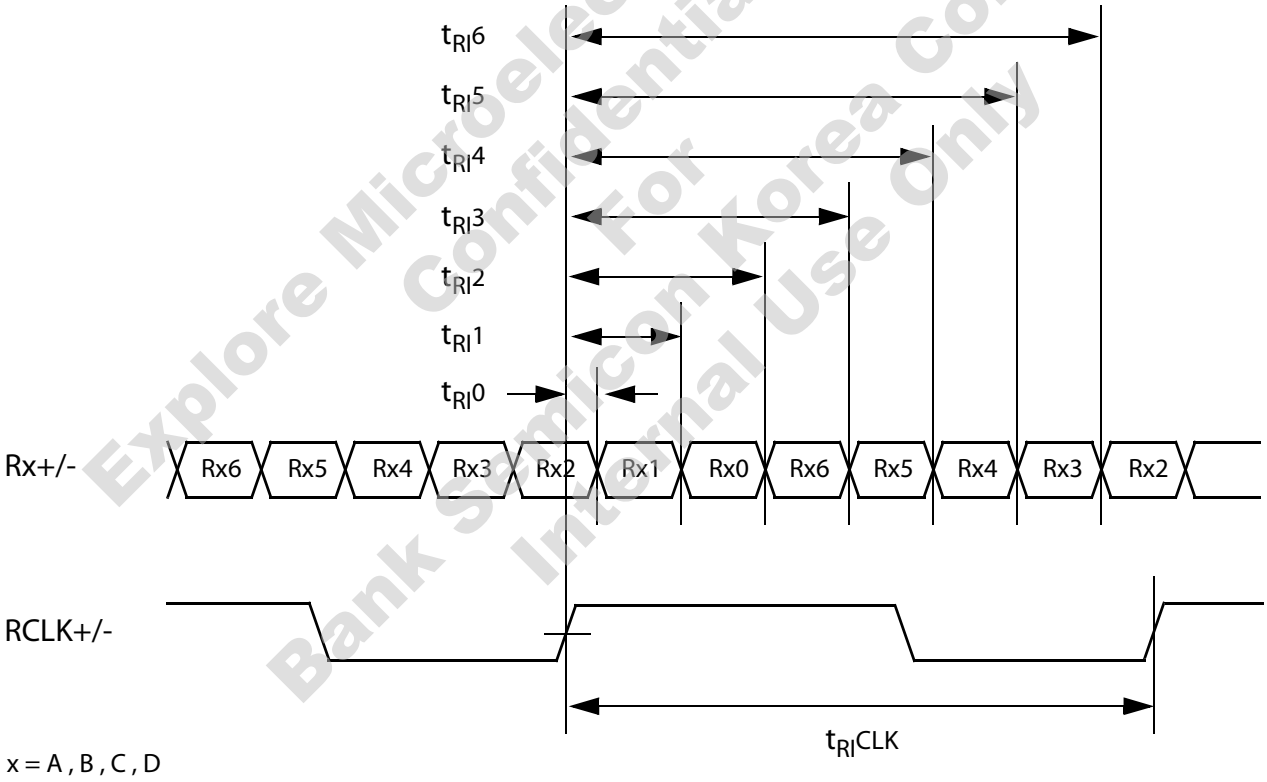


Figure 2-4 LVDS Receiver AC Timing

AC timing diagrams

LVDS input



2.5 LVDS Outputs / TTL Data Inputs Mapping

The LVDS Clock waveshape is shown in the following figure. Note that the rising edge of the LVDS clock occurs two LVDS sub symbols before the current cycle of data. The clock is composed of a 4 LVDS sub symbol HIGH time and a 3 LVDS sub symbol LOW time.

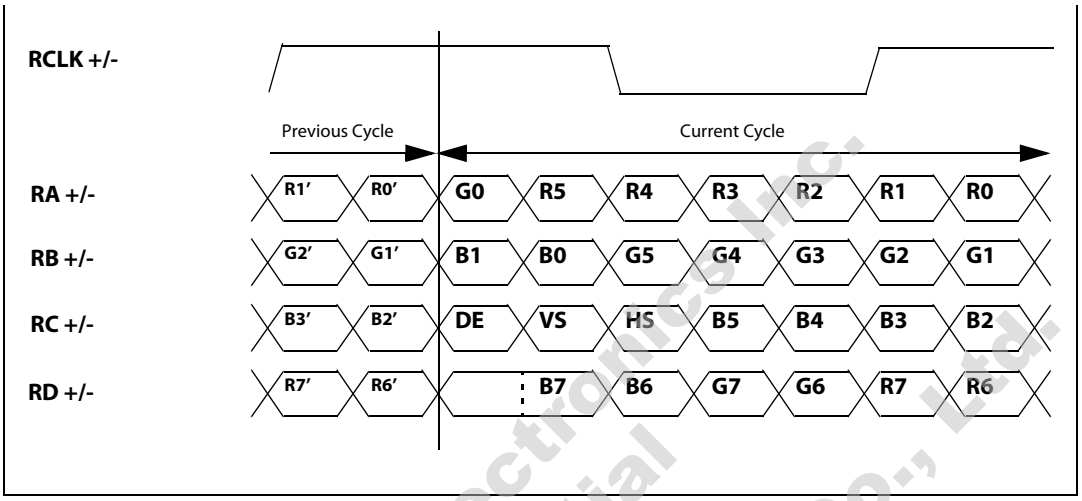
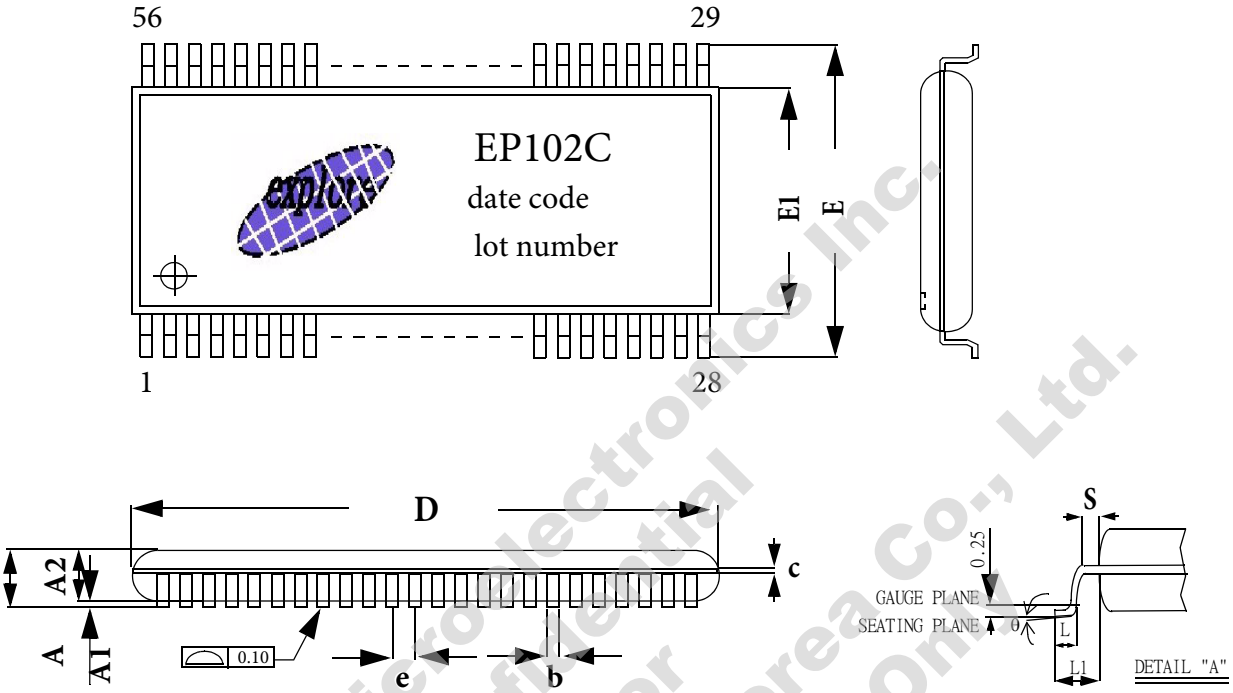


Figure 2-5 LVDS Inputs / TTL Outputs Data Mapping

Appendix A Package

Figure A-1 EP102C Footprint Diagram

TSSOP 56L



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.05	0.1	0.15
A2	0.08	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D	13.90	14.00	14.10
E1	6.00	6.10	6.20
E	8.10 BSC		
e	0.50 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	-	-
θ	0"	-	8"

NOTES:
1. JEDEC OUTLINE : MO-153 EE REV.F
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTERLEAD FLASH, PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN SPROTRUSION AND ADJACENT LEAD IS 0.07mm.