High Speed 8-bits LVDS Transmitter
EP103T

User Guide
V0.5

Revised Date: May 19, 2011

Original Release Date: Aug 25, 2010

Explore Microelectronics, Taiwan

Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Aug/25/2010	Ether Lai	Initial Version
0.2	Nov/01/2010	Kyle Kuo	1. Modified Package Dimension 2. Modified V_{OD} 、V_{OC} From LVDS Transmitter DC Specification 3. Added supply current
0.3	Nov/23/2010	Ether Lai	Fix typos & Revise Input Data Assignment Table;
0.4	Jan/19/2011	Kyle Kuo	Modified chip version and chip package
0.5	May/19/2011	Ether Lai	Revise the Thermal Resistance & Redraw the Pin Assignment

Section 1 Introduction

1.1 Overview

The EP103T LVDS transmitter supports transmission between the host and the flat panel display up to SXGA+ resolutions. The transmitter converts 25 bits (8-bits/color, 2 dummy bits) of Low Voltage TTL data and 3 control bits into 4 LVDS (Low Voltage Differential Signal) data streams. At a maximum input clock rate of 135MHz, each LVDS differential data pair speed is 945Mbps, providing a total throughput of 3.78Gbps. The transmitter can be configured to input clock rising edge or falling edge strobe through an external pin.

1.2 Features

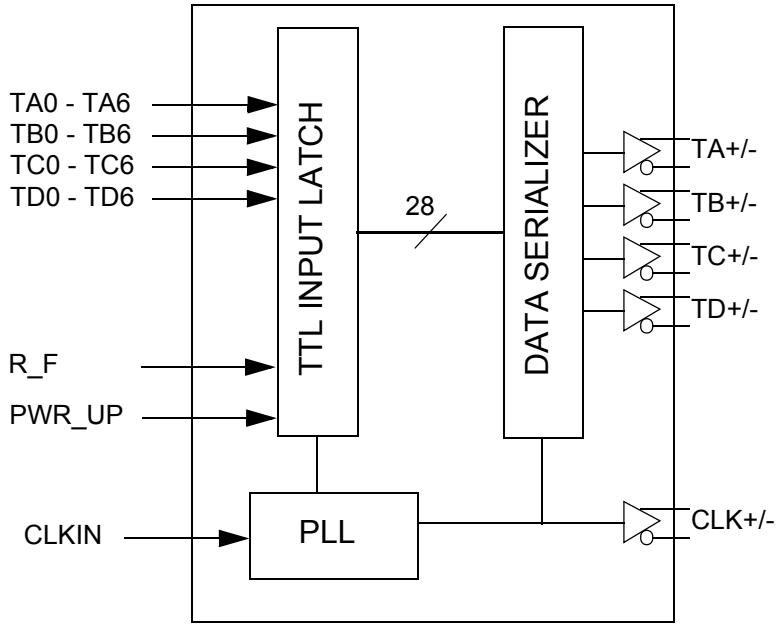
The EP103T includes the following distinctive features:

- Support 10MHz to 135MHz clock rates for HVGA to SXGA+ resolution
- Up to 3.78Gbps bandwidth
- PLL requires no external components
- Cycle-to-cycle jitter rejection
- 3.3V to 1.8V Low Voltage TTL tolerant Input
- Programmable data and control strobe select
- Power down mode supported
- TSSOP package (8.1mm x 14mm)

Section 2 Overview

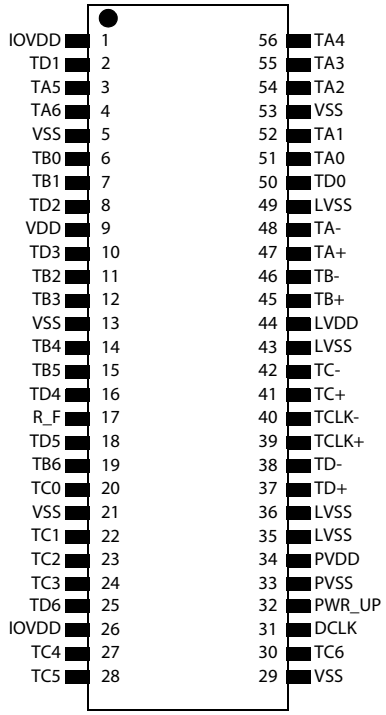
2.1 Block Diagram

Figure 2-1 Block Diagram of LVDS Transmitter



2.2 Pin Diagram

Figure 2-2 TSSOP Pin Diagram



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Input Control/Data/CLK Pins

NAME	IN/OUT	DESCRIPTION
TA0~TA6 TB0~TB6 TC0~TC6 TD0~TD6	IN	Pixel Data Inputs
DCLK	IN	Data Clock Input.
PWR_UP	IN	Power Up.
R_F	IN	Input data latching Edge. 1: DCLK Rising Edge; 0: DCLK Falling Edge.

Table 2-2 LVDS Output Pins

NAME	IN/OUT	DESCRIPTION
TA-	OUT	Negative LVDS differential data output.
TA+	OUT	Positive LVDS differential data output.
TB-	OUT	Negative LVDS differential data output.
TB+	OUT	Positive LVDS differential data output.
TC-	OUT	Negative LVDS differential data output.
TC+	OUT	Positive LVDS differential data output.
TCLK-	OUT	Negative LVDS differential clock output.
TCLK+	OUT	Positive LVDS differential clock output.
TD-	OUT	Negative LVDS differential data output.
TD+	OUT	Positive LVDS differential data output.

Table 2-3 Power and Ground Pins

NAME	IN/OUT	DESCRIPTION
VDD	PWR	Digital VDD, 3.3V
VSS	GND	Digital Ground.
LVDD	PWR	Analog VDD, 3.3V
LVSS	GND	Analog Ground.
PVDD	PWR	PLL VDD, 3.3V
PVSS	GND	PLL Ground.
IOVDD	PWR	IO Power (1.8V ~ 3.3V)

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc} + 0.3	V
V_{OD}	LVDS Driver Output Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature	-25		125	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		70		°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		45		°C/W

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vio	I/O Voltage	1.62	1.8/2.5/3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	-10	25	70	°C

TTL Input DC Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage	IOVCC = 3.3V	IOVCC/2 + 0.5			V
		IOVCC = 2.5V	IOVCC/2 + 0.4			
		IOVCC = 1.8V	IOVCC/2 + 0.3			
V_{IL}	Low-level Input Voltage	IOVCC = 3.3V			IOVCC/2 - 0.5	V
		IOVCC = 2.5V			IOVCC/2 - 0.4	
		IOVCC = 1.8V			IOVCC/2 - 0.3	

LVDS Transmitter DC Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	R_L = 100 Ω, Normal Swing	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L = 100 Ω			35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between complimentary output states				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100 Ω		-7.5	-15	mA
I_{OZ}	Output Tri-State Current	PWR_UP = 0V		+/- 1	+/- 10	uA

Supply Current (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{TCCG}	F=75 Mhz	R_L = 100 Ω, C_L = 5 pF VDD=LVDD=PVDD=3.3V IOVDD = 1.8V	Worst Case Pattern TEST-TTL/ECL		50	65	mA
			16 Grayscale Pattern		48	60	mA
			W50%_B50%		48	60	mA
	F = 100 Mhz	R_L = 100 Ω, C_L = 5 pF	Worst Case Pattern TEST-TTL/ECL		53	65	mA
	F = 135 Mhz	R_L = 100 Ω, C_L = 5 pF	Worst Case Pattern TEST-TTL/ECL		60	75	mA
I_{TCCZ}		Transmitter Supply Current Power Down PWR_UP = 0; Input Pins = LOW			5	250	uA

Figure 2-3 Worst Case Pattern

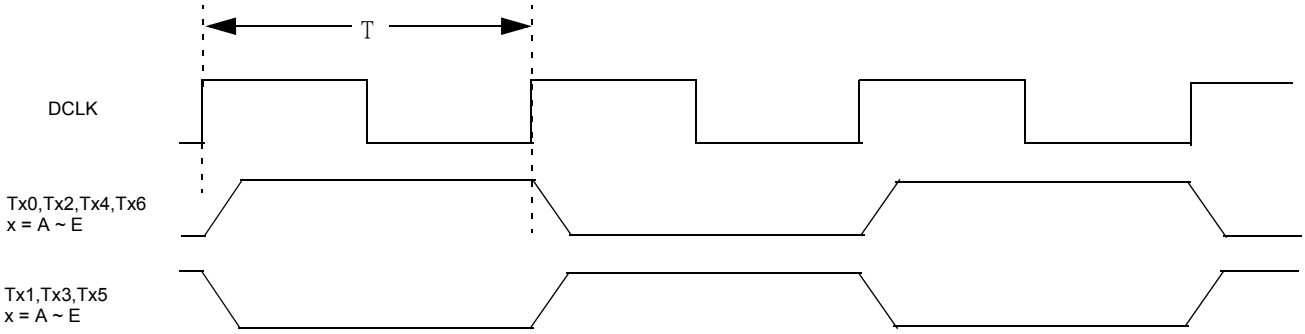
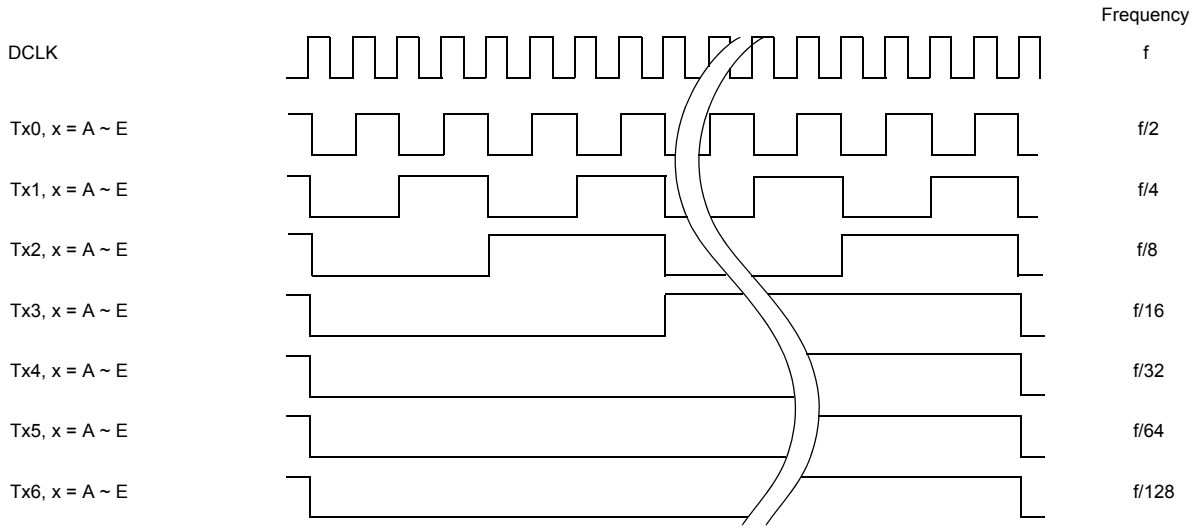


Figure 2-4 Grayscale Pattern



Recommended Transmitter Input Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIT}	DCLK IN Transition Time				3.0	ns
T_{CIP}	DCLK IN Period		7.4		125	ns
T_{TCH}	DCLK IN High Time		0.35T	0.5T	0.65T	ns
T_{TCL}	DCLK IN Low Time		0.35T	0.5T	0.65T	ns

Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{LHT}	LVDS Transition Time			0.7	1.5	ns
T_{TS}	TTL Data Setup to DCLK IN		3.0			ns
T_{TH}	TTL Data Hold from DCLK IN		0			ns
T_{PLLS}	PLL Set Time				10	ms
T_{PDO}	Power Down Delay				100	ns

2.5 Timing Diagrams

Figure 2-5 LVDS Output Timing Definition

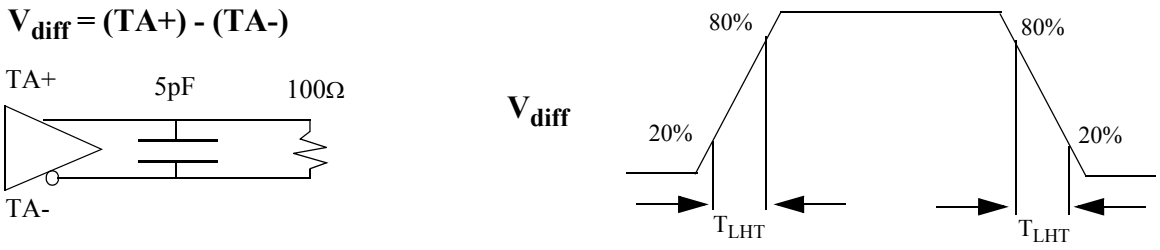


Figure 2-6 TTL Input Timing Definition

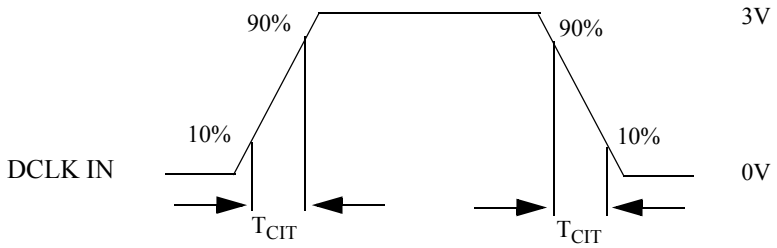


Figure 2-7 Setup/Hold and High/Low Timing Definition (Falling Edge Strobe)

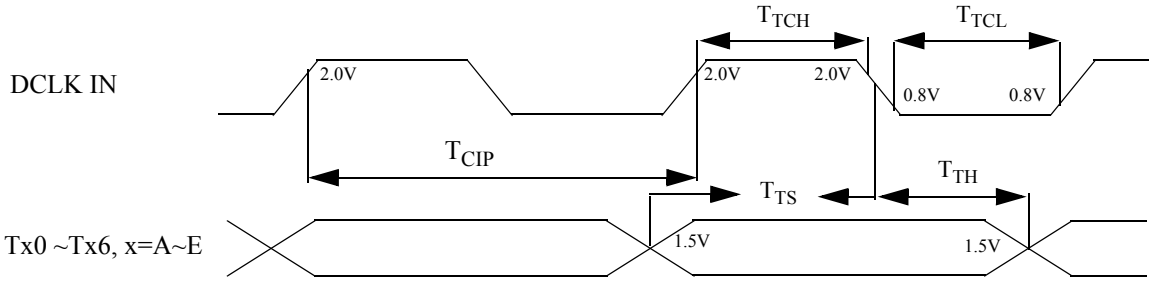


Figure 2-8 Phase Lock Loop Set Time Definition

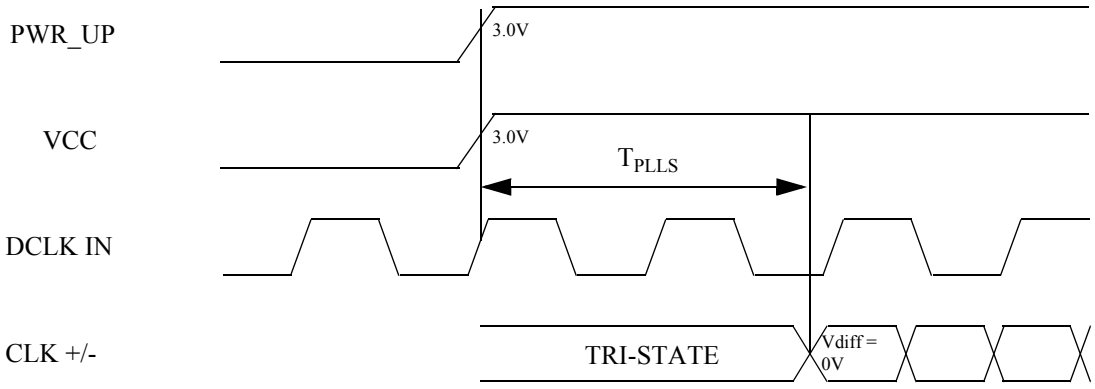
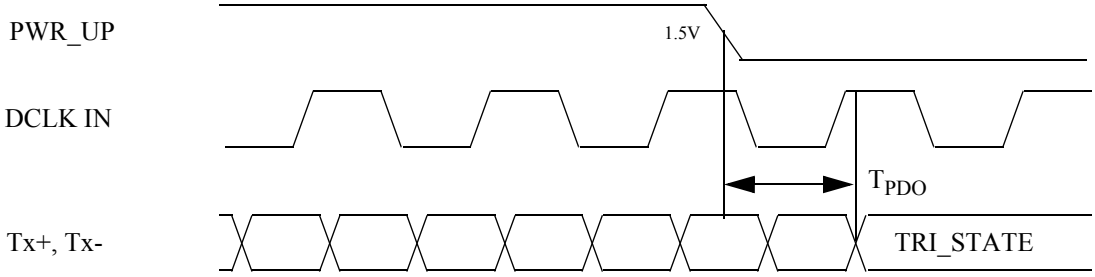


Figure 2-9 Power Down Delay Timing Definition

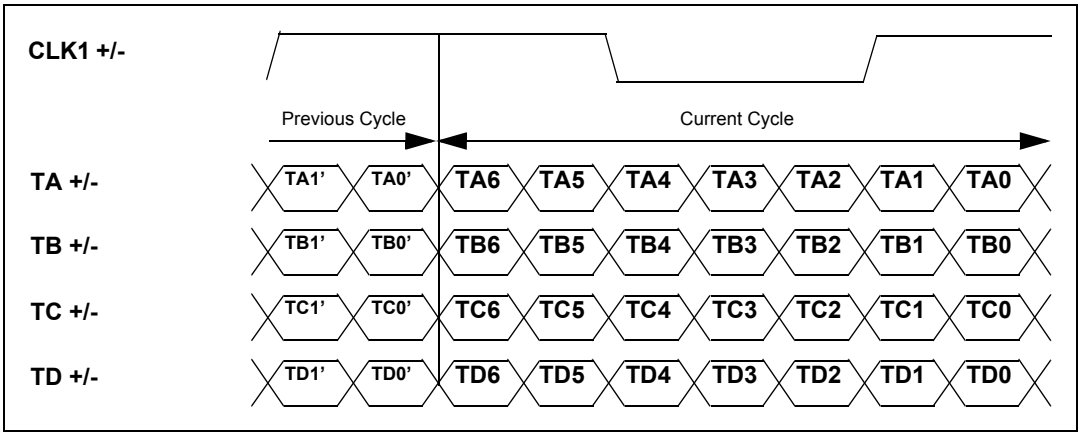


2.6 LVDS Outputs / TTL Data Inputs Mapping

The LVDS Clock waveshape is shown in the following figure. Note that the rising edge of the LVDS clock occurs two LVDS sub symbols before the current cycle of data. The clock is composed of a 4 LVDS sub symbol HIGH time and a 3 LVDS sub symbol LOW time.

The respective pin names are shown in the figure and these names are not the color mapping information but pin names only.

Figure 2-10 LVDS Outputs / TTL Inputs Data Mapping



Following table shows the data mapping for the 8-bits/6-bits input application.

Table 2-4 Input Data Assignment

Data Width	8-bits (R[7:0], G[7:0], B[7:0])		6-bits (R[5:0], G[5:0], B[5:0])
Protocol	JEIDA	VESA	
TA0	R2	R0	R0
TA1	R3	R1	R1
TA2	R4	R2	R2
TA3	R5	R3	R3
TA4	R6	R4	R4
TA5	R7	R5	R5
TA6	G2	G0	G0
TB0	G3	G1	G1
TB1	G4	G2	G2
TB2	G5	G3	G3
TB3	G6	G4	G4
TB4	G7	G5	G5
TB5	B2	B0	B0
TB6	B3	B1	B1
TC0	B4	B2	B2
TC1	B5	B3	B3
TC2	B6	B4	B4
TC3	B7	B5	B5

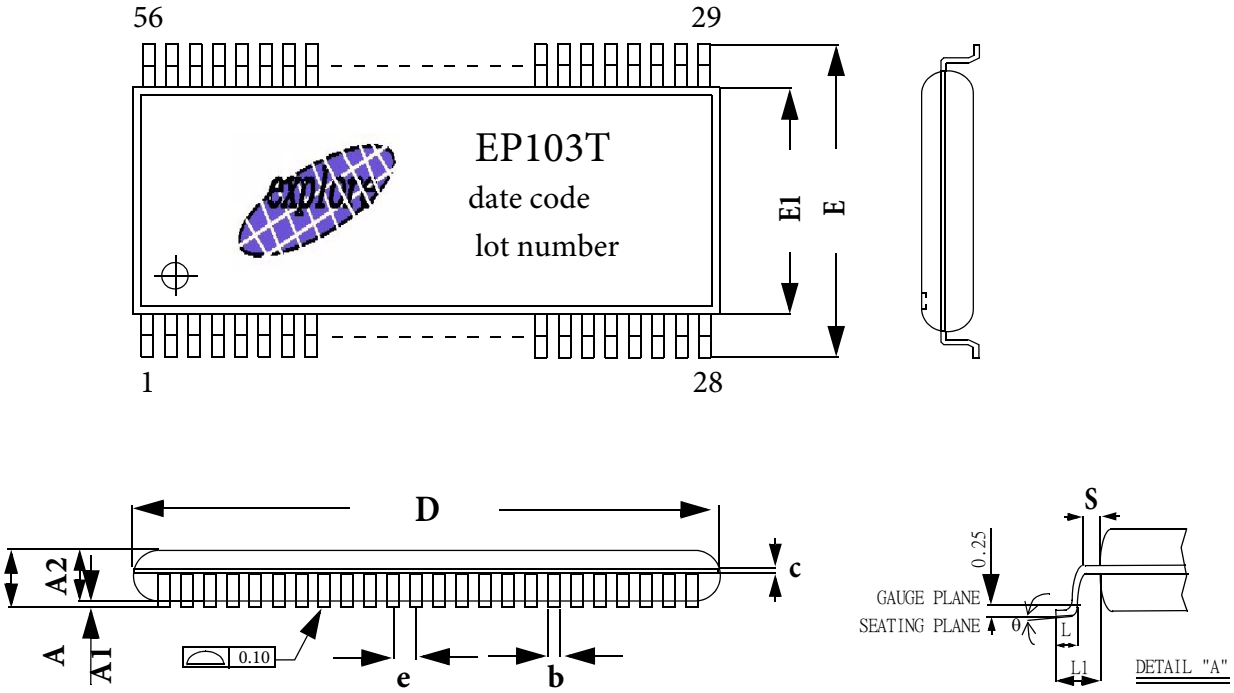
Table 2-4 Input Data Assignment

Data Width	8-bits (R[7:0], G[7:0], B[7:0])		6-bits (R[5:0], G[5:0], B[5:0])
Protocol	**JEIDA**	**VESA**	
TC4	HSYNC	HSYNC	HSYNC
TC5	VSYNC	VSYNC	VSYNC
TC6	DE	DE	DE
TD0	R0	R6	GND
TD1	R1	R7	GND
TD2	G0	G6	GND
TD3	G1	G7	GND
TD4	B0	B6	GND
TD5	B1	B7	GND
TD6	GND	GND	GND

Appendix A Package

Figure A-1 EP103T Footprint Diagram

TSSOP 56L



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.05	0.1	0.15
A2	0.08	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D	13.90	14.00	14.10
E1	6.00	6.10	6.20
E	8.10 BSC		
e	0.50 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	-	-
θ	0"	-	8"

NOTES:
1. JEDEC OUTLINE : MO-153 EE REV.F
2. DIMENSIONS “D” DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSIONS “E1” DOES NOT INCLUDE INTERLEAD FLASH, PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION “b” DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN SPROTRUSION AND ADJACENT LEAD IS 0.07mm.