Block Diagram

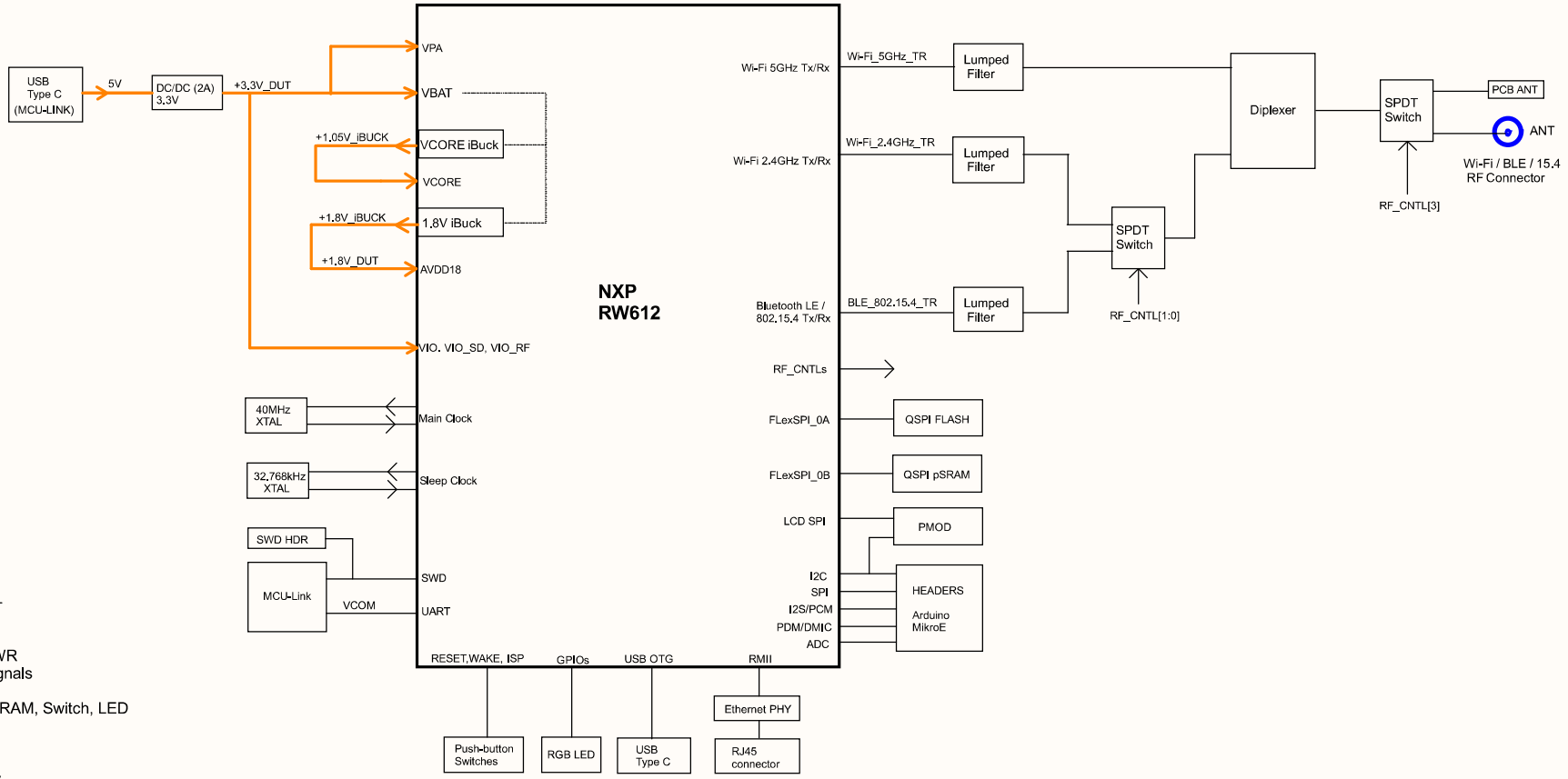
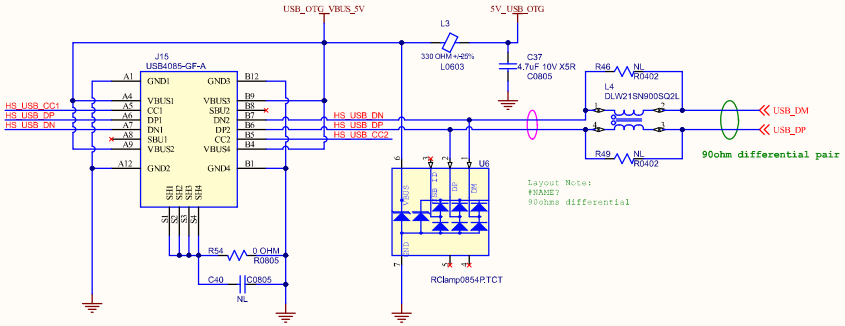
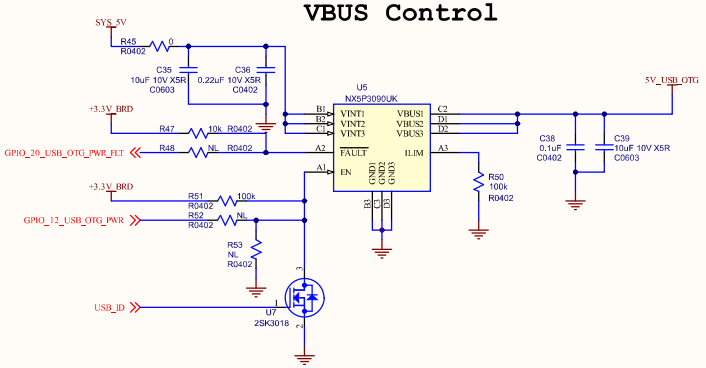


Table of Contents

USB2.0 Type C

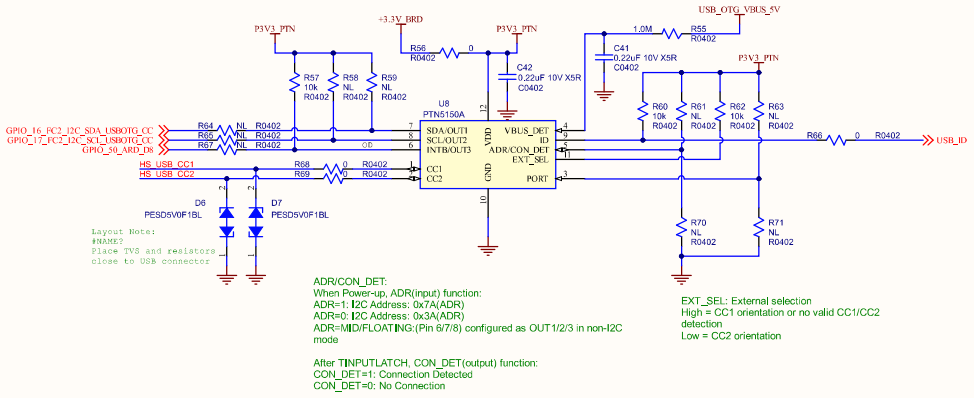


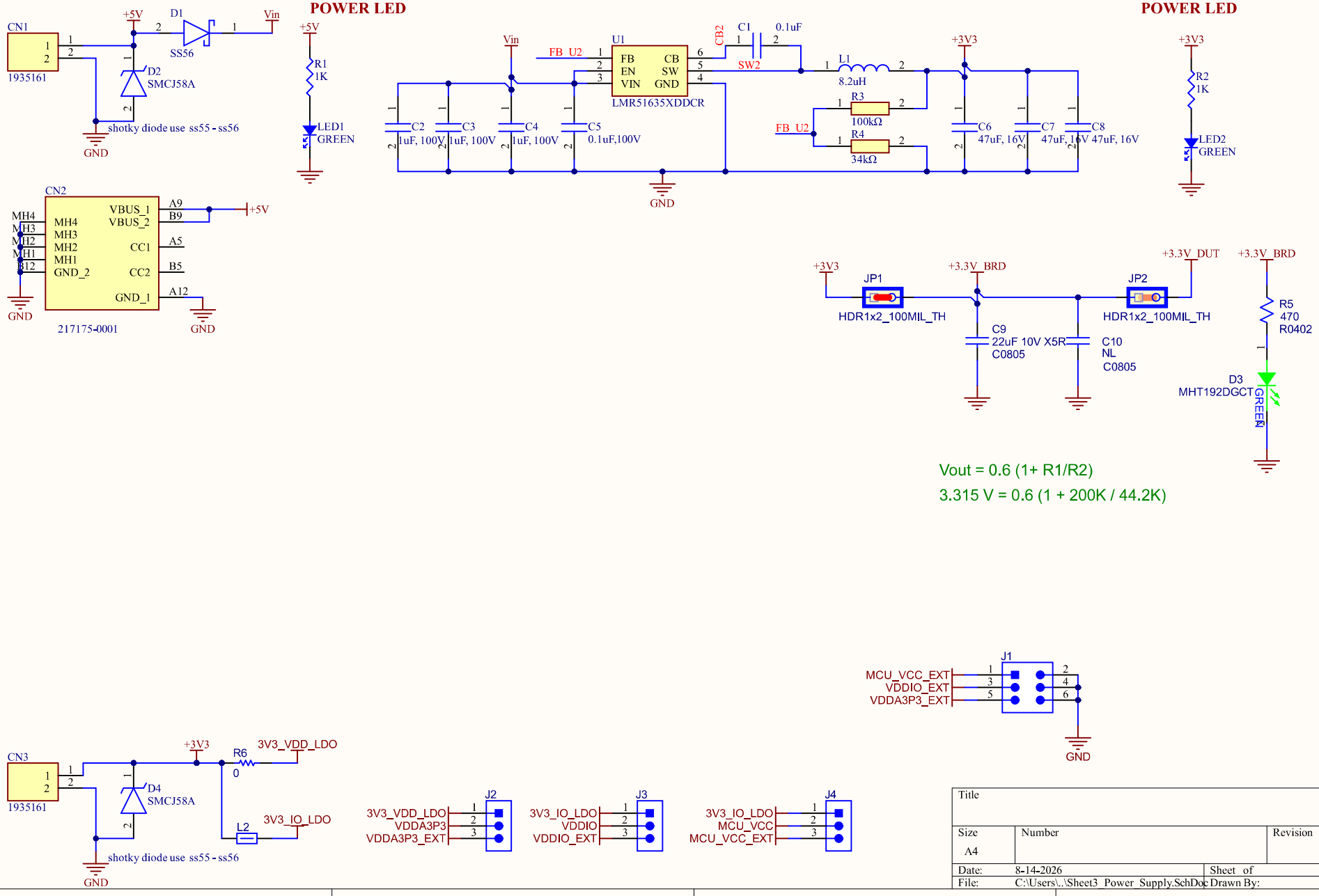
VBUS Control



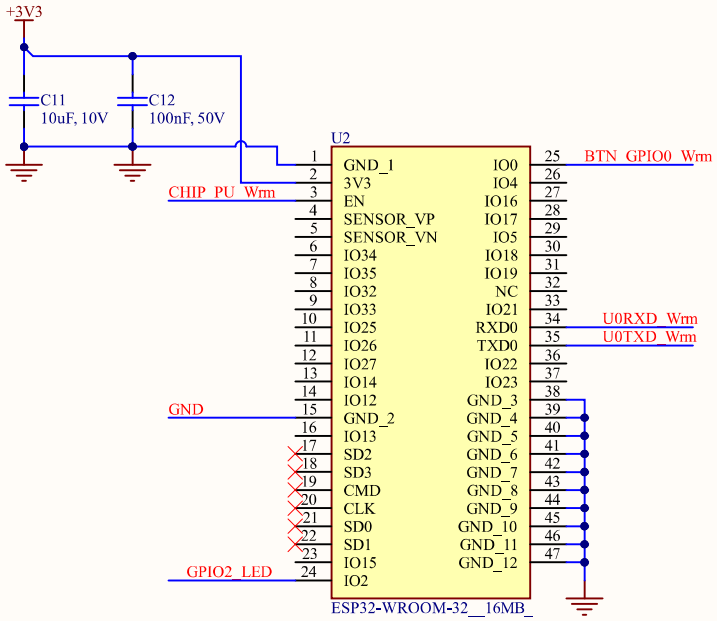
USB_OTG HIGH SPEED

CC Logic Control

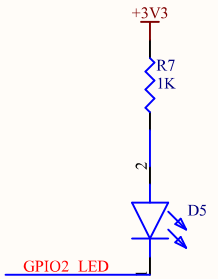



POWER LED
POWER LED
CN1
1935161
+5V
D1
SS56
Vin
D2
SMCJ58A
shotky diode use ss55 - ss56
GND
R1
1K
LED1
GREEN
Vin
FB_U2
U1
FB
EN
VIN
CB
SW
GND
LMR51635XDDCR
CB2
C1
0.1uF
SW2
L1
8.2uH
+3V3
R3
100kΩ
R4
34kΩ
C2
1uF, 100V
C3
1uF, 100V
C4
1uF, 100V
C5
0.1uF,100V
C6
47uF, 16V
C7
47uF, 16V
C8
47uF, 16V
R2
1K
LED2
GREEN
CN2
MH4
MH3
MH2
MH1
B12
VBUS_1
VBUS_2
CC1
CC2
GND_2
GND_1
A9
B9
A5
B5
A12
217175-0001
+3V3
JP1
HDR1x2_100MIL_TH
+3.3V_BRD
C9
22uF 10V X5R
C0805
JP2
+3.3V_DUT
C10
NL
C0805
R5
470
R0402
D3
MHT192DGCT
GREEN
Vout = 0.6 (1+ R1/R2)
3.315 V = 0.6 (1 + 200K / 44.2K)
J1
MCU_VCC_EXT
VDDIO_EXT
VDDA3P3_EXT
CN3
1935161
D4
SMCJ58A
R6
0
3V3_VDD_LDO
L2
3V3_IO_LDO
J2
J3
J4
MCU_VCC
Title
Size
A4
Number
Revision
Date:
8-14-2026
Sheet of
File:
C:\Users\..\Sheet3_Power_Supply.SchDoc
Drawn By:

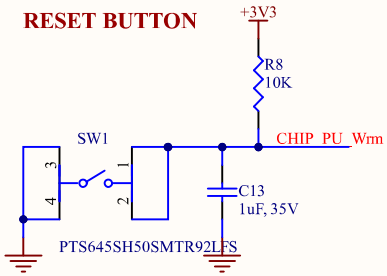
ESP32 Wroom MODULE



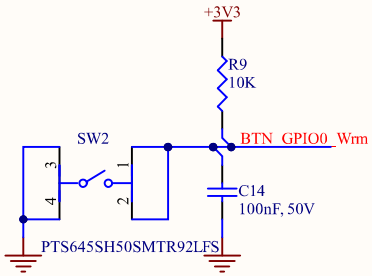
USER LED

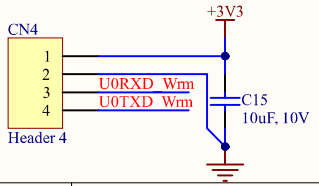


RESET BUTTON



BOOT / USER BUTTON





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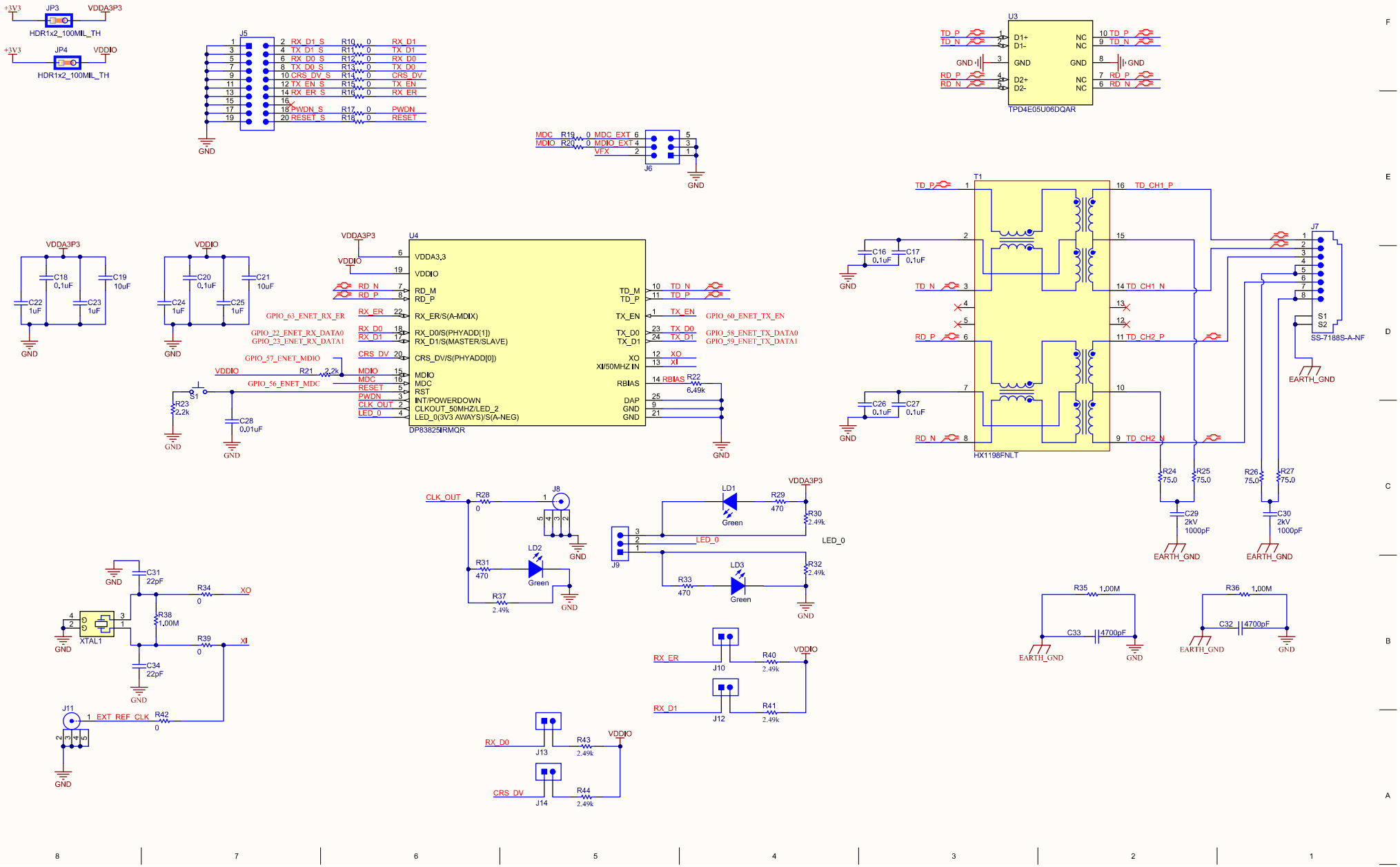
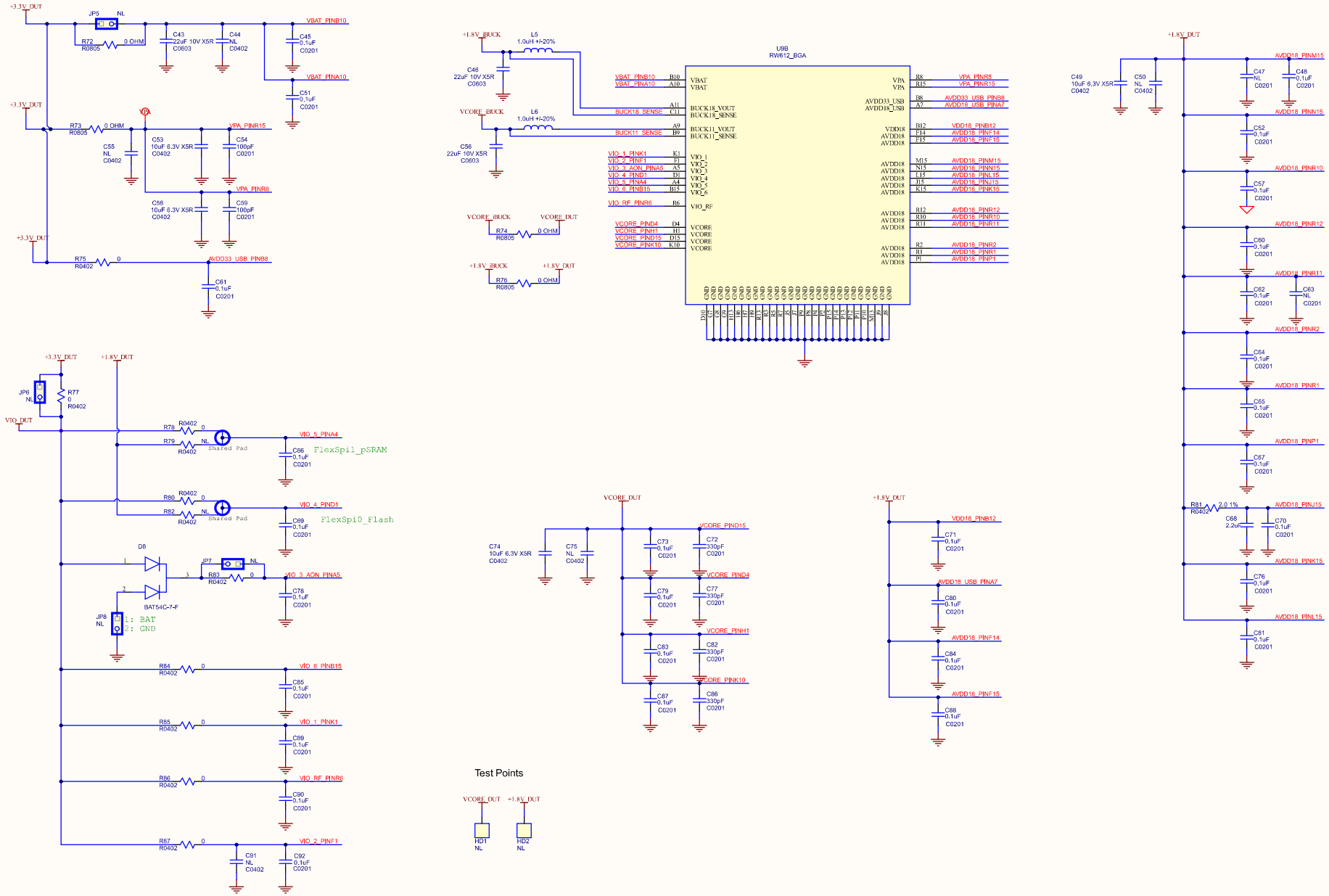
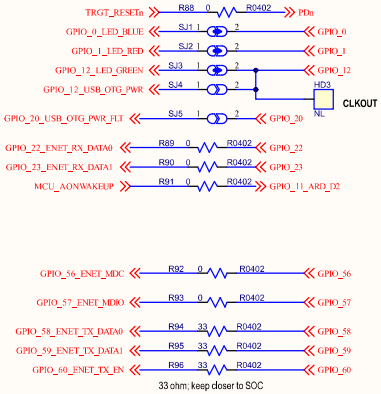
Date: 8-14-2026		Sheet of
File: C:\Users\..\Sheet4_ESP32Wroom.SchDoc		Drawn By:

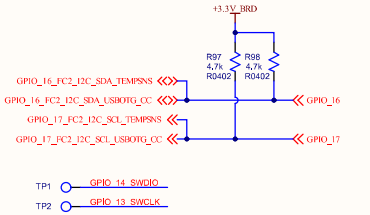

+3V3
JP3
VDDA3P3
HDR1x2_100MIL_TH
+3V3
JP4
VDDIO
HDR1x2_100MIL_TH
J5
RX_D1_S
TX_D1_S
RX_D0_S
TX_D0_S
CRS_DV_S
TX_EN_S
RX_ER_S
PWDN_S
RESET_S
R10 0 RX_D1
R11 0 TX_D1
R12 0 RX_D0
R13 0 TX_D0
R14 0 CRS_DV
R15 0 TX_EN
R16 0 RX_ER
R17 0 PWDN
R18 0 RESET
GND
U3
TD_P
TD_N
RD_P
RD_N
GND
D1+
D1-
D2+
D2-
NC
TPD4E05U06DQAR
MDC R19 0 MDC_EXT
MDIO R20 0 MDIO_EXT
VFX
J6
GND
T1
TD_P
TD_N
RD_P
RD_N
TD_CH1_P
TD_CH1_N
TD_CH2_P
TD_CH2_N
HX1198FNLT
C16 0.1uF
C17 0.1uF
C26 0.1uF
C27 0.1uF
J7
S1
S2
SS-71188S-A-NF
EARTH_GND
VDDA3P3
VDDIO
C18 0.1uF
C19 10uF
C22 1uF
C23 1uF
C20 0.1uF
C21 10uF
C24 1uF
C25 1uF
U4
VDDA3.3
VDDIO
RD_M
RD_P
RX_ER/S(A-MDIX)
RX_D0/S(PHYADD[1])
RX_D1/S(MASTER/SLAVE)
CRS_DV/S(PHYADD[0])
MDIO
MDC
RST
INT/POWERDOWN
CLKOUT_50MHZ/LED_2
LED_0(3V3 AWAYS)/S(A-NEG)
TD_M
TD_P
TX_EN
TX_D0
TX_D1
XO
XI/50MHZ IN
RBIAS
DAP
GND
DP83825IRMQR
GPIO_63_ENET_RX_ER
GPIO_22_ENET_RX_DATA0
GPIO_23_ENET_RX_DATA1
GPIO_57_ENET_MDIO
GPIO_56_ENET_MDC
GPIO_60_ENET_TX_EN
GPIO_58_ENET_TX_DATA0
GPIO_59_ENET_TX_DATA1
R21 2.2k
R22 6.49k
R23 2.2k
C28 0.01uF
S1
R24 75.0
R25 75.0
R26 75.0
R27 75.0
C29 2kV 1000pF
C30 2kV 1000pF
R35 1.00M
C33 4700pF
R36 1.00M
C32 4700pF
CLK_OUT
R28 0
J8
LD1
Green
R29 470
R30 2.49k
LD2
R31 470
R37 2.49k
J9
LED_0
LD3
R33 470
R32 2.49k
VDDA3P3
C31 22pF
R34 0
XO
XTAL1
R38 1.00M
R39 0
XI
C34 22pF
J11
EXT_REF_CLK
R42 0
RX_ER
J10
R40 2.49k
RX_D1
J12
R41 2.49k
RX_D0
J13
R43 2.49k
CRS_DV
J14
R44 2.49k

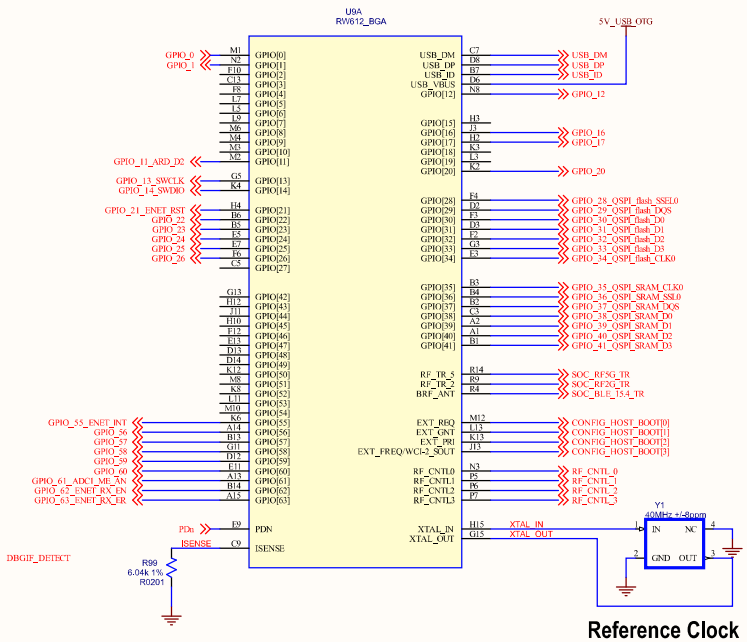
RW612 SOC Power



RW612 SOC Signals

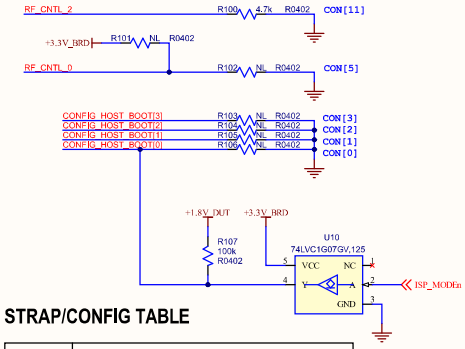






Reference Clock
40MHz XTAL

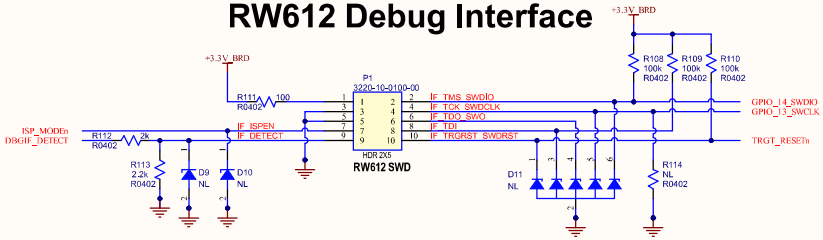
STRAP CONFIG



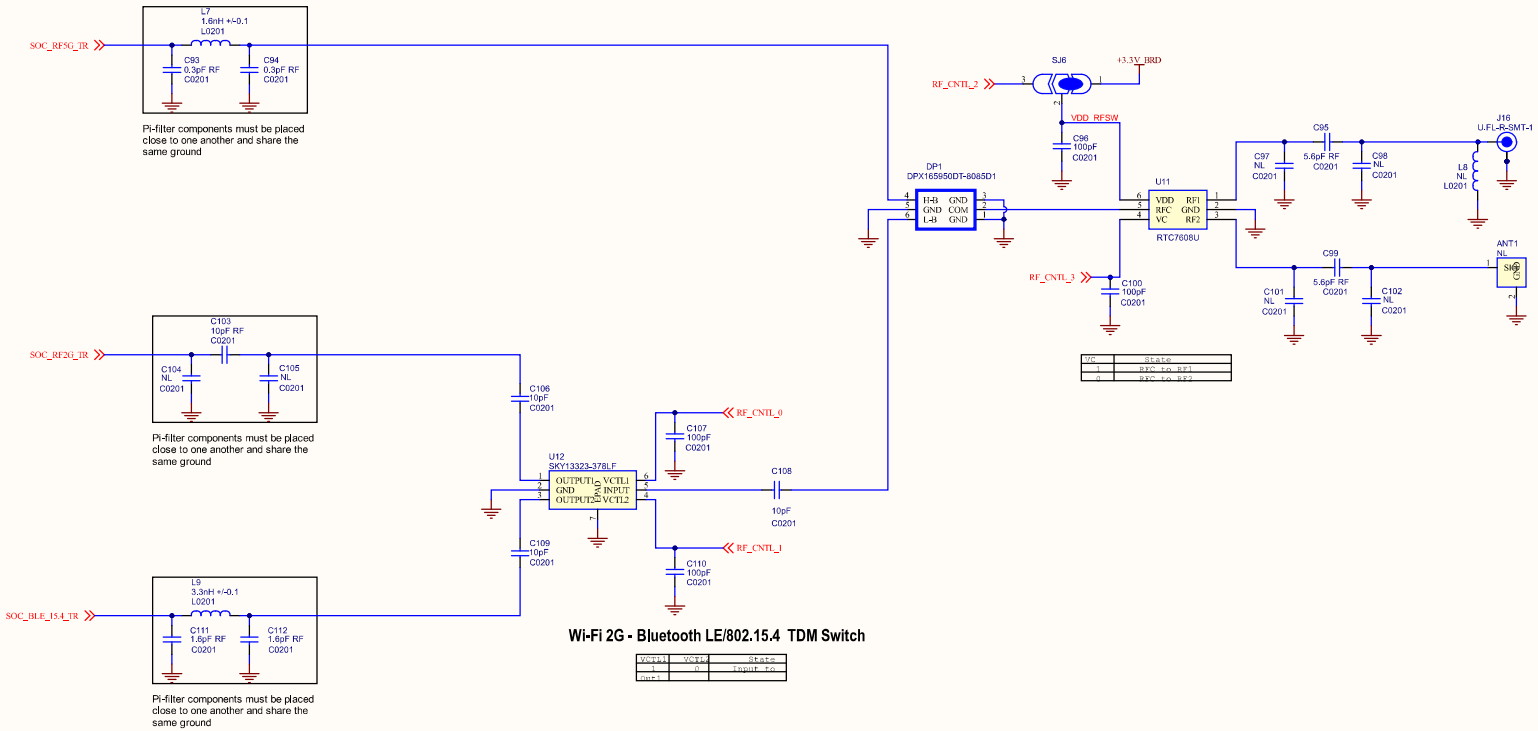
STRAP/CONFIG TABLE

CON	FUNCTION	
[11]	CONFIG_DAP_USE_JTAG : RF_CNTL2 1 : DAP uses JTAG (default) 0 : DAP uses SWD	
[5]	CONFIG XOSC_SEL: 1 : 40 MHz (Default) 0 : 38.4 MHz	
[3:0]	CONFIG HOST BOOT[3:0] : EXT_FREQ,	
	CON[3:0]	Boot
	1111	Boot from QSPI Flash (Default)
	1110	ISP boot (UART/I2C/SPI/USB)
	1101	Serial boot (UART/I2C/SPI/USB)
	1100	ISP boot (SDIO)
	1011	Serial boot (SDIO)
	1010	Reserved

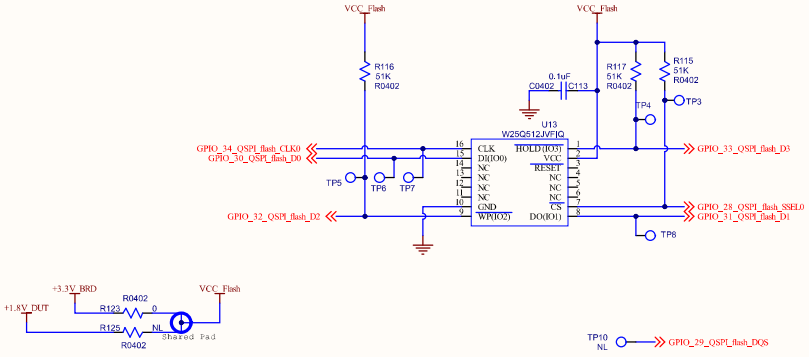
RW612 Debug Interface



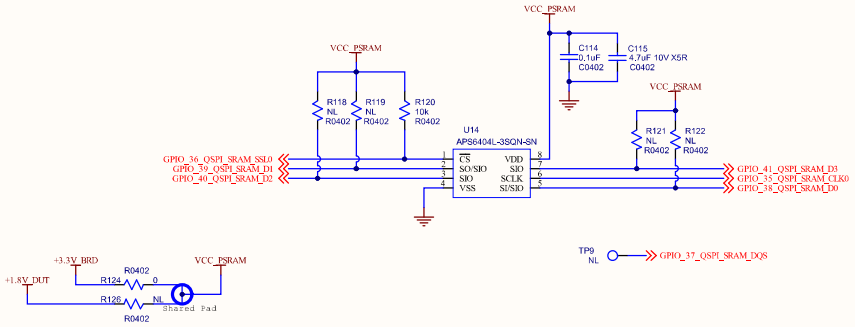
RF Front End


SOC_RF5G_TR
L7
1.6nH +/-0.1
L0201
C93
0.3pF RF
C0201
C94
0.3pF RF
C0201
Pi-filter components must be placed close to one another and share the same ground
SOC_RF2G_TR
C103
10pF RF
C0201
C104
NL
C0201
C105
NL
C0201
Pi-filter components must be placed close to one another and share the same ground
SOC_BLE_15.4_TR
L9
3.3nH +/-0.1
L0201
C111
1.6pF RF
C0201
C112
1.6pF RF
C0201
Pi-filter components must be placed close to one another and share the same ground
C106
10pF
C0201
C109
10pF
C0201
U12
SKY13323-378LF
OUTPUT1
GND
OUTPUT2
VCTL1
INPUT
VCTL2
PAD
C107
100pF
C0201
C110
100pF
C0201
RF_CNTL_0
RF_CNTL_1
C108
10pF
C0201
Wi-Fi 2G - Bluetooth LE/802.15.4 TDM Switch
VCTL1 VCTL2 State
1 0 Input to
SJ6
+3.3V_BRD
RF_CNTL_2
VDD_RFSW
C96
100pF
C0201
DP1
DPX165950DT-8085D1
H-B GND
GND COM
L-B GND
U11
VDD RF1
RFC GND
VC RF2
RTC7608U
RF_CNTL_3
C100
100pF
C0201
VC State
1 RFC to RF1
0 RFC to RF2
C95
5.6pF RF
C0201
C97
NL
C0201
C98
NL
C0201
J16
U.FL-R-SMT-1
L8
NL
L0201
C99
5.6pF RF
C0201
C101
NL
C0201
C102
NL
C0201
ANT1
NL
SIG
GND

QSPI Flash

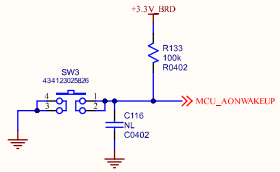


PSRAM

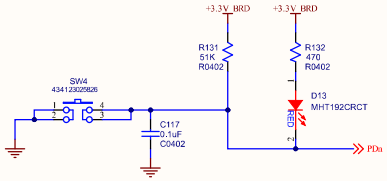


Push Buttons

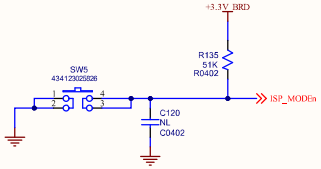
MCU WAKEUP



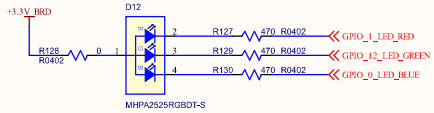
PDn / RESET



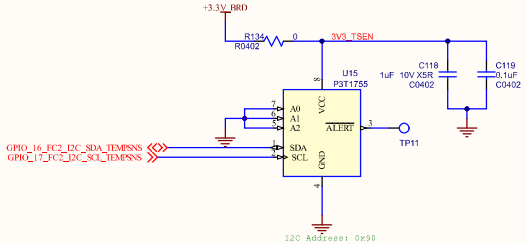
ISP



RGB LED



TEMPERATURE SENSOR



H1 1 GND

H2 1 GND

H3 1 GND

H4 1 EARTH_GND

SH-J1 SH-J2 SH-J3 SH-J4 SH-J5

H5 1902C

H6 1902C

H7 1902C

H8 1902C

FID1 FID2 FID3 FID4 FID5 FID6

PCB Number:
PCB Rev:

PCB LOGO
Texas Instruments

CE Mark

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

You should delete the nylon screws/standoffs and/or the bumpons as needed for your design (or substitute other parts from Hardware.IntLib). Bumpons are cheaper, but provide less clearance.

Deleting anything else from this page may result in your EVM submission being rejected (until you add them back).

Update the Label Text in the Label Table as needed for each Assembly Variant.

You should delete this note too.

PCB Label

Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Variant/Label Table	
Variant	HSDC045A
001	DP83825EVM

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.