**TI Case # CS0272390 - Meteorcomm, LLC – Trouble with DP83867IRPAPT certification**

We are testing for compliance with IEEE 802.3. The only test that fails is the peak voltage test for points A and B of the test waveform - everything else passes.  The amplitude control register is not documented anywhere in the product literature, but I was told about it by the support engineer that was handling my case.  Measuring the peak voltage per the spec is a fairly involved process - lots of averaging and such, that the compliance application on my scope deals with.  In order to measure it, you need to load the RJ45 channels with 100 ohms each and use a differential probe.

Writing to it is fairly simple, but needs to be done from the UBoot prompt using the mdio command set.  It gets complicated by the fact that the register is in the extended register set, so you have to use indirect addressing to set or read it.  The register address is 0x009F, and it's default value is 0xBBBB.  Here is an example of setting the register:

mdio write ethernet@ff0b0000 0x000D   0x001F     // enables extended register access
mdio write ethernet@ff0b0000 0x000E   0x009f      // set address of target register
mdio write ethernet@ff0b0000 0x000D   0x401F    // set pointer to data register
mdio write ethernet@ff0b0000 0x000E   0xFFFF    // set target data

and reading it back:

mdio write ethernet@ff0b0000 0x000D   0x001F     // enables extended register access
mdio write ethernet@ff0b0000 0x000E   0x009f      // set address of target register
mdio write ethernet@ff0b0000 0x000D   0x401F    // set pointer to data register
mdio read ethernet@ff0b0000 0x000e                    // read value

This should read back a value of 0xFFFF if everything went right.

There are 4 channels to each ethernet interface, and each nibble of the data word controls one of them, so it is theoretically possible to tune on a per-channel basis.  The valid range for the amplitude register is 0x0000 to 0xFFFF, but on the eval board, I didn't see much if any change for values less than 0x6666.

In order to activate the test waveform, you need to put the PHY in test mode 1:

mdio write ethernet@ff0b0000 0x001F   0x8000
mdio write ethernet@ff0b0000 0x0000   0x0140
mdio write ethernet@ff0b0000 0x0010   0x5008
mdio write ethernet@ff0b0000 0x0009   0x3B00
mdio write ethernet@ff0b0000 0x000D   0x001F
mdio write ethernet@ff0b0000 0x000E   0x0025
mdio write ethernet@ff0b0000 0x000D   0x401F
mdio write ethernet@ff0b0000 0x000E   0x0480

where ff0b0000 is the base address for ETH0,  ff0c0000 is ETH1, and ff0e000 eth Maint.