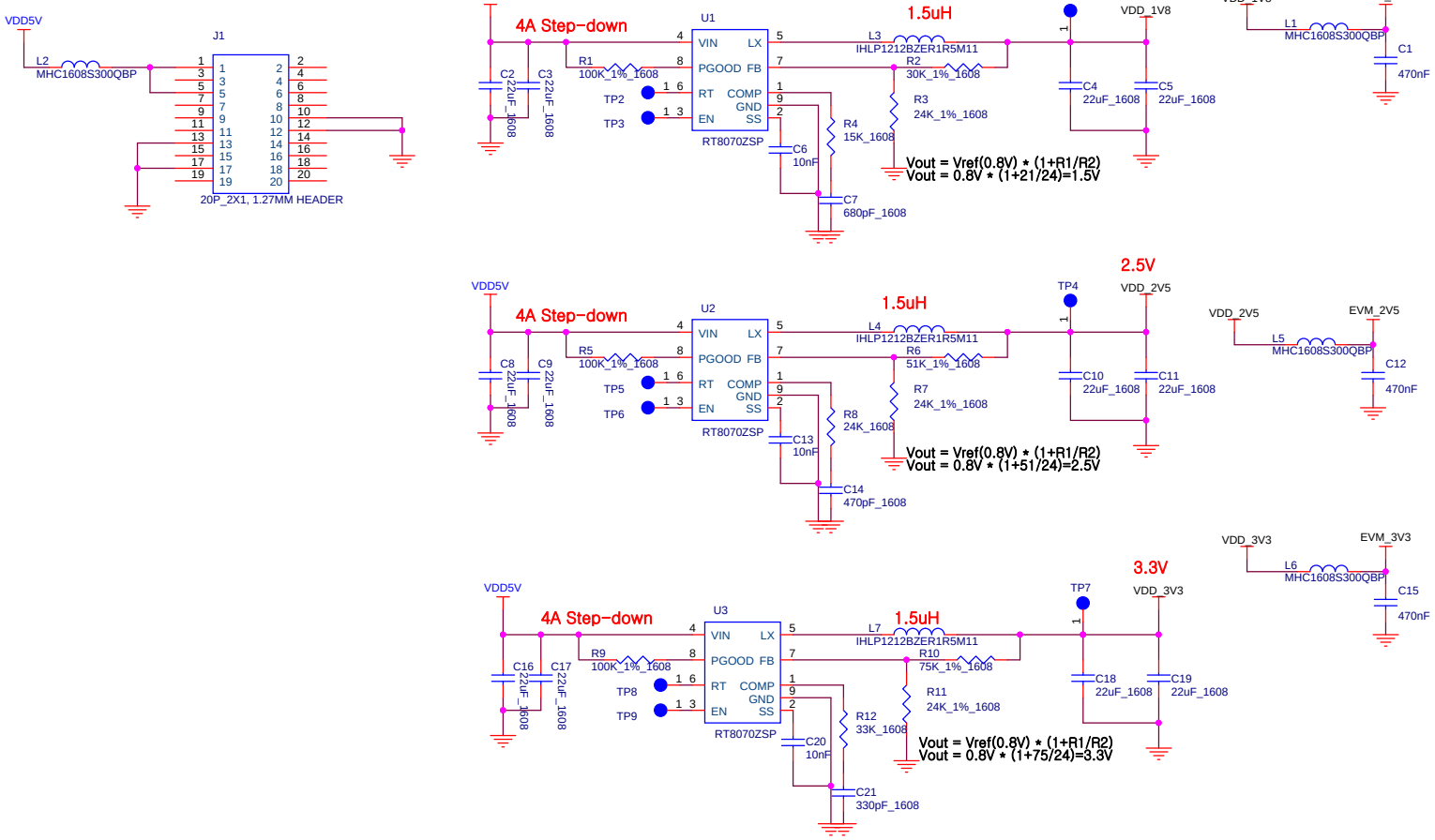
Ethernet B/D- Power



GNSD		
Title: SX-G100C DEBUG		
Size: A3	Document Number: MAIN POWER	Rev: V0.1
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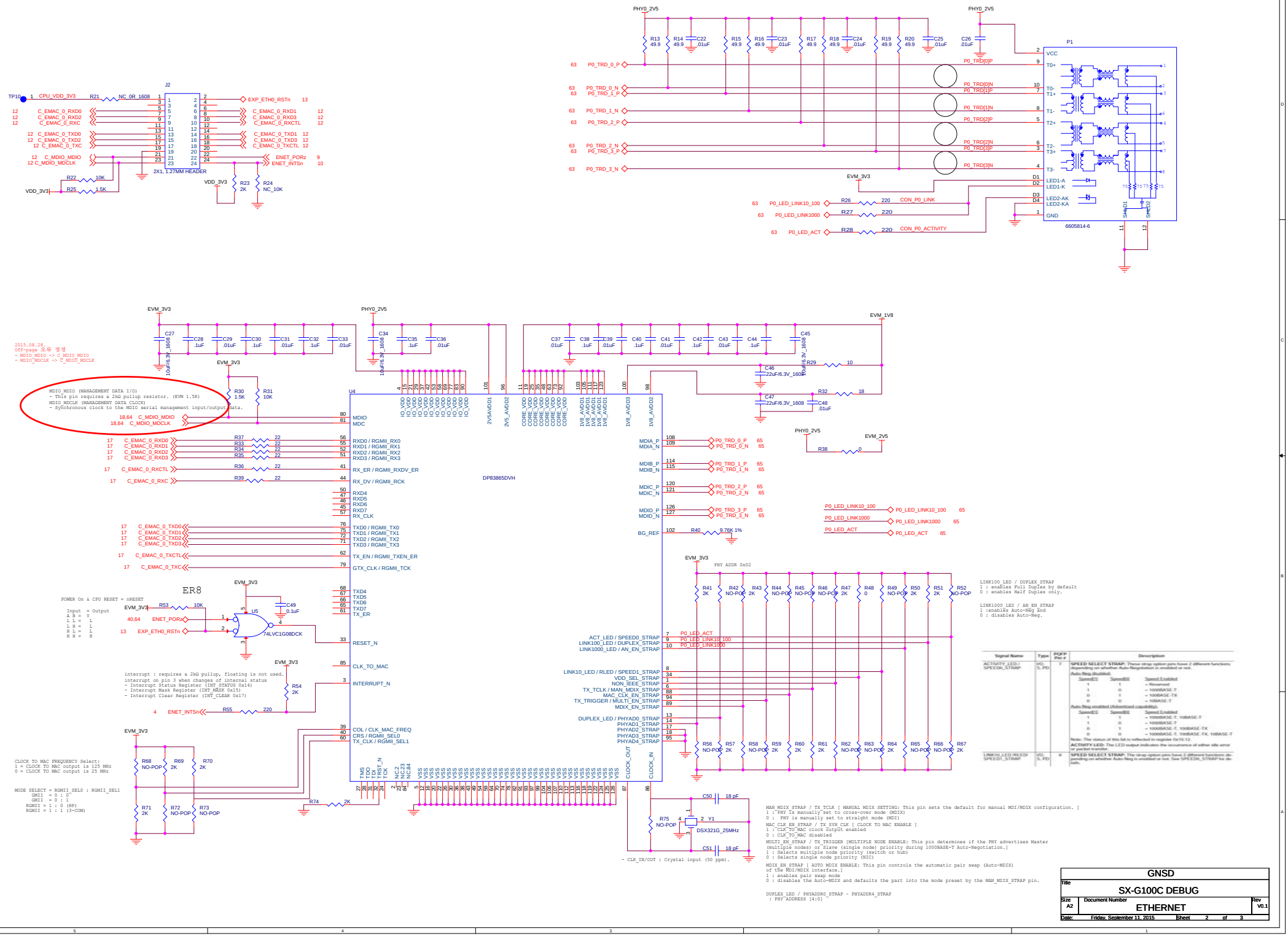
J2
2X1, 1.27MM HEADER
P1
6605814-6
U4
DP83865DVH
U5
74LVC1G08DCK
ER8
Y1
DSX321G_25MHz
2015.08.28.
Off-page 오류 정정
- MDIO_MDIO -> C_MDIO_MDIO
- MDIO_MDCLK -> C_MDIO_MDCLK
MDIO_MDIO (MANAGEMENT DATA I/O)
- This pin requires a 2kΩ pullup resistor. (EVM 1.5K)
MDIO_MDCLK (MANAGEMENT DATA CLOCK)
- Synchronous clock to the MDIO serial management input/output data.
POWER On & CPU RESET = nRESET
interrupt : requires a 2kΩ pullup, floating is not used.
interrupt on pin 3 when changes of internal status
- Interrupt Status Register (INT_STATUS 0x14)
- Interrupt Mask Register (INT_MASK 0x15)
- Interrupt Clear Register (INT_CLEAR 0x17)
CLOCK TO MAC FREQUENCY Select:
1 = CLOCK TO MAC output is 125 MHz
0 = CLOCK TO MAC output is 25 MHz
MODE SELECT = RGMII_SEL0 : RGMII_SEL1
GMII = 0 : 0
GMII = 0 : 1
RGMII = 1 : 0 (HP)
RGMII = 1 : 1 (3-COM)
- CLK_IN/OUT : Crystal input (50 ppm).
LINK100_LED / DUPLEX_STRAP
1 : enables Full Duplex by default
0 : enables Half Duplex only.
LINK1000_LED / AN_EN_STRAP
1 :enables Auto-Neg and
0 : disables Auto-Neg.
MAN_MDIX_STRAP / TX_TCLK [MANUAL MDIX SETTING: This pin sets the default for manual MDI/MDIX configuration.]
1 : PHY is manually set to cross-over mode (MDIX)
0 : PHY is manually set to straight mode (MDI)
MAC_CLK_EN_STRAP / TX_SYN_CLK [CLOCK TO MAC ENABLE]
1 : CLK_TO_MAC clock output enabled
0 : CLK_TO_MAC disabled
MULTI_EN_STRAP / TX_TRIGGER [MULTIPLE NODE ENABLE: This pin determines if the PHY advertises Master (multiple nodes) or Slave (single node) priority during 1000BASE-T Auto-Negotiation.]
1 : Selects multiple node priority (switch or hub)
0 : Selects single node priority (NIC)
MDIX_EN_STRAP [AUTO MDIX ENABLE: This pin controls the automatic pair swap (Auto-MDIX) of the MDI/MDIX interface.]
1 : enables pair swap mode
0 : disables the Auto-MDIX and defaults the part into the mode preset by the MAN_MDIX_STRAP pin.
DUPLEX_LED / PHYADDR0_STRAP ~ PHYADDR4_STRAP
: PHY ADDRESS [4:0]
GNSD
Title
SX-G100C DEBUG
Size A2
Document Number
ETHERNET
Rev V0.1
Date: Friday, September 11, 2015
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