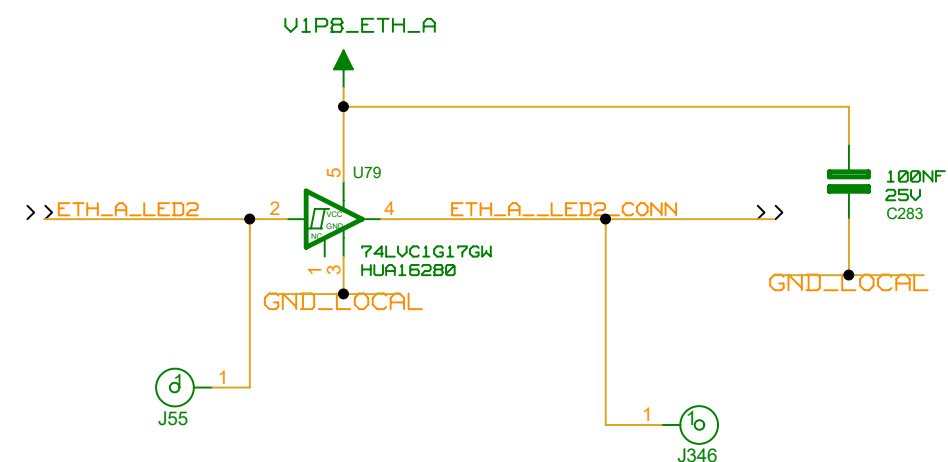
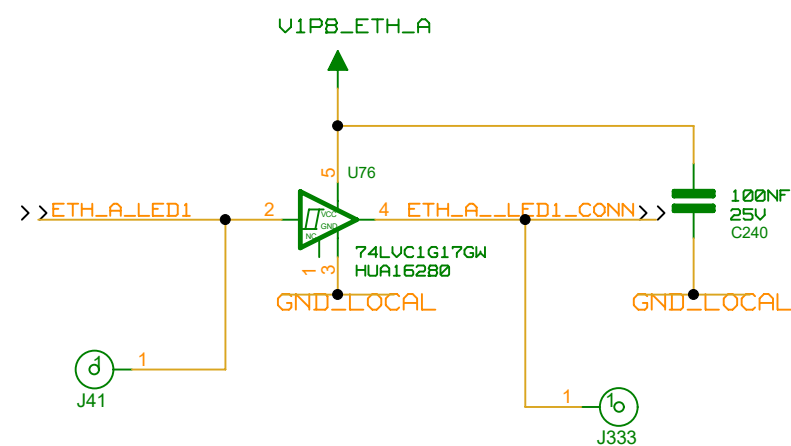
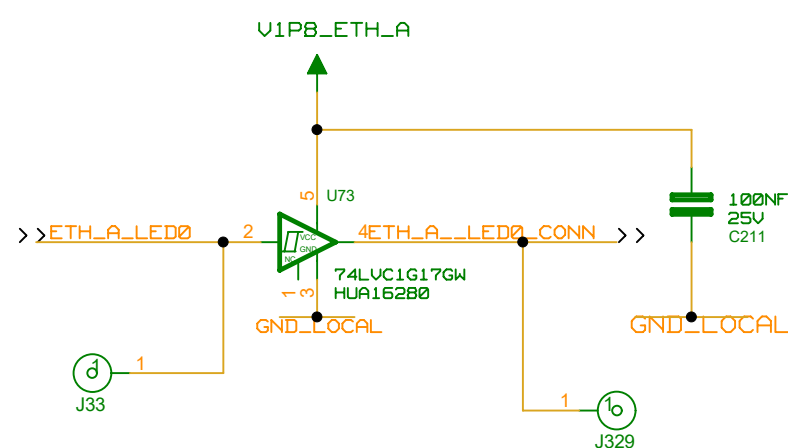
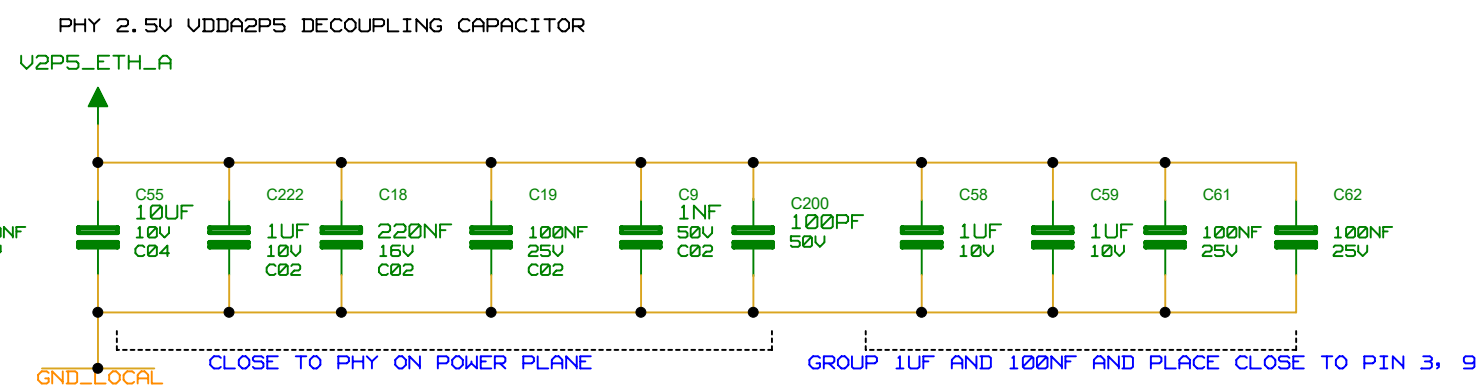
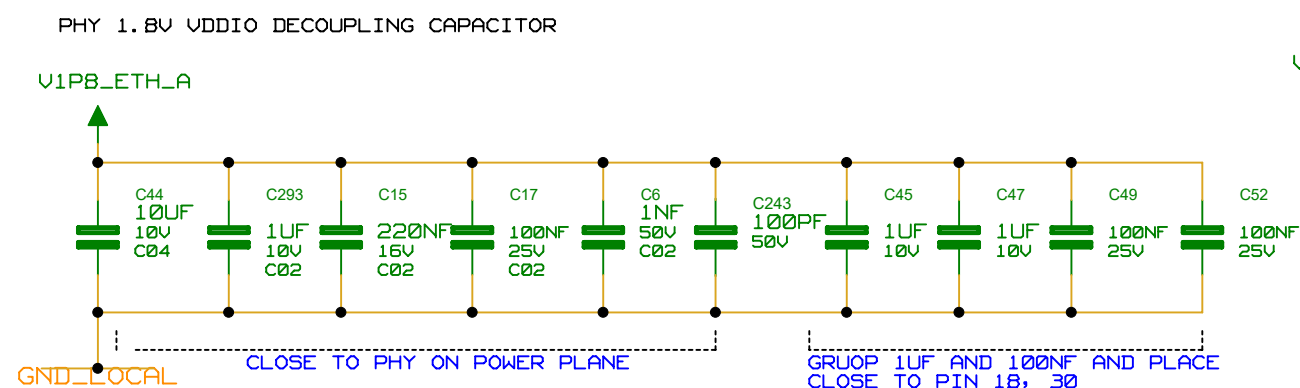
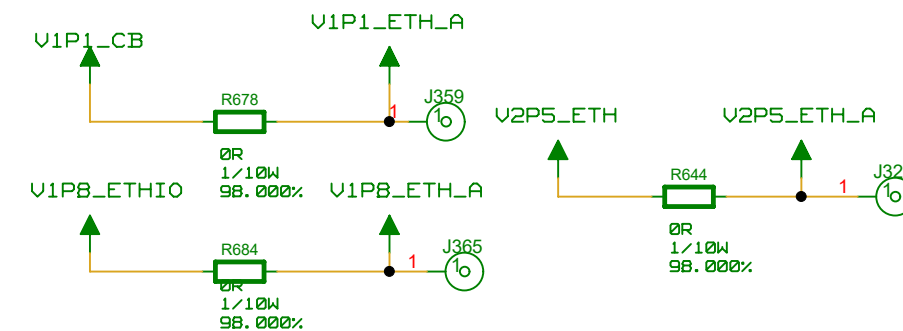
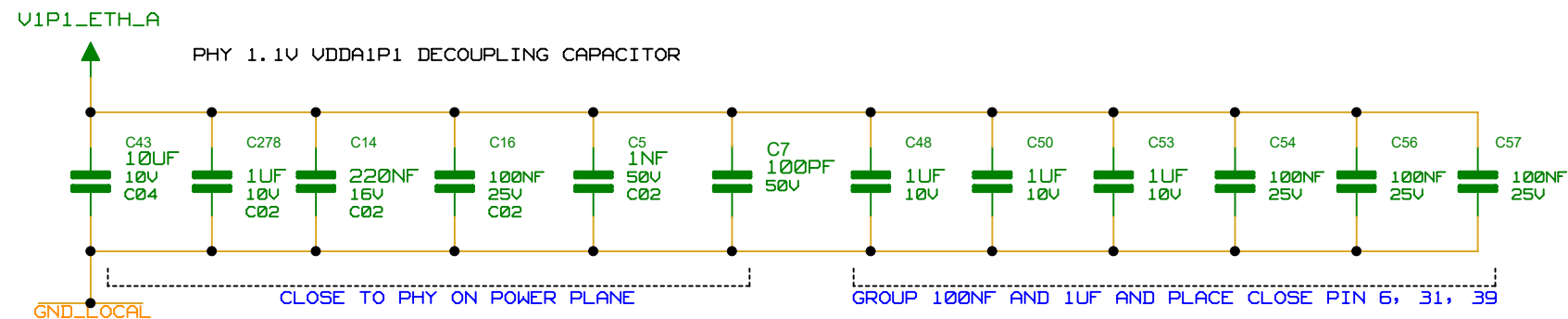


ETHERNET- A DECAPS AND LED BUFFERS



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PCB SOM AM64 SIZE M CARRIER BOARD
PCB SOM AM64 SIZE M CARRIER BOARD
A60-GENERIC SCHEMATIC

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BLOCK NAME = top

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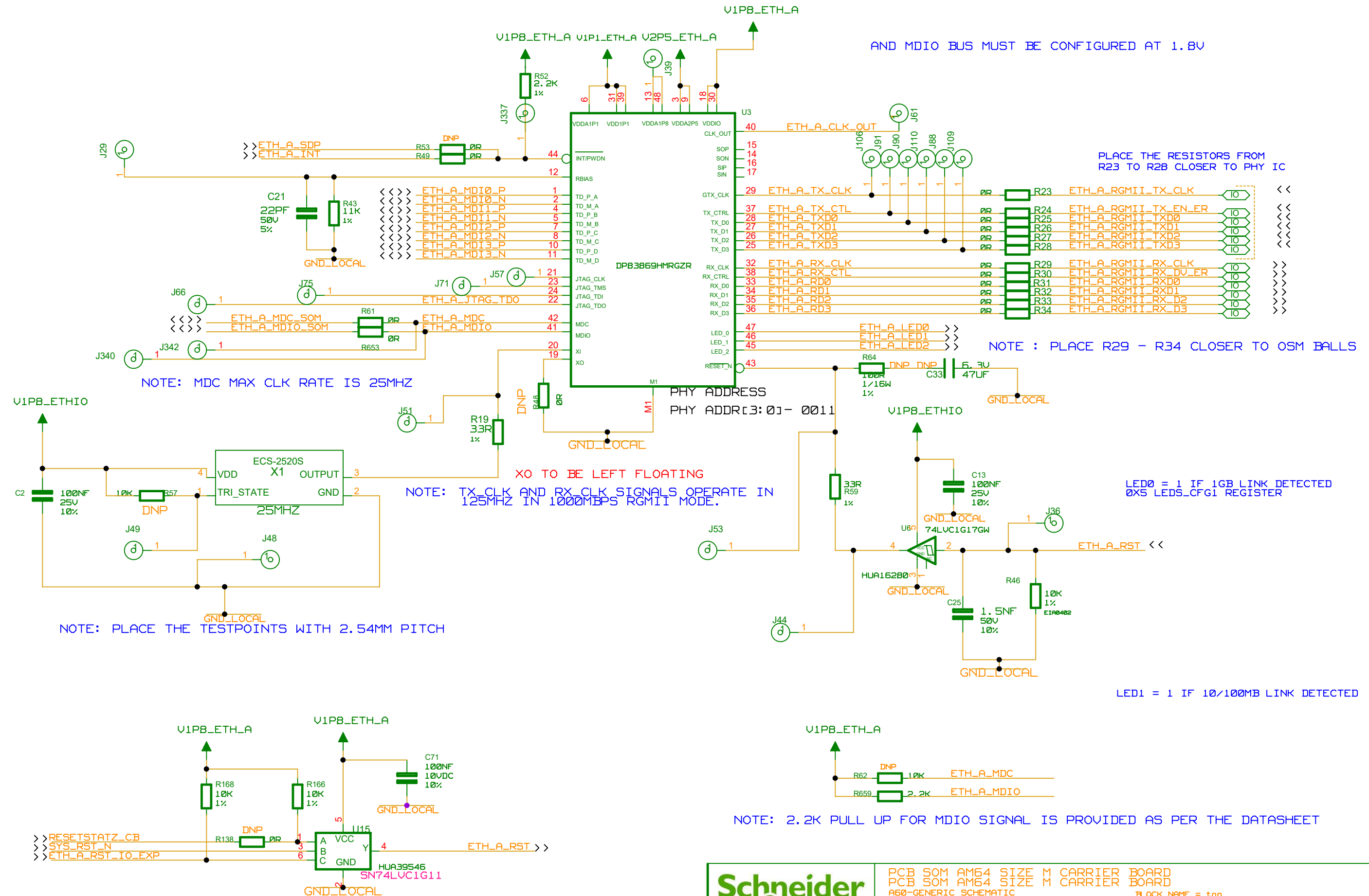
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14/55

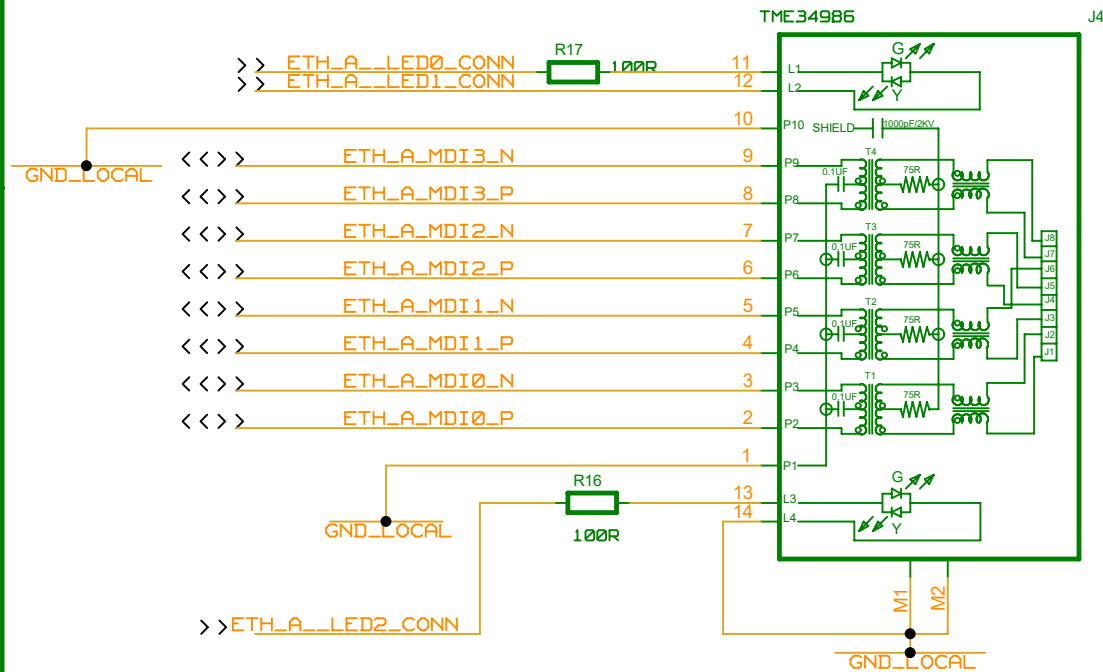
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STATE :

ETHERNET- A



ETHERNET- A CONNECTOR AND STRAPS



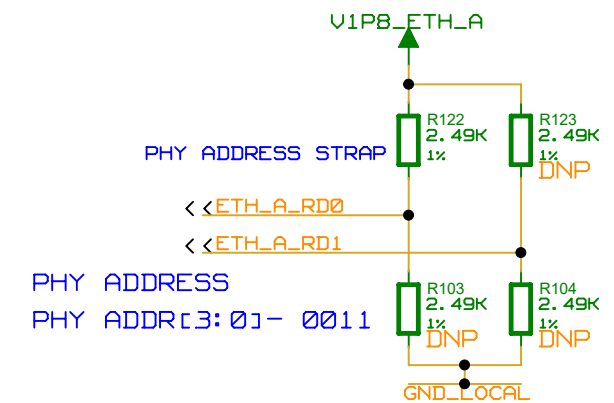
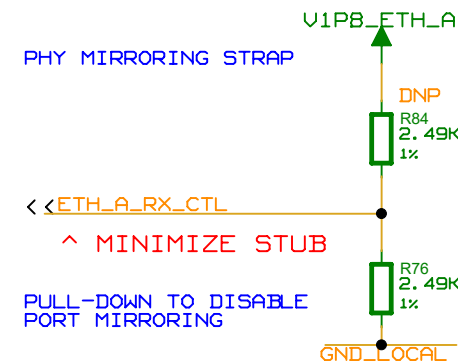
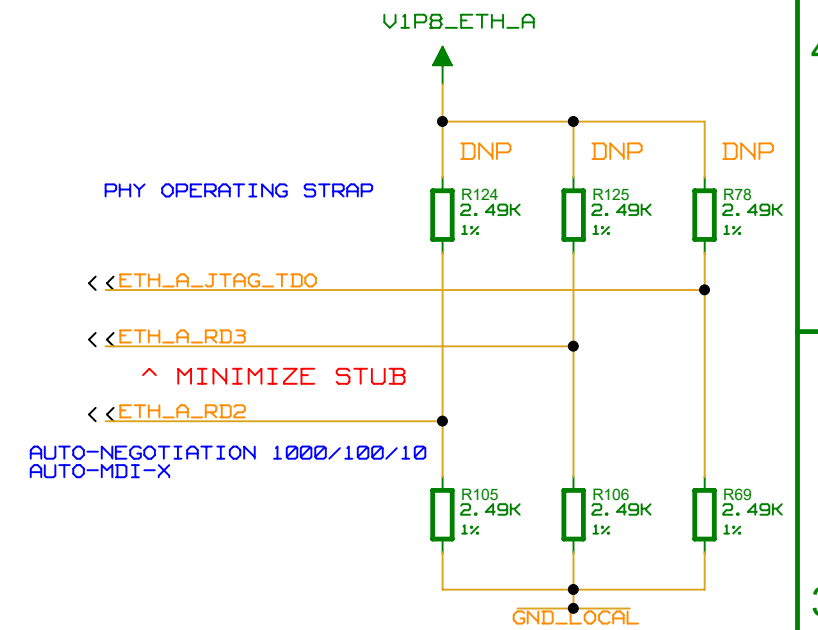
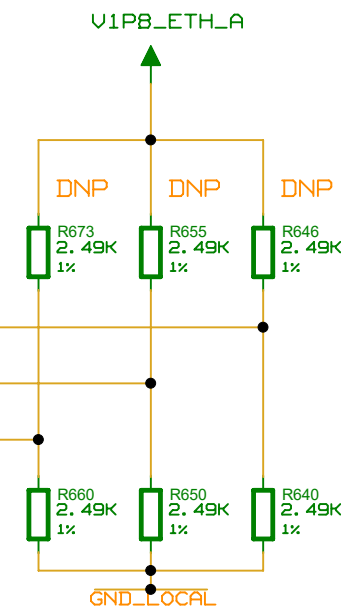
PHY AUTO-NEGOTIATION STRAP

<< ETH_A_LED0

<< ETH_A_LED1

<< ETH_A_LED2

RGMII TO COPPER(1000 BASE-T
100BASE-TX/10BASE-TE)



7.5.1.2 Strap for DP83869HM Functional Mode Selection

Table 7-12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMO DE[2]	OPMO DE[1]	OPMO DE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
				1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-TX to 100Base-FX
RX_D2	OPMODE[2]	35	0	1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

Table 7-14. Copper Ethernet Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	ANEG_DIS	ANEGS EL_1	ANEGS EL_0	FUNCTION
LED_0	ANEG_DIS	47	0	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	0	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	1	NA
				1	0	0	NA
				1	0	1	NA
LED_2	ANEGSEL_1	45	0	1	1	0	Forced 100M, full duplex, MDI mode
				1	1	1	Forced 100M, full duplex, MDI-X mode
RX_CTRL	MIRROR_EN	38	0		0		Port Mirroring Disabled
					1		Port Mirroring Enabled

Table 7-11. PHY Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD1	PHY_ADD0
				MODE 0	0
				MODE 1	0
				MODE 2	1
				MODE 3	0
				MODE 3	1

PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD3	PHY_ADD2
				MODE 0	0
				MODE 1	0
				MODE 2	1
				MODE 3	0
				MODE 3	1

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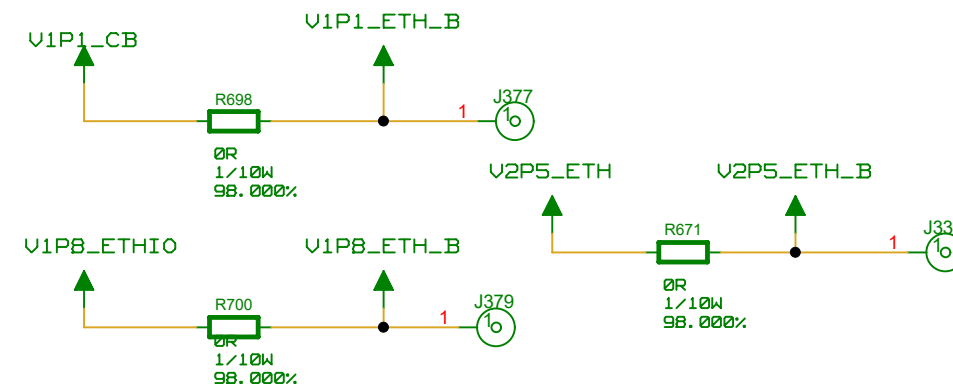
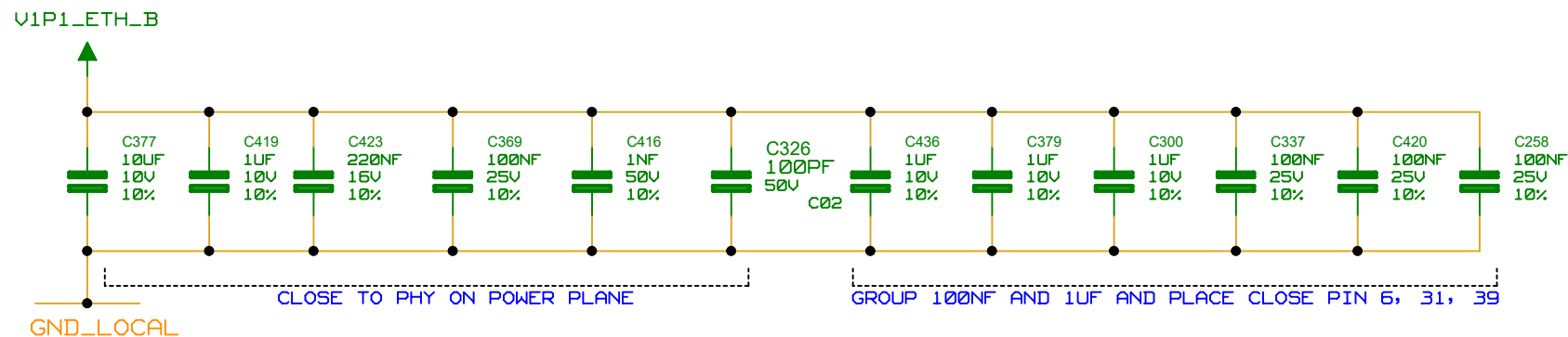
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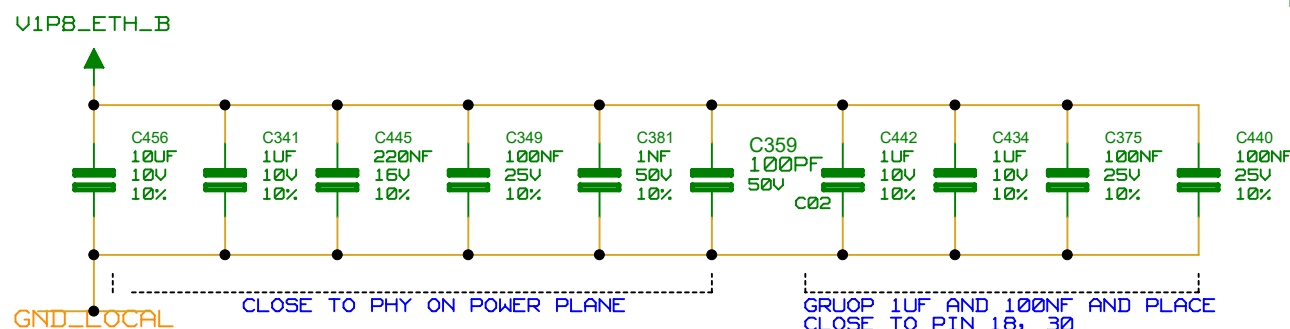
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ETHERNET- B DECAPS AND LED BUFFERS

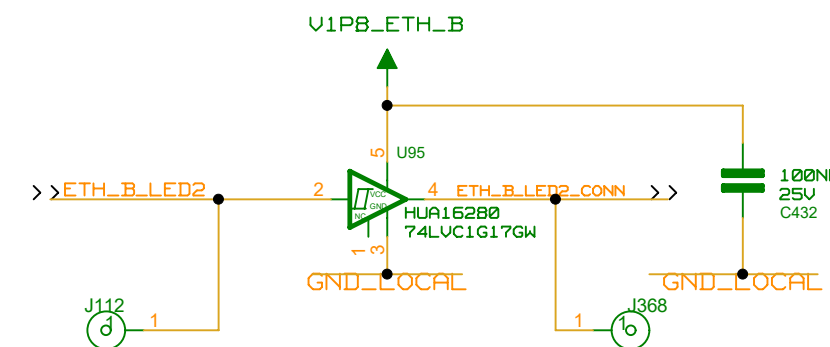
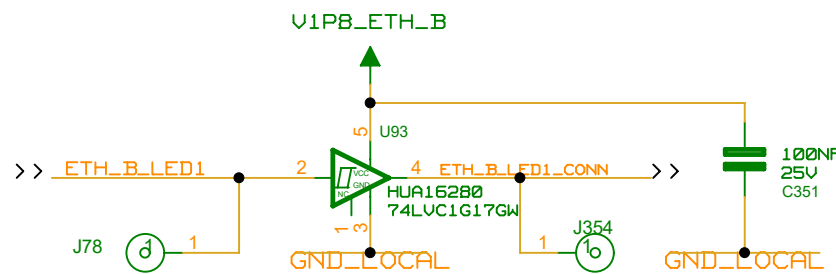
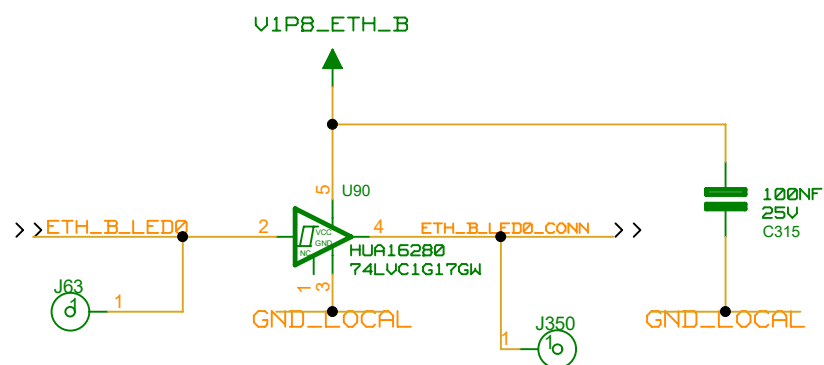
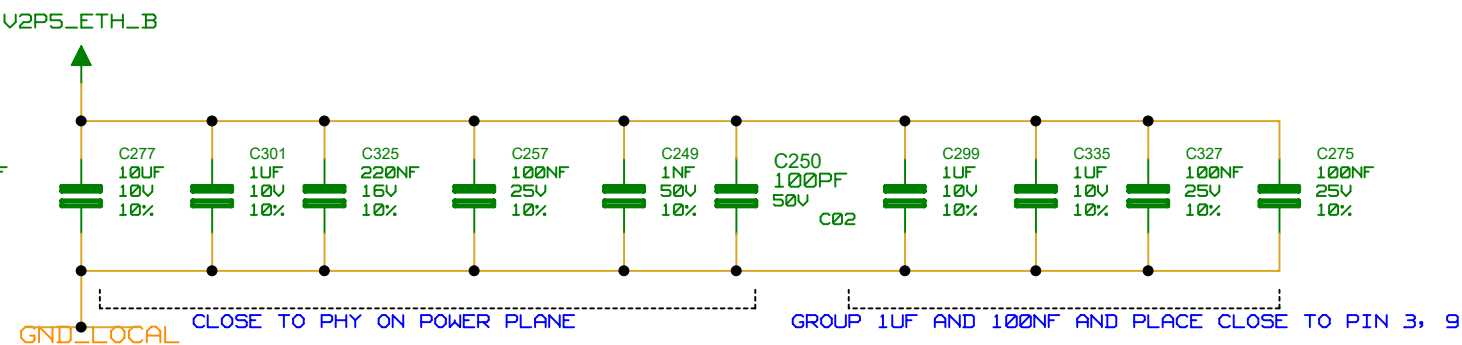
PHY 1.1V VDDA1P1 DECOUPLING CAPACITOR



PHY 1.8V VDDIO DECOUPLING CAPACITOR



PHY 2.5V VDDA2P5 DECOUPLING CAPACITOR



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PCB SOM AM64 SIZE M CARRIER BOARD
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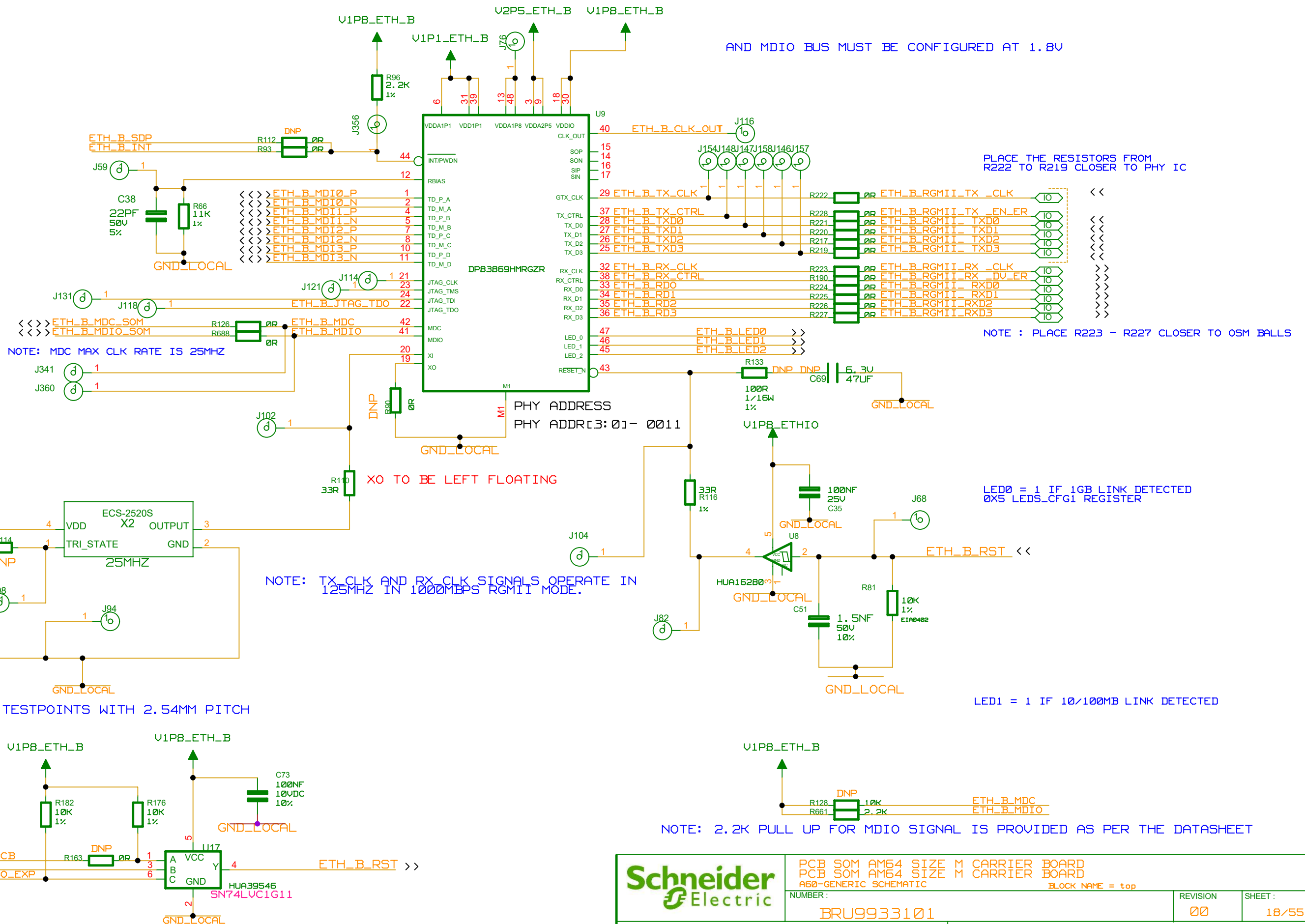
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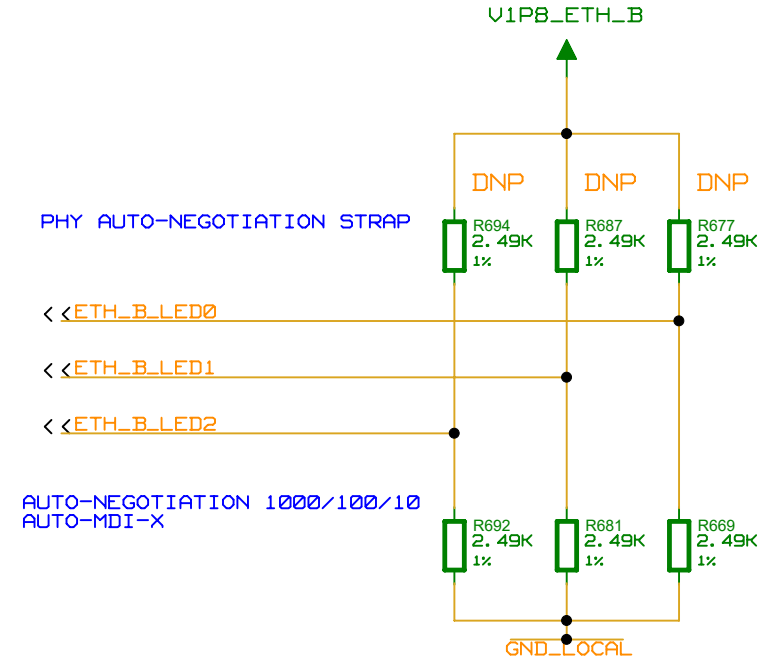
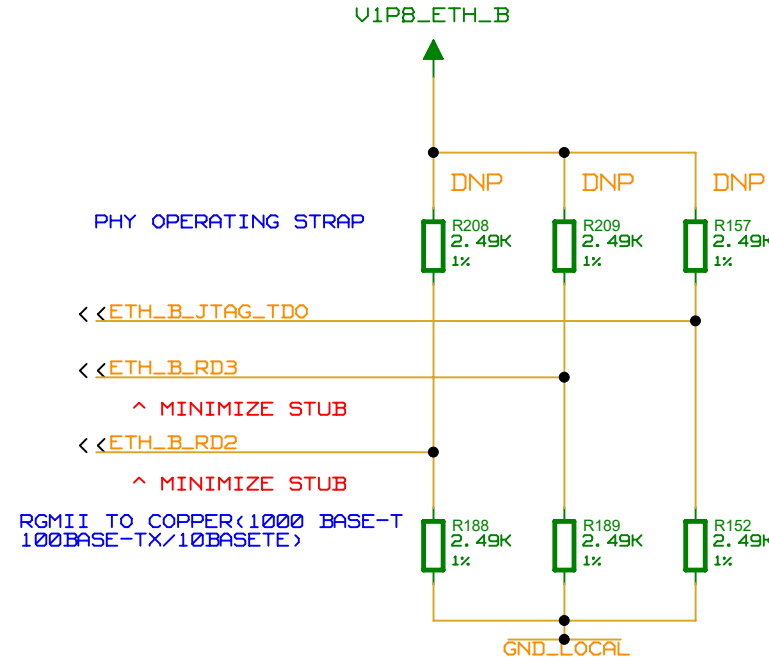
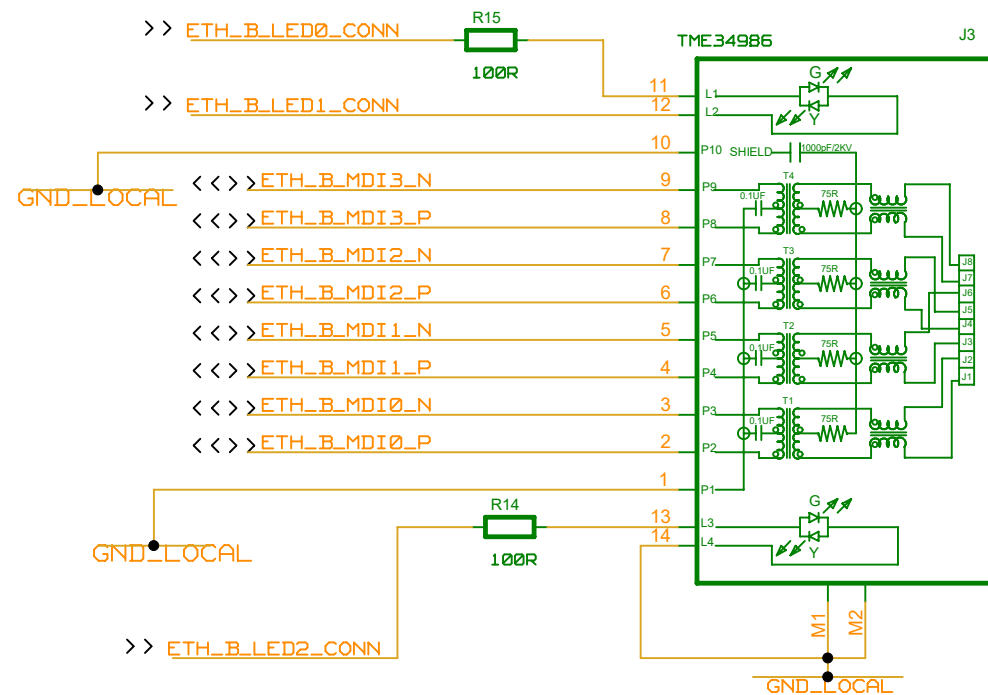
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STATE :

ETHERNET- B



ETHERNET- B CONNECTOR AND STRAPS



7.5.1.2 Strap for DP83869HM Functional Mode Selection

Table 7-12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMO DE[2]	OPMO DE[1]	OPMO DE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
				1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-TX to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

7.5.1.4 Straps for RGMII/SGMII to Copper

Table 7-14. Copper Ethernet Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	ANEGS EL_1	ANEGS EL_0	FUNCTION
LED_0	ANEG_DIS	47	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	NA
				1	0	NA
				1	0	NA
LED_2	ANEGSEL_1	45	0	1	1	Forced 100M, full duplex, MDI mode
				1	1	Forced 100M, full duplex, MDI-X mode
				0	0	Port Mirroring Disabled
				1	1	Port Mirroring Enabled

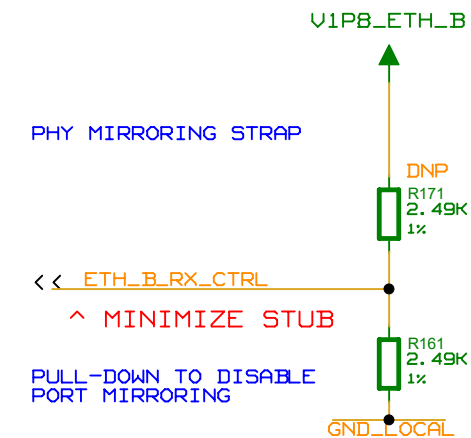
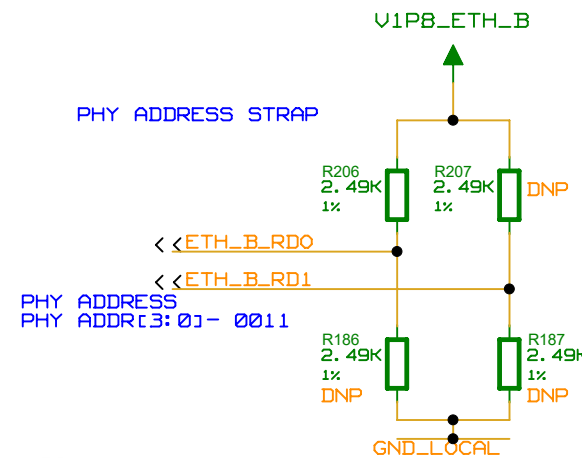


Table 7-11. PHY Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD1	PHY_ADD0
				MODE 0	0
				MODE 1	1
				MODE 2	0
				MODE 3	1

PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD3	PHY_ADD2
				MODE 0	0
				MODE 1	1
				MODE 2	0
				MODE 3	1

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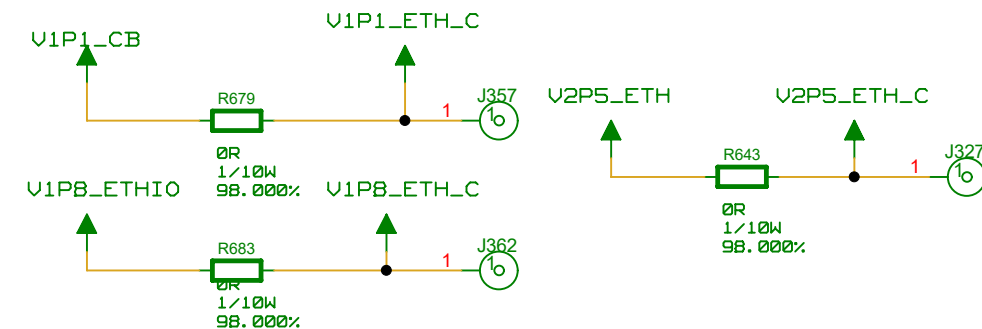
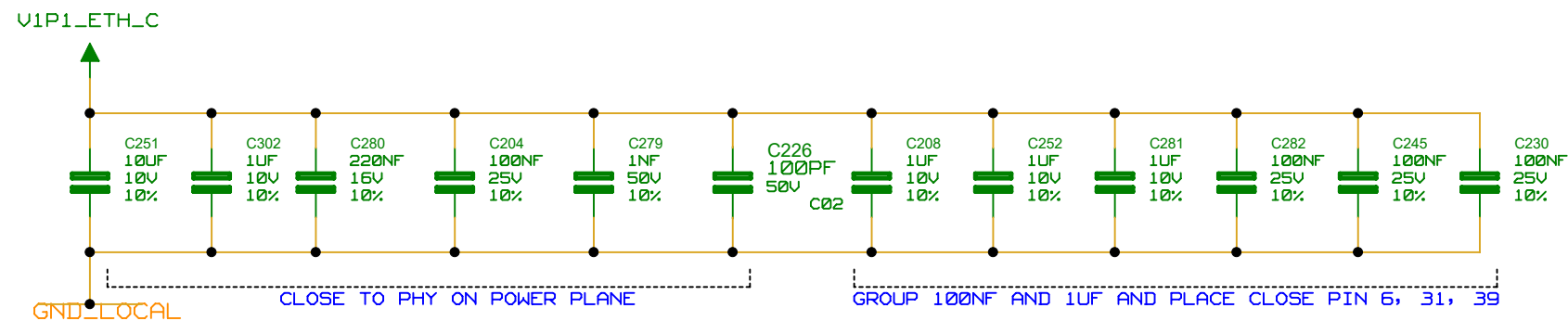
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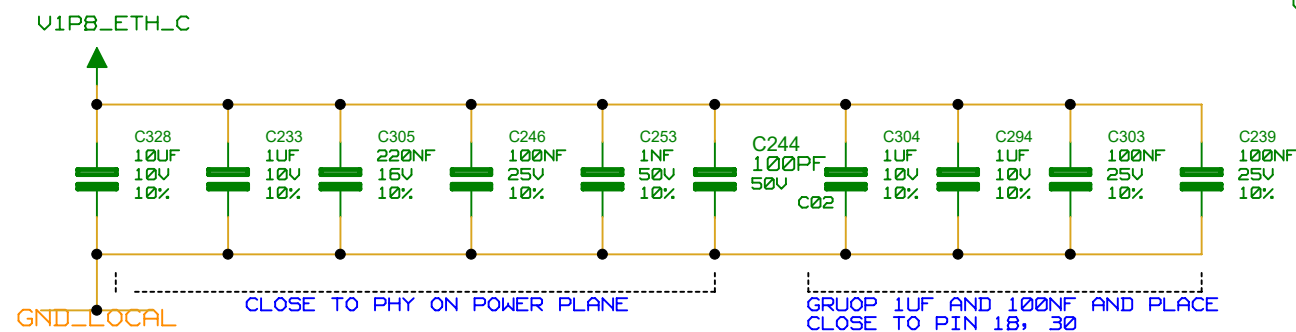
STATE :

ETHERNET- C DECAPS AND LED BUFFERS

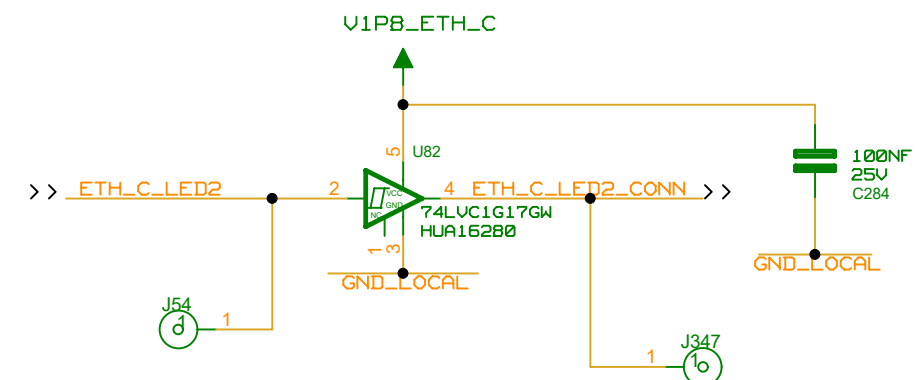
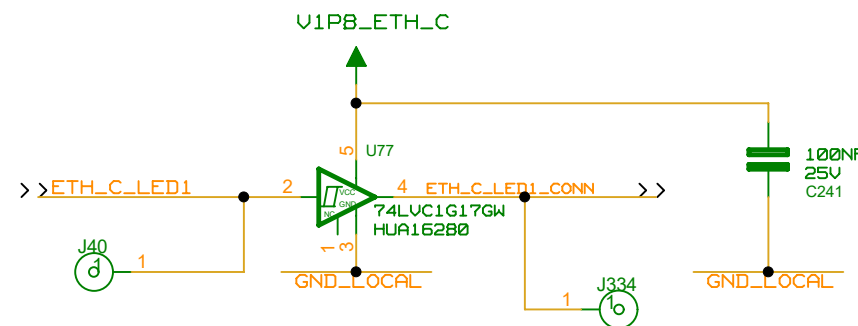
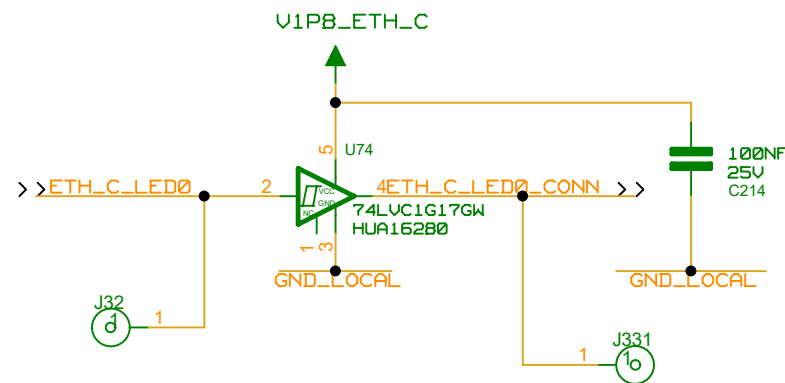
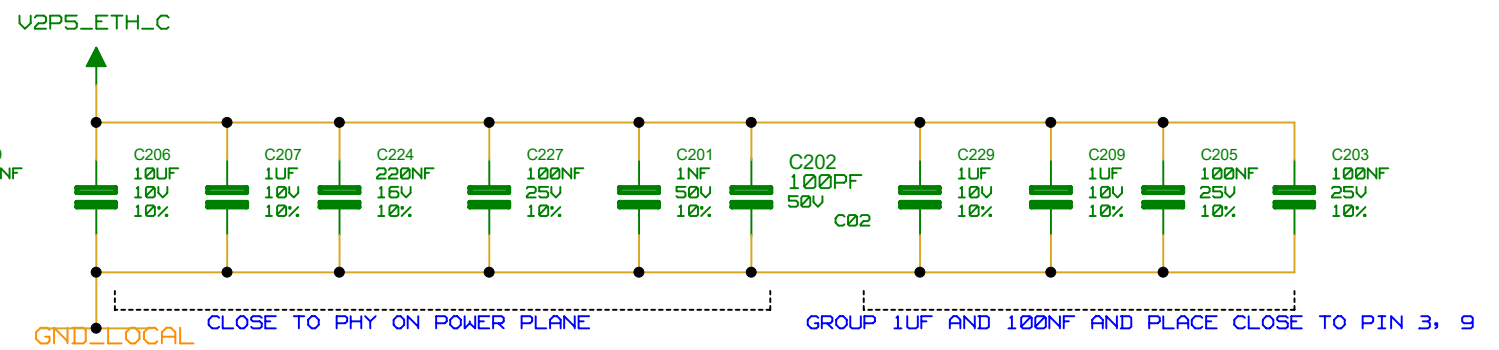
PHY 1.1V VDDA1P1 DECOUPLING CAPACITOR



PHY 1.8V VDDIO DECOUPLING CAPACITOR



PHY 2.5V VDDA2P5 DECOUPLING CAPACITOR



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PCB SOM AM64 SIZE M CARRIER BOARD
PCB SOM AM64 SIZE M CARRIER BOARD
A60-GENERIC SCHEMATIC

NUMBER :

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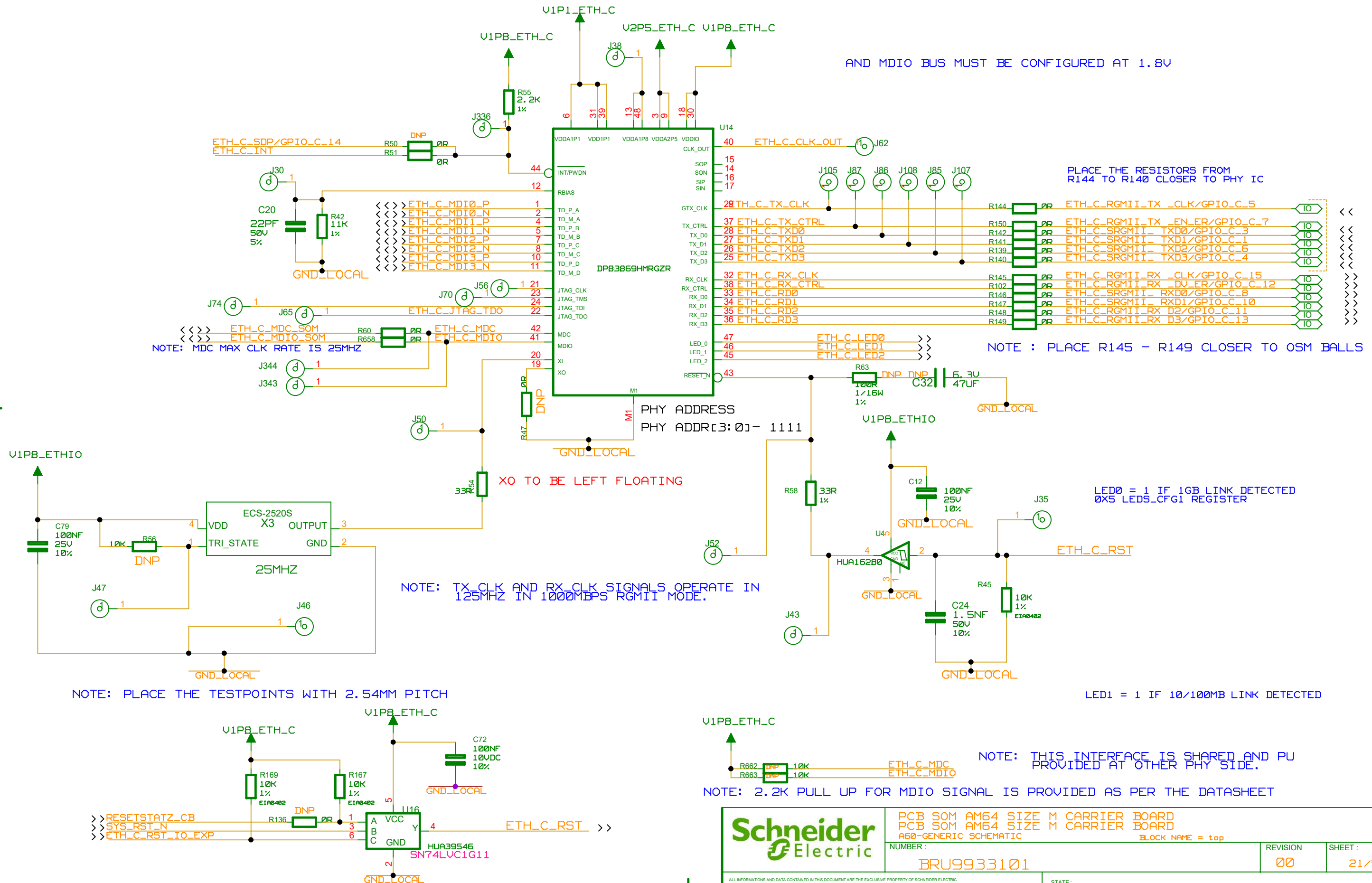
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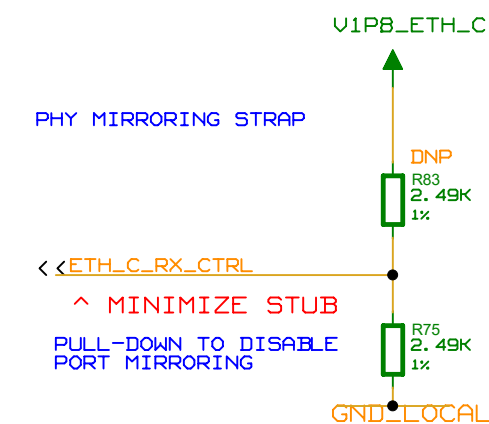
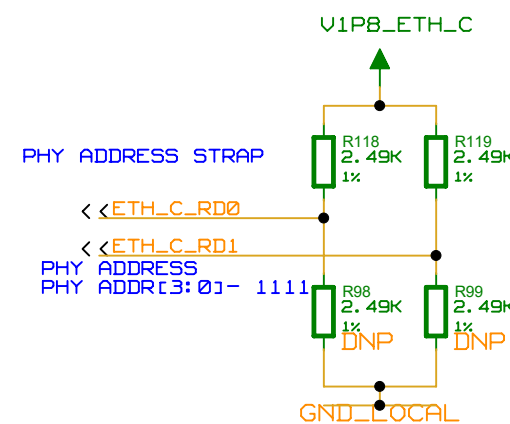
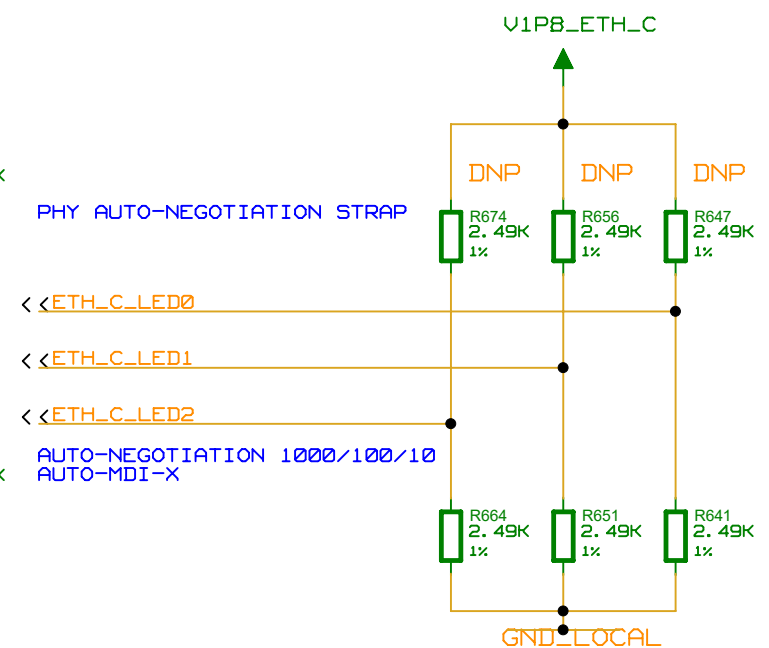
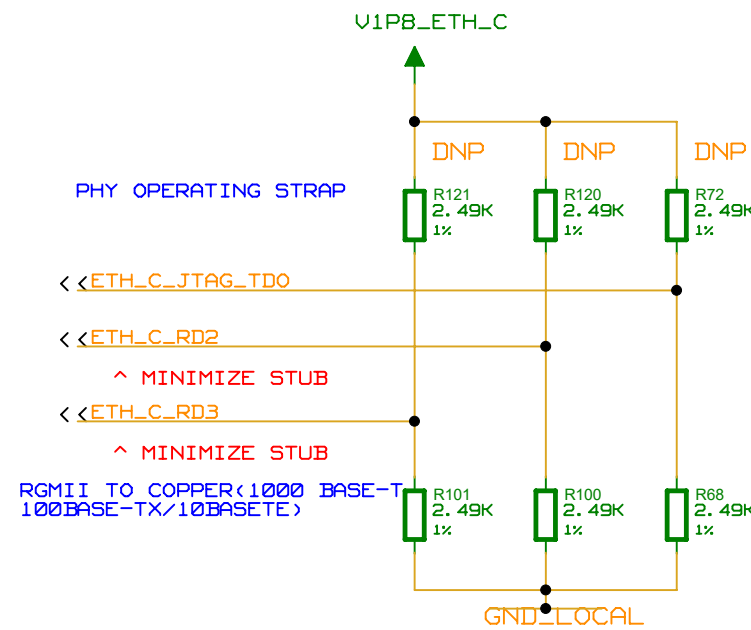
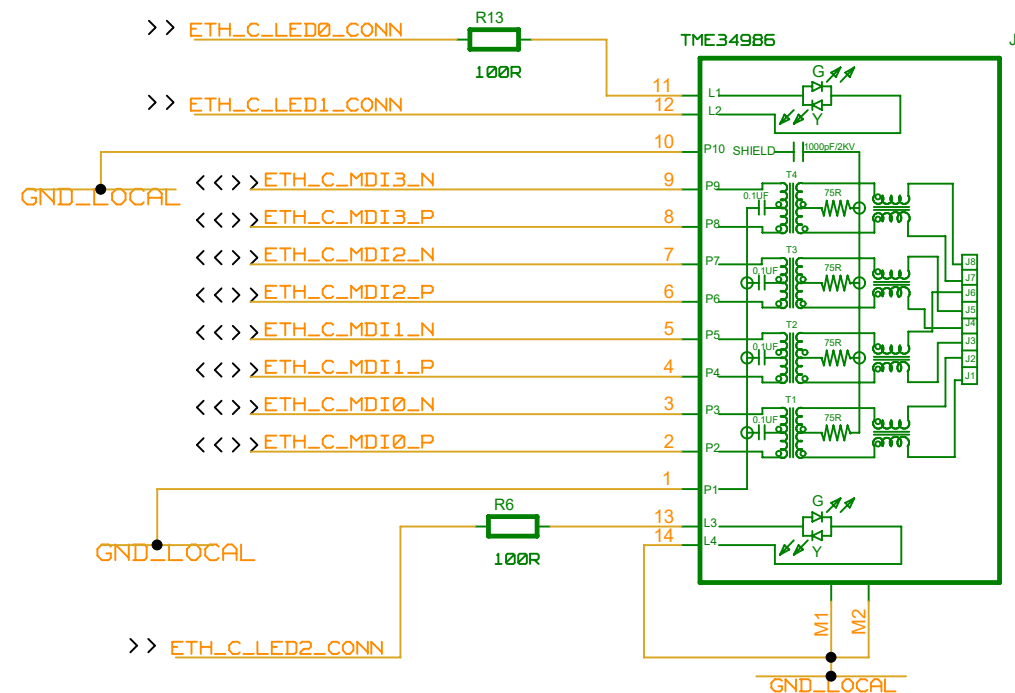
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STATE :

ETHERNET- C



ETHERNET- C CONNECTOR AND STRAPS



7.5.1.2 Strap for DP83869HM Functional Mode Selection

Table 7-12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMO DE[2]	OPMO DE[1]	OPMO DE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
				1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-TX to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

7.5.1.4 Straps for RGMII/SGMII to Copper

Table 7-14. Copper Ethernet Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	ANEG DIS	ANEGS EL_1	ANEGS EL_0	FUNCTION
LED_0	ANEG_DIS	47	0	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	0	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	1	NA
				1	0	0	NA
				1	0	1	NA
LED_2	ANEGSEL_1	45	0	1	1	0	Forced 100M, full duplex, MDI mode
				1	1	1	Forced 100M, full duplex, MDI-X mode
				0	0	0	Port Mirroring Disabled
				1	1	1	Port Mirroring Enabled

Table 7-11. PHY Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD1	PHY_ADD0
				MODE 0	0
				MODE 1	1
				MODE 2	0
				MODE 3	1

PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD3	PHY_ADD2
				MODE 0	0
				MODE 1	1
				MODE 2	0
				MODE 3	1

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A60-GENERIC SCHEMATIC

NUMBER :
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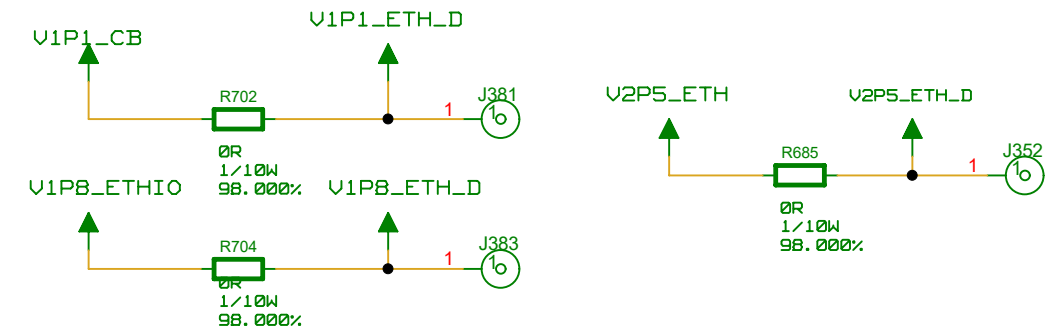
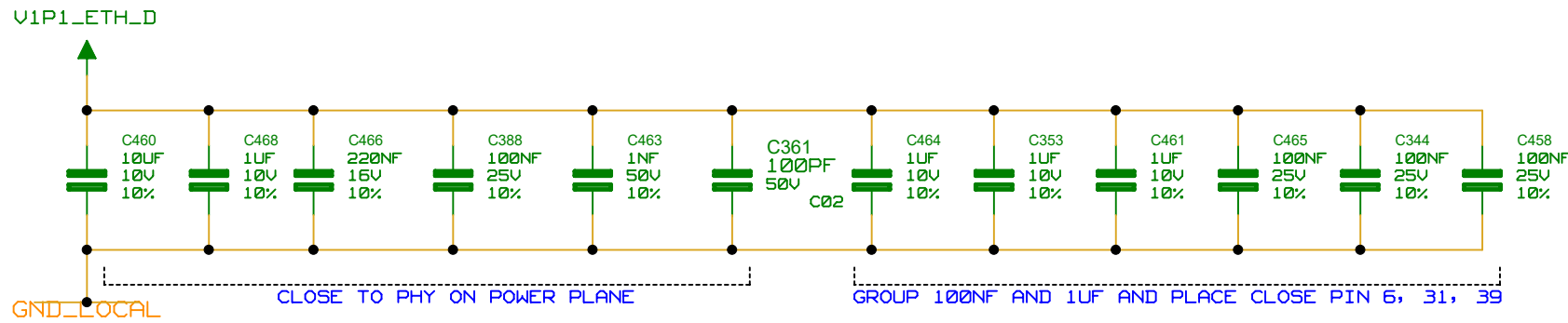
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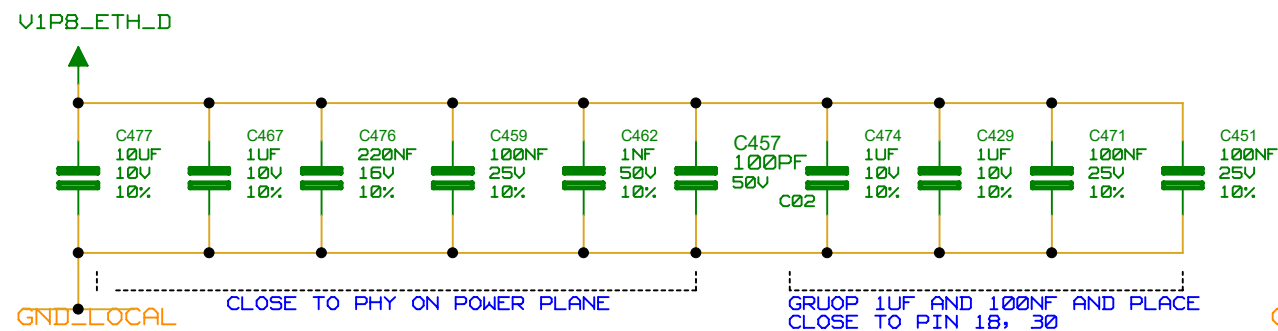
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ETHERNET- D DECAPS AND LED BUFFERS

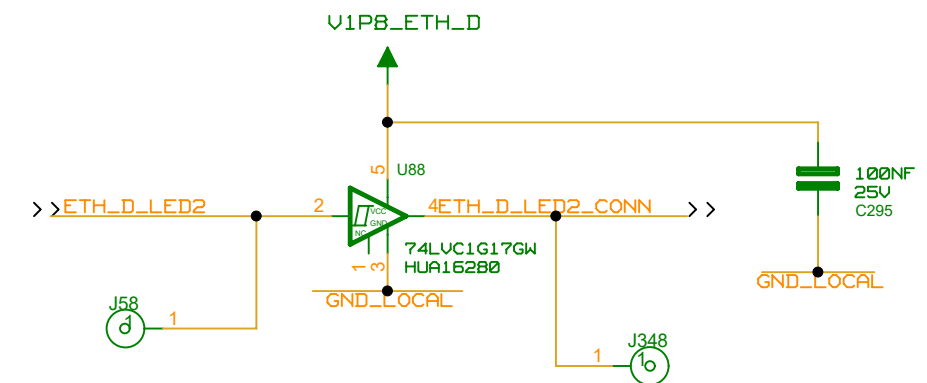
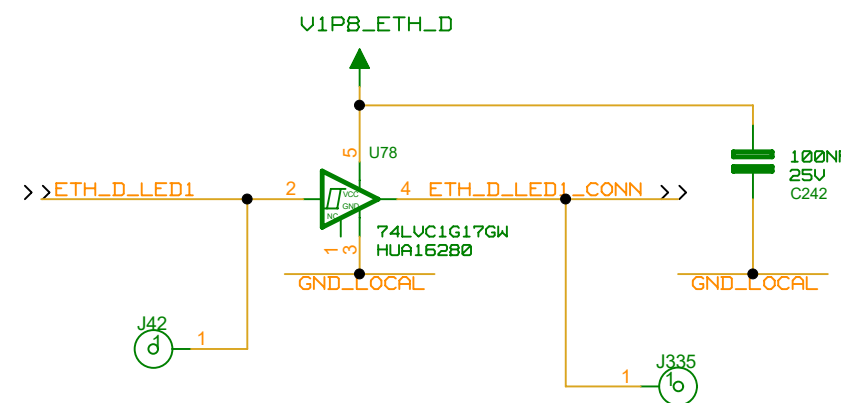
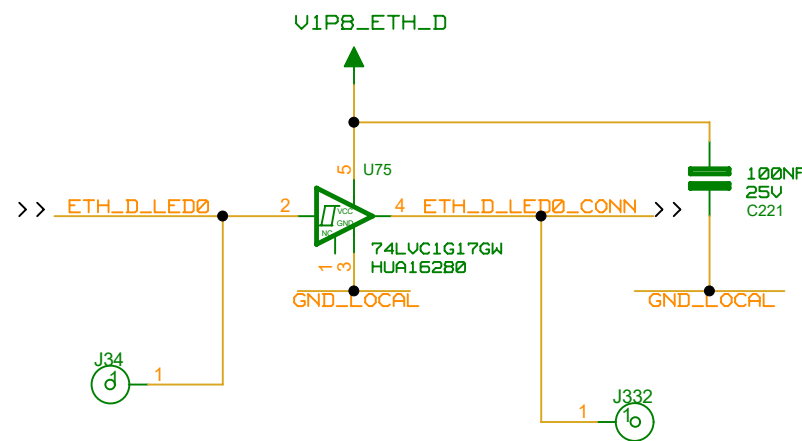
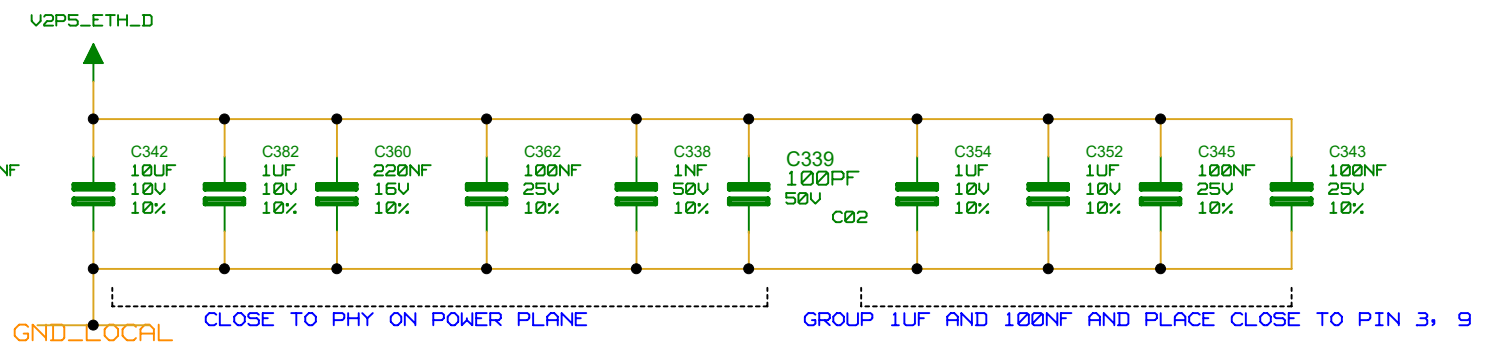
PHY 1.1V UDDA1P1 DECOUPLING CAPACITOR



PHY 1.8V UDDIO DECOUPLING CAPACITOR



PHY 2.5V UDDA2P5 DECOUPLING CAPACITOR



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PCB SOM AM64 SIZE M CARRIER BOARD
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A60-GENERIC SCHEMATIC

NUMBER :
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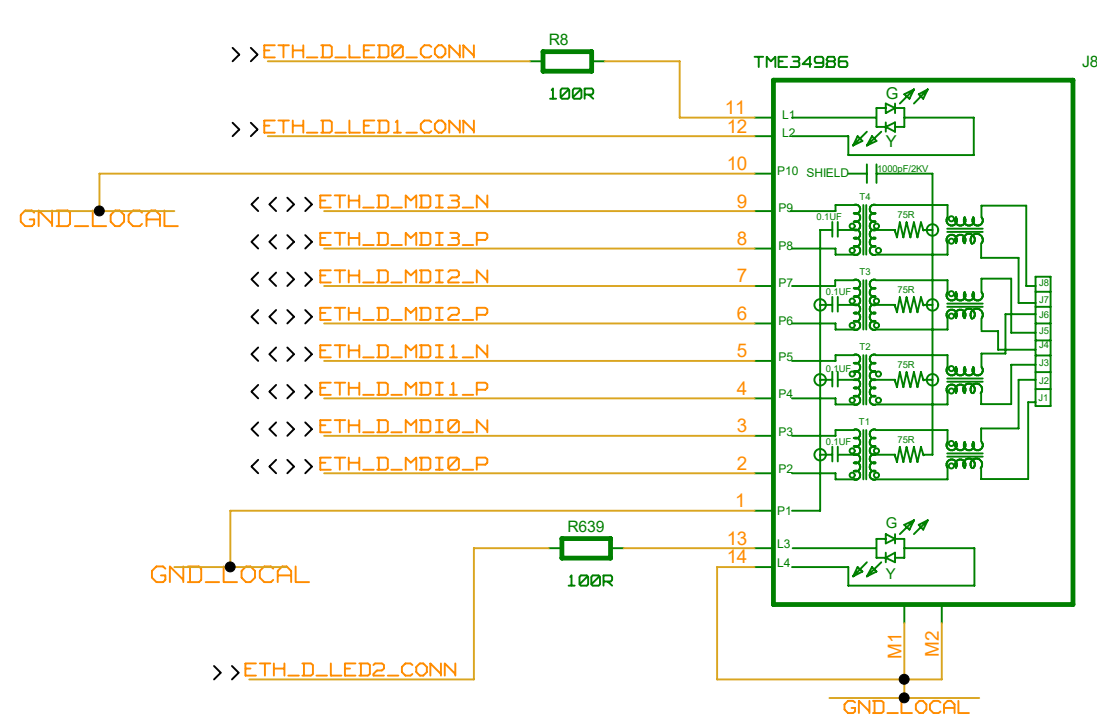
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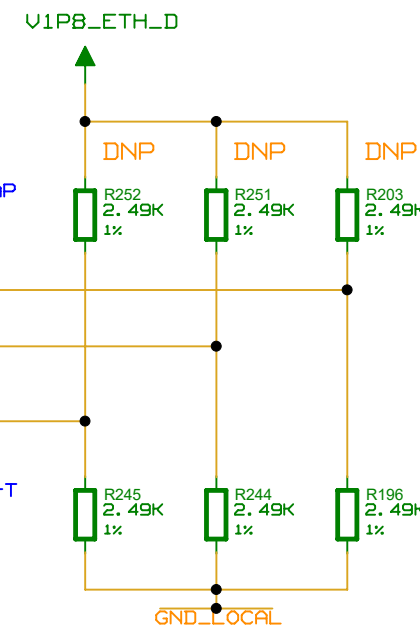
STATE :

ETHERNET-D CONNECTOR AND STRAPS



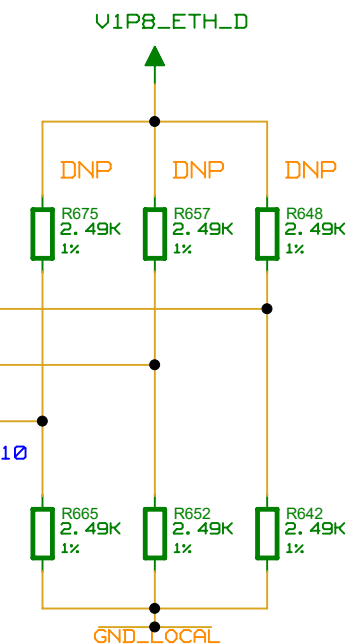
PHY OPERATING STRAP

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<< ETH_D_RD2
^ MINIMIZE STUB
<< ETH_D_RD3
^ MINIMIZE STUB
RGMII TO COPPER(1000 BASE-T
100BASE-TX/10BASE-TE)



PHY AUTO-NEGOTIATION STRAP

<< ETH_D_LED0
<< ETH_D_LED1
<< ETH_D_LED2
AUTO-NEGOTIATION 1000/100/10
AUTO-MDI-X



7.5.1.2 Strap for DP83869HM Functional Mode Selection

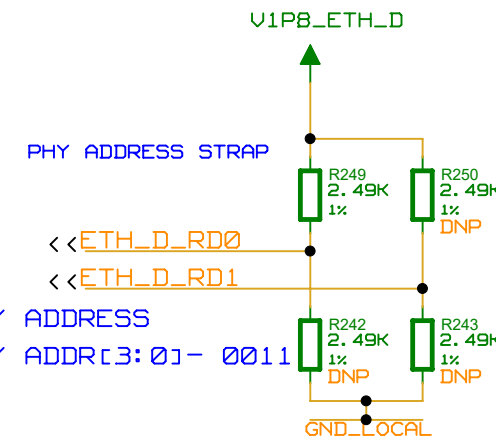
Table 7-12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMO DE[2]	OPMO DE[1]	OPMO DE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
RX_D2	OPMODE[2]	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-TX to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

7.5.1.4 Straps for RGMII/SGMII to Copper

Table 7-14. Copper Ethernet Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	ANEG DIS	ANEGS EL_1	ANEGS EL_0	FUNCTION
LED_0	ANEG_DIS	47	0	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	0	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	1	NA
				1	0	0	NA
LED_2	ANEGSEL_1	45	0	1	0	1	NA
				1	1	0	Forced 100M, full duplex, MDI mode
RX_CTRL	MIRROR_EN	38	0	1	1	1	Forced 100M, full duplex, MDI-X mode
				0	0	0	Port Mirroring Disabled
				1	1	1	Port Mirroring Enabled



PHY MIRRORING STRAP

<< ETH_D_RX_CTRL
^ MINIMIZE STUB
PULL-DOWN TO DISABLE
PORT MIRRORING

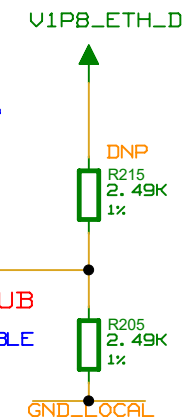


Table 7-11. PHY Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT			
RX_D0	PHY_ADD[1:0]	33	00	PHY_ADD1	PHY_ADD0	
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1

PIN NAME	STRAP NAME	PIN #	DEFAULT			
RX_D1	PHY_ADD[3:2]	34	00	PHY_ADD3	PHY_ADD2	
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1

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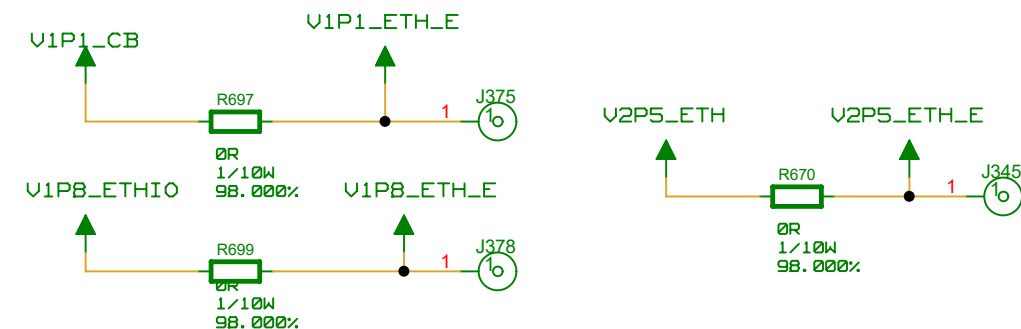
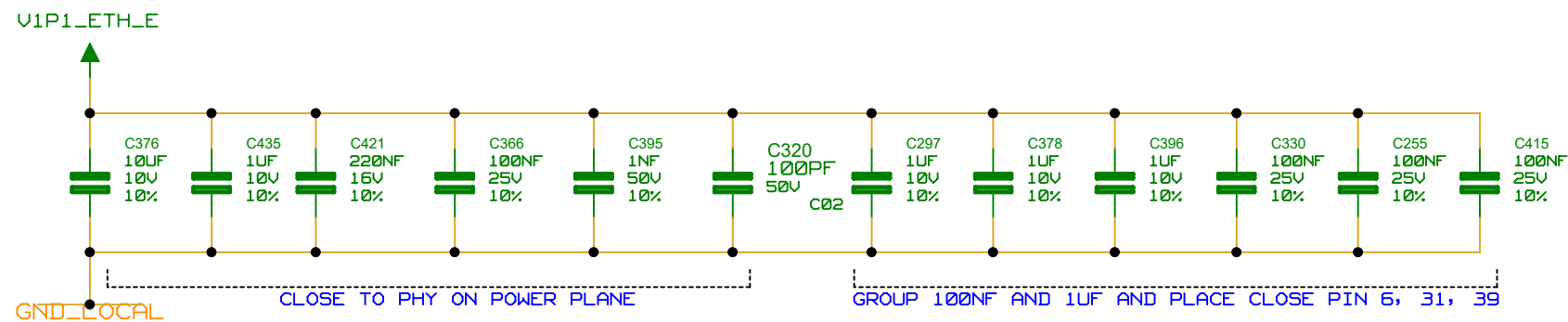
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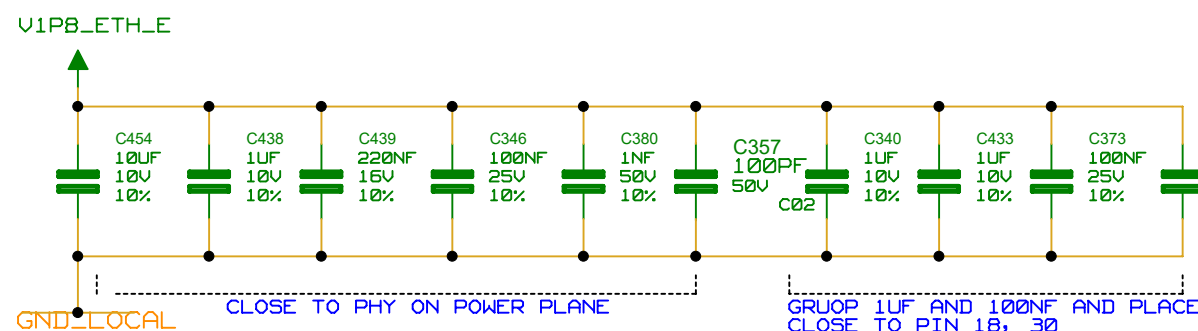
STATE :

ETHERNET- E DECAPS AND LED BUFFERS

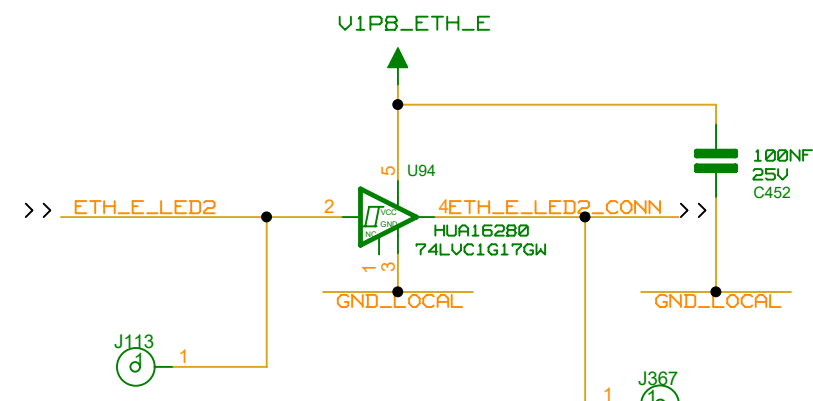
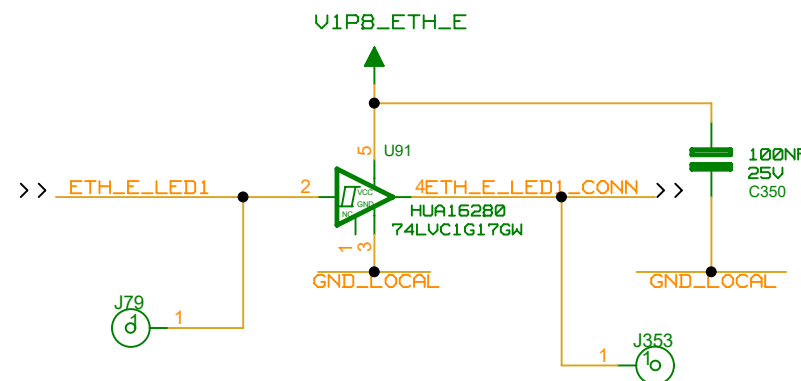
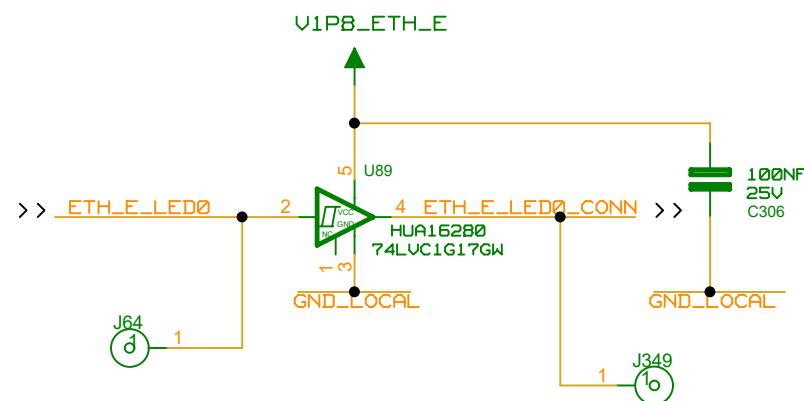
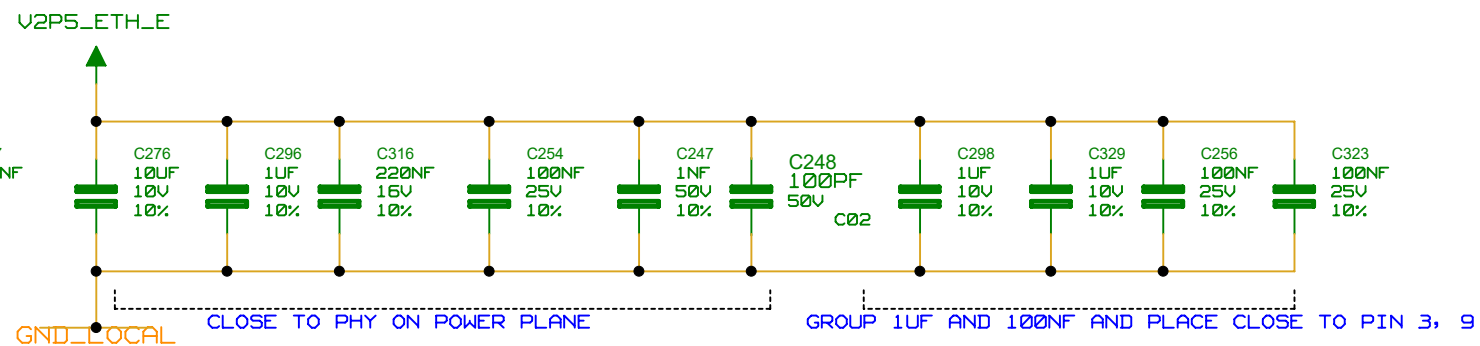
PHY 1.1V VDDA1P1 DECOUPLING CAPACITOR



PHY 1.8V VDDIO DECOUPLING CAPACITOR



PHY 2.5V VDDA2P5 DECOUPLING CAPACITOR



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AND MDIO BUS MUST BE CONFIGURED AT 1.8V

PLACE THE RESISTORS FROM R232 TO R229 CLOSER TO PHY IC

NOTE : PLACE R233 - R237 CLOSER TO OSM BALLS

NOTE: MDC MAX CLK RATE IS 25MHZ

NOTE: TX_CLK AND RX_CLK SIGNALS OPERATE IN 125MHZ IN 1000MBPS RGMII MODE.

NOTE: PLACE THE TESTPOINTS WITH 2.54MM PITCH

LED0 = 1 IF 1GB LINK DETECTED
0X5 LED5_CFG1 REGISTER

LED1 = 1 IF 10/100MB LINK DETECTED

NOTE: THIS INTERFACE IS SHARED AND PU PROVIDED AT OTHER PHY SIDE.

NOTE: 2.2K PULL UP FOR MDIO SIGNAL IS PROVIDED AS PER THE DATASHEET

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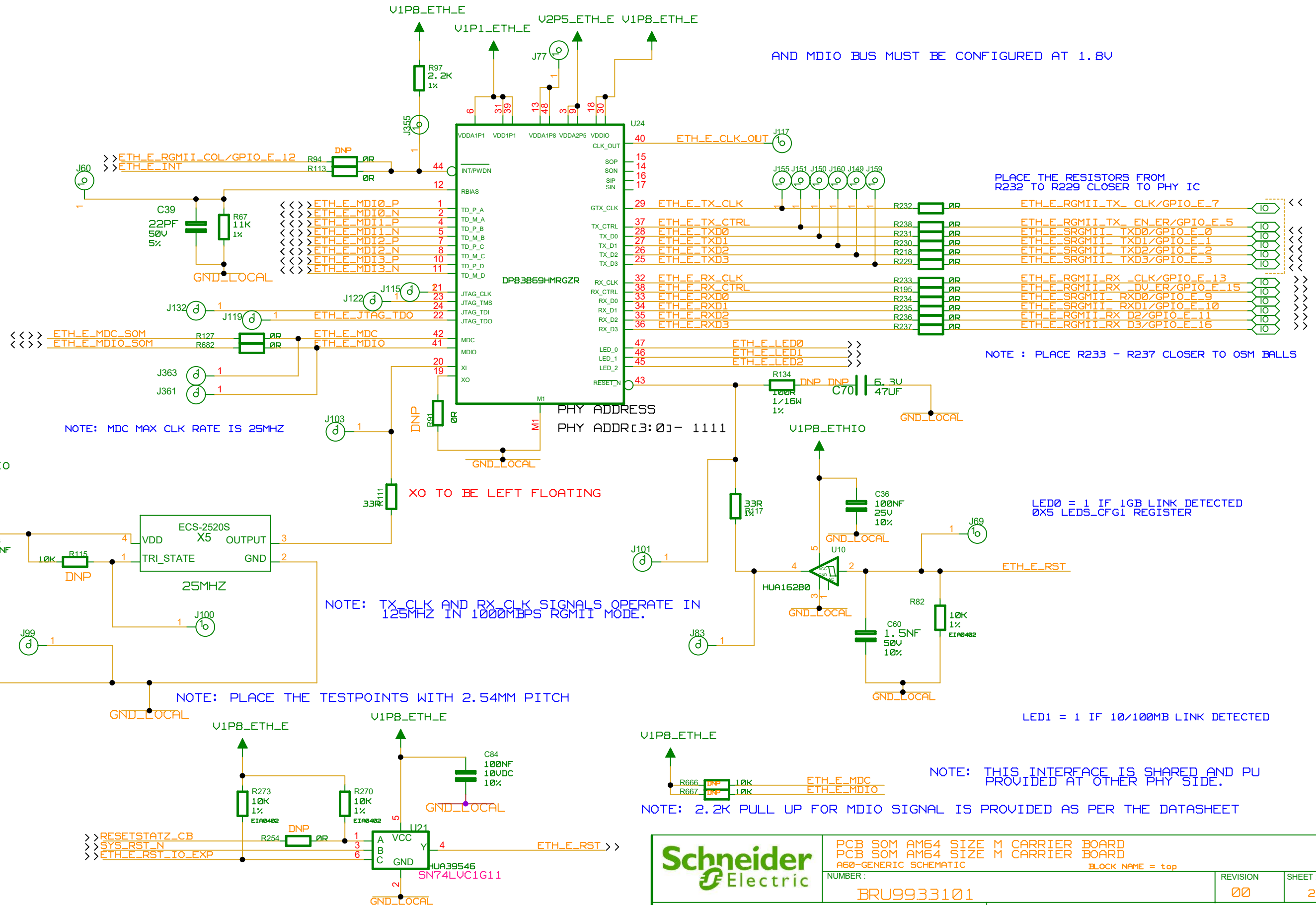
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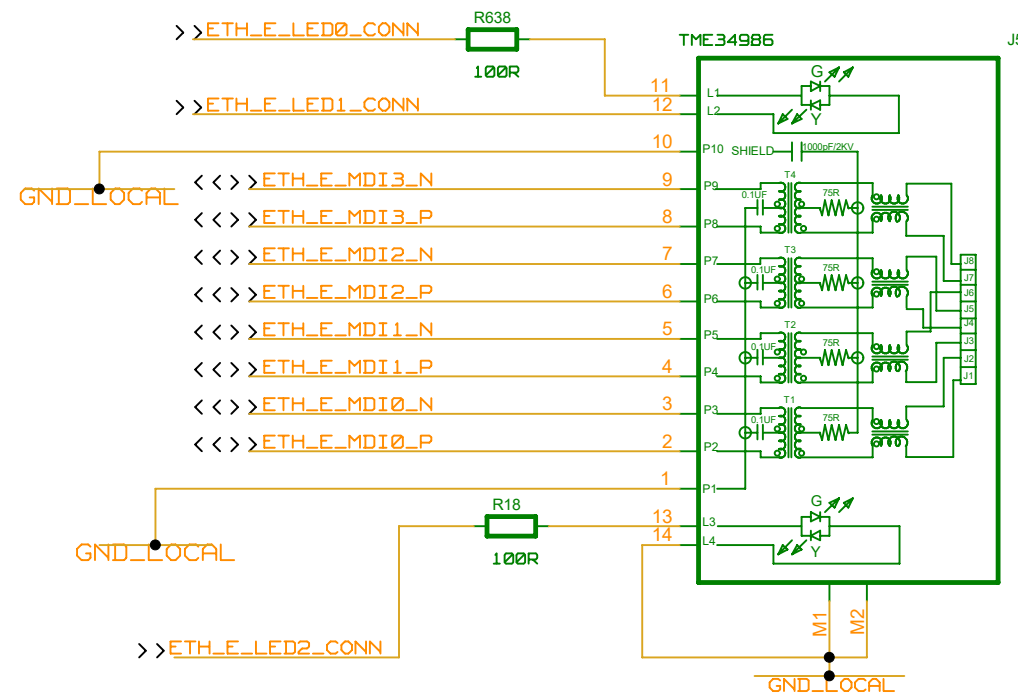
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ETHERNET- E CONNECTOR AND STRAPS



PHY OPERATING STRAP

<<ETH_E_JTAG_TDO

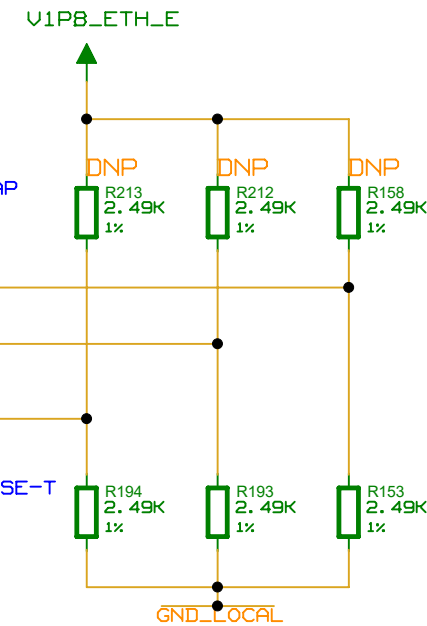
<<ETH_E_RXD2

^ MINIMIZE STUB

<<ETH_E_RXD3

^ MINIMIZE STUB

RGMII TO COPPER(1000 BASE-T
100BASE-TX/10BASE-T)



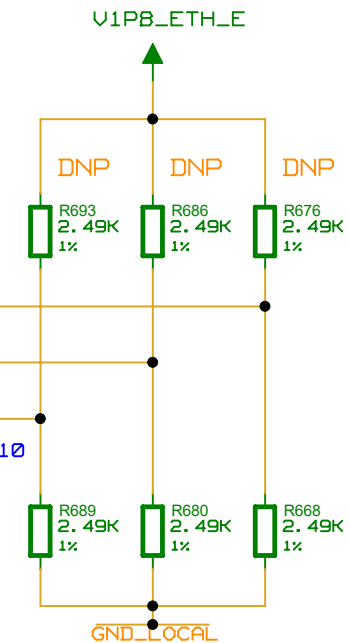
PHY AUTO-NEGOTIATION STRAP

<<ETH_E_LED0

<<ETH_E_LED1

<<ETH_E_LED2

AUTO-NEGOTIATION 1000/100/10
AUTO-MDI-X



7.5.1.2 Strap for DP83869HM Functional Mode Selection

Table 7-12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMO DE[2]	OPMO DE[1]	OPMO DE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
RX_D2	OPMODE[2]	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-TX to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

7.5.1.4 Straps for RGMII/SGMII to Copper

Table 7-14. Copper Ethernet Strap Table

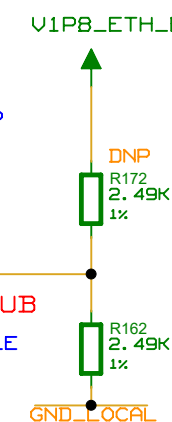
PIN NAME	STRAP NAME	PIN #	DEFAULT	ANEG_DIS	ANEGS EL_1	ANEGS EL_0	FUNCTION
LED_0	ANEG_DIS	47	0	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	0	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	1	NA
				1	0	0	NA
LED_2	ANEGSEL_1	45	0	1	0	1	NA
				1	1	0	Forced 100M, full duplex, MDI mode
				1	1	1	Forced 100M, full duplex, MDI-X mode
RX_CTRL	MIRROR_EN	38	0	0	0	0	Port Mirroring Disabled
				1	1	1	Port Mirroring Enabled

PHY MIRRORING STRAP

<<ETH_E_RX_CTRL

^ MINIMIZE STUB

PULL-DOWN TO DISABLE
PORT MIRRORING

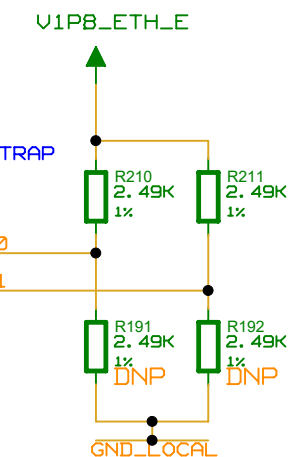


PHY ADDRESS STRAP

<<ETH_E_RXD0

<<ETH_E_RXD1

PHY ADDRESS
PHY ADDR[3:0] = 1111



7.5.1.2 Strap for DP83869HM Functional Mode Selection

Table 7-12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMO DE[2]	OPMO DE[1]	OPMO DE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
RX_D2	OPMODE[2]	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-TX to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

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