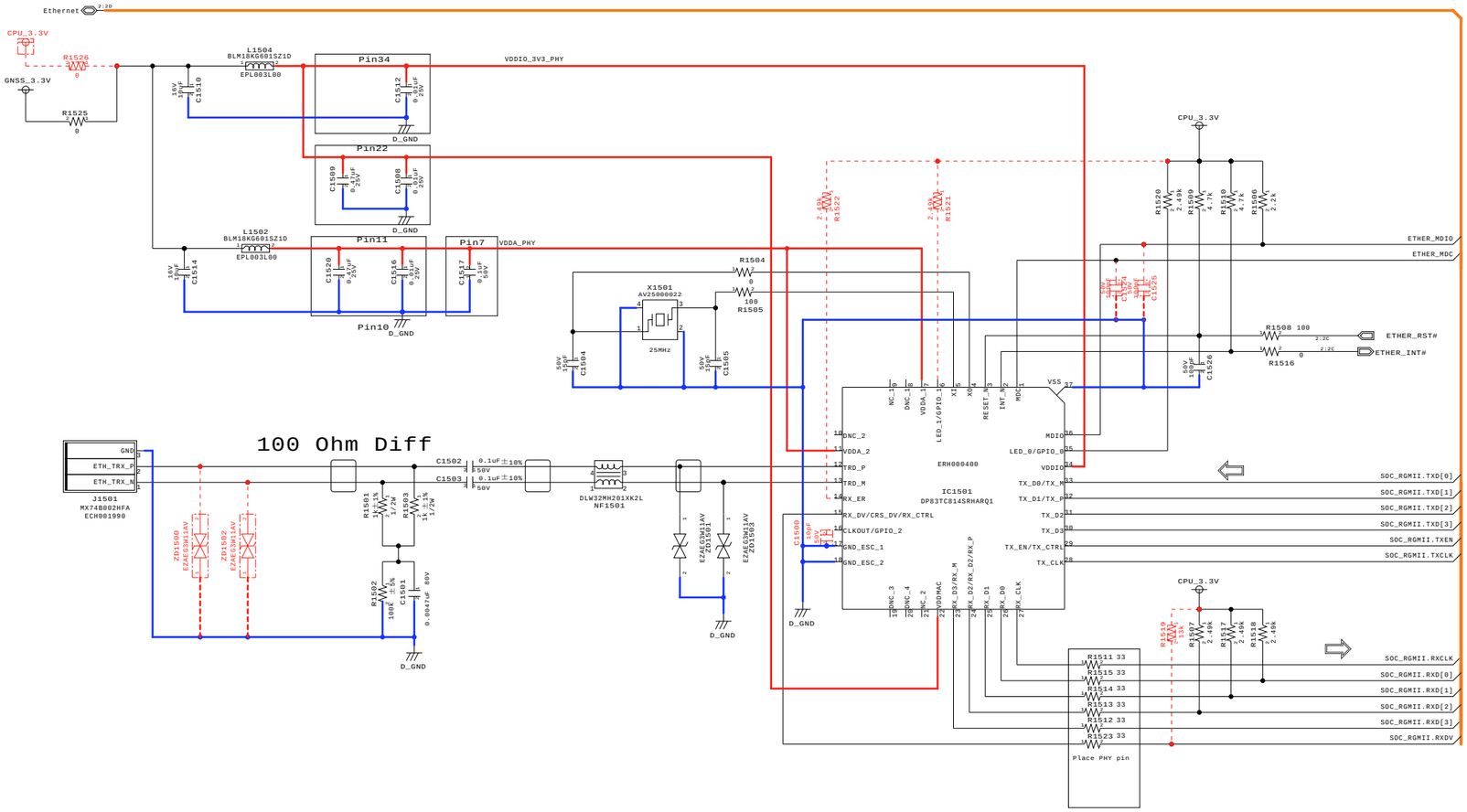


```
PHY Addr = 0x0
PHY Address:
ADD[3210]  RX_DV RX_ER
============================
0000(0X0)  OPEN   OPEN
1000(0X8)  OPEN   13K
1010(0XA)  OPEN   4.5K
0100(0X4)  13K    OPEN
1100(0XC)  13K    13K
1110(0XE)  13K    4.5K
0101(0X5)  4.5K   OPEN
1101(0XD)  4.5K   13K
1111(0XF)  4.5k   4.5k

Master/Slave: MASTER
LED0
========================
0 OPEN  SLAVE
1 2.49K MASTER

MAC INTERFACE MODE: RGMII(RX DELAY)
    RX_D2 RX_D1 RXD0
============================
000 OPEN  OPEN  OPEN  SGMII
001 OPEN  OPEN  2.49K MII
010 OPEN  2.49K OPEN  RMII SLAVE
011 OPEN  2.49K 2.49K RMII MASTER
100 2.49K OPEN  OPEN  RGMII(ALIGN)
101 2.49K OPEN  2.49K RGMII(TX DELAY)
110 2.49K 2.49K OPEN  RGMII(TX/RX DELAY)
111 2.49K 2.49K 2.49K RGMII(RX DELAY)

AUTO: Autonomous
    LED1
============================
0   OPEN   AUTONOMOUS
1   2.49K  MANAGED MODE
```

SYM	DATE	REVISION	DWG	CAL WT(g)	MATERIAL
			DSGN		
			CHK	ACT WT(g)	FINISH
MODEL		DATE	APPR	SCALE FREE	UNIT mm TOL

NAME: CIRCUIT DIAGRAM
DWG NO.
faurecia clarion ELECTRONICS