



# **SERDES Demonstration Kit User Manual**

**NSID: SERDES05-40USB**  
(DS99R105/106)

Rev 0.1

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## Introduction:

National Semiconductor's SERDES evaluation kit contains one (1) DS99R105 Serializer (Tx) board, one (1) DS99R106 De-serializer (Rx) board, and one (1) two (2) meter high speed USB 2.0 cable.

*Note: the demo boards are not for EMI testing. The demo boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, and multiple connector options.*

The DS99R105/106 chipset supports a variety of display applications. The single FPD-LINKII (FPD-LinkII) interface is well-suited for any display system interface. Typical applications include: navigation displays, automated teller machines (ATMs), POS, video cameras, global positioning systems (GPS), portable equipment/instruments, factory automation, etc.

The DS99R105 and DS99R106 can be used as a 24-bit general purpose FPD-LinkII Serializer and De-serializer chipset designed to transmit data at clocks speeds ranging from 3 to 40 MHz.

The Serializer board accepts LVCMOS input signals. The FPD-LinkII Serializer converts the LVCMOS parallel lines into a single serialized FPD-LINKII data pair with an embedded FPD-LINKII clock. The serial data stream toggles at 28 times the base clock rate. With an input clock at 40 MHz, the transmission rate for FPD-LinkII line is 960Mbps.

The De-serializer board accepts the FPD-LinkII serialized data stream with embedded clock and converts the data back into parallel LVCMOS signals and clock. Note that NO reference clock is needed to prevent harmonic lock as with other devices currently on the market.

Suggested equipment to evaluate the chipset, an LVCMOS signal source such as a video generator or word generator or pulse generator and oscilloscope with a bandwidth of at least 40 MHz will be needed.

The user needs to provide the proper LVCMOS/RGB inputs and LVCMOS/clock to the Serializer and also provide a proper interface from the De-serializer output to an LCD panel or test equipment. The Serializer and De-serializer boards can also be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used on the input to the DS99R105 and to the output of the DS99R106.

Example of suggested display setup:

- 1) video generator with LVCMOS output
- 2) 6-bit LCD panel with a LVCMOS input interface.

## Contents of the Evaluation Kit:

- 1) One Serializer board with the DS99R105
- 2) One De-serializer board with the DS99R106
- 3) One 2-meter high speed USB 2.0 cable (4-pin USB A to 5-pin mini USB)
- 4) Evaluation Kit Documentation (this manual)
- 5) DS99R105/106 Datasheet

## SERDES Typical Application:

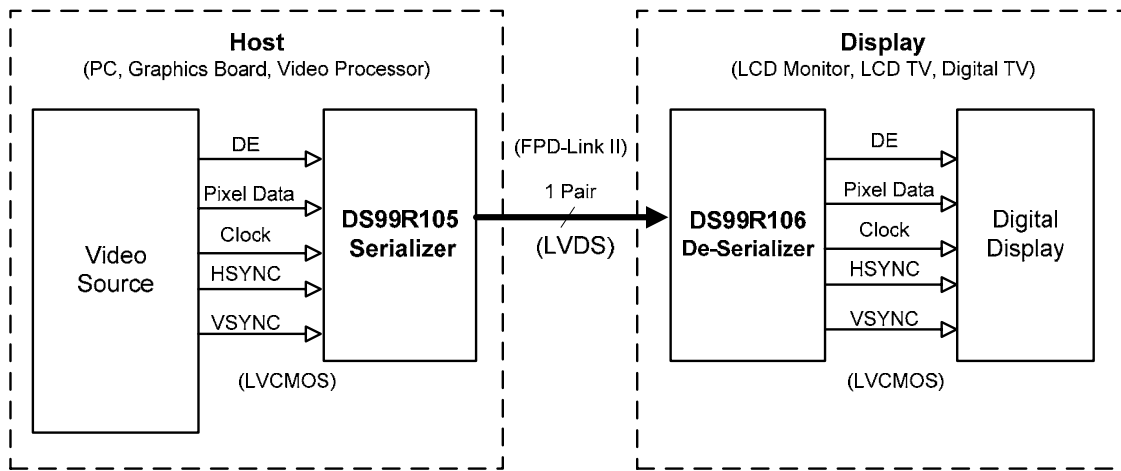


Figure 1a. Typical SERDES Application (18-bit RGB Color)

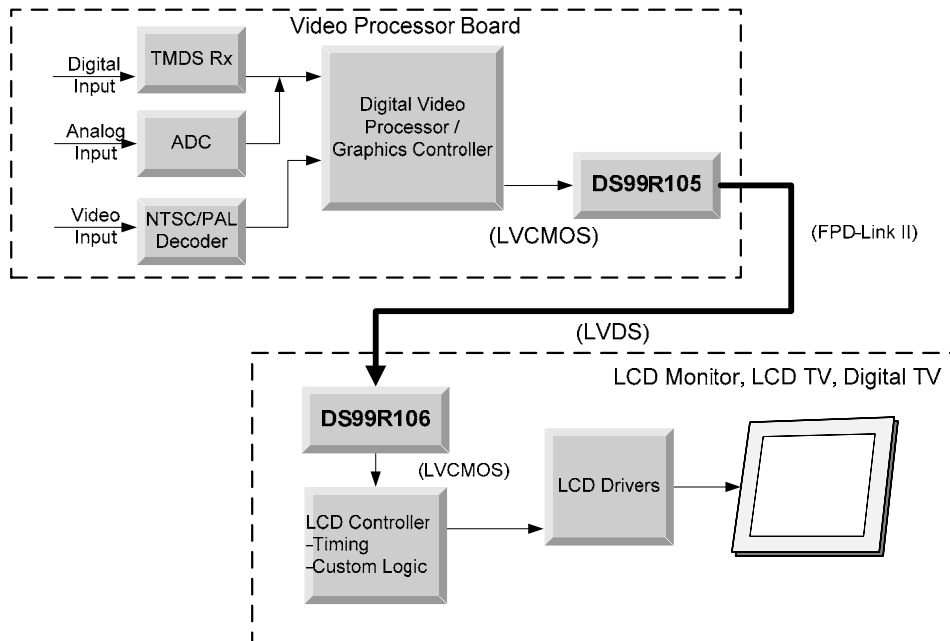


Figure 1b. Typical SERDES System Diagram

Figures 1a and 1b illustrate the use of the Chipset (Tx/Rx) in a Host to Flat Panel Interface.

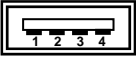
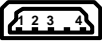
The chipsets support up to 18-bit color depth TFT LCD Panels.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

## How to set up the Evaluation Kit:

The PCB routing for the Tx input pins (DIN) have been laid out to accept incoming LVCMOS signals from 50-pin IDC connector. The TxOUT/RxIN (DOOUT/RIN) interface uses a single twisted pair cable (provided). The PCB routing for the Rx output pins (ROUT) are accessed through a 50-pin IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

- 1) A two (2) meter high speed USB 2.0 cable has been included in the kit. A two (2) meter USB connector/cable assembly has been included in the kit. Connect 4-pin

USB A  **A** side of cable harness to the serializer board and the other side 5-pin mini USB jack  <sup>MIN</sup> to the de-serializer board. This completes the FPD-LINKII interface connection.

**NOTE: The DS99R105 and DS99R106 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.**

- 2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings for more details.
- 3) From the Video Decoder board, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the De-serializer board to the panel. *Note: For non 50 ohm signal sources, provide 3.3V LVCMOS input signal levels into DIN[23:0] and TCLK or remove the 49.9 ohm parallel termination resistors R1-R25 on the DS99R105 Serializer board.*
- 4) Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

## Power Connection:

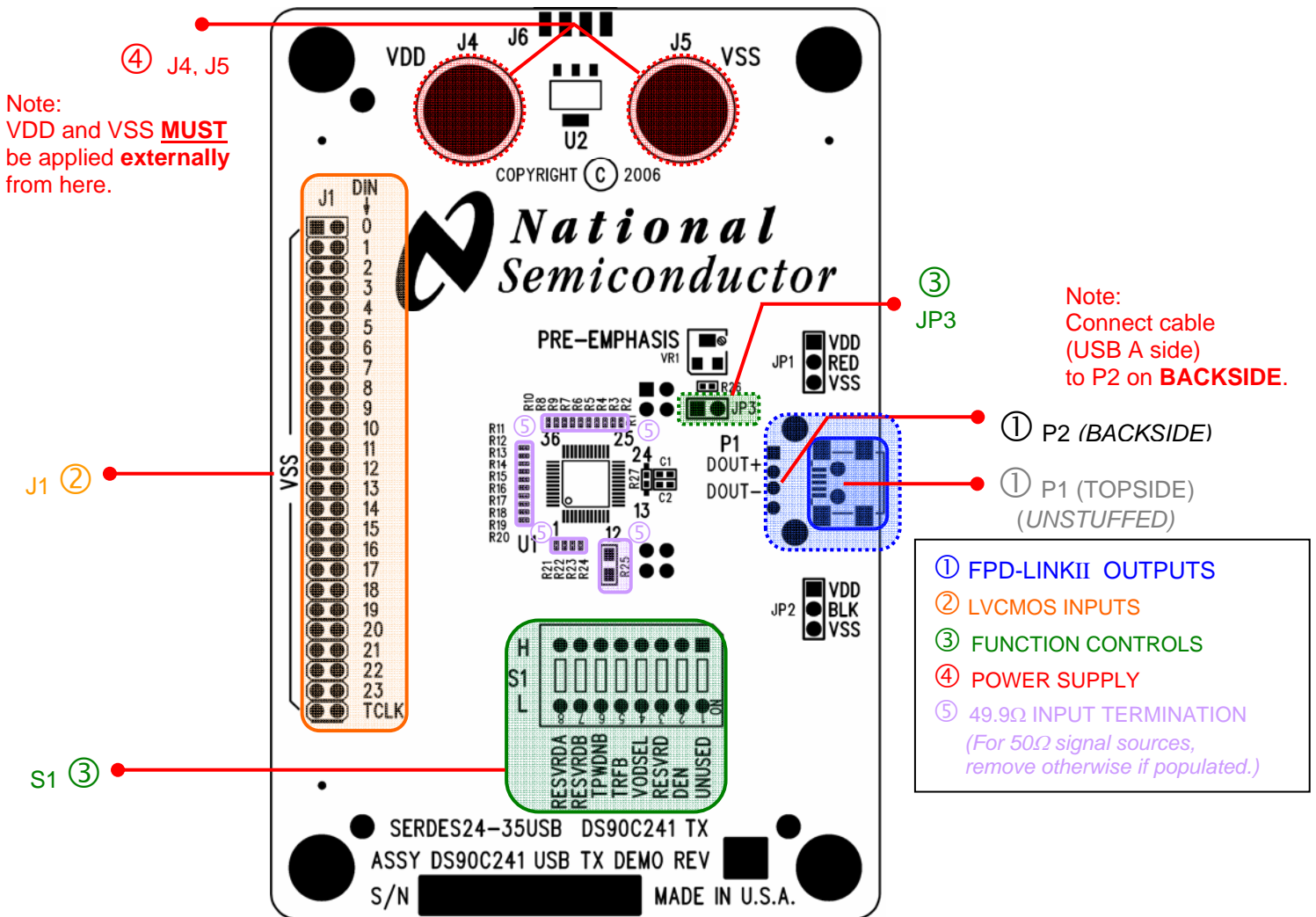
The Serializer and De-serializer boards must be powered by supplying power externally through J4 (VDD) and J5 (VSS) on Serializer Board and J4 (VDD) and J5 (VSS) on De-serializer board. Note +4V is the MAXIMUM voltage that should ever be applied to the SERDES Serializer (DS99R105) or De-serializer (DS99R106) VDD terminal. Damage to the device(s) can result if the voltage maximum is exceeded.

## SERDES Serializer Board Description:

The 50-pin IDC connector J1 accepts 24 bits of LVCMOS RGB data along with the clock input.

The SERDES Serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the Serializer to be operational, the Power Down (S1-TPWDB) and Data Enable (S1-DEN) switches on S1 must be set HIGH. The board is factory configured (with series capacitors on the FPD-LINKII outputs) in AC coupled mode: S1-RESVRDA, RESVRDB, and VODSEL must be set LOW. Rising or falling edge reference clock is also selected on S1-TRFB: HIGH (rising) or LOW (falling).

The USB connector P2 (USB-A side) on the bottom side of the board provides the interface connection to the FPD-LINKII signals to the De-serializer board. Note: P1 (mini USB) on the top side is un-stuffed and not to be used with the cable provided in the kit.






## Configuration Settings for the Tx Board

### S1: Serializer Input Features Selection







Reference	Description	Input = L	Input = H	S1
RESVRDA	<b>DCAOFF</b>	MUST be tied low for normal operation <b>(Default)</b>	-	
RESVRDB	<b>DCBOFF</b>	MUST be tied low for normal operation <b>(Default)</b>	-	
TPWDNB	<b>PoWerDown Bar</b>	Powers Down	Operational <b>(Default)</b>	
TRFB	Latch input data on Rising or Falling edge of TCLK	Falling Edge <b>(Default)</b>	Rising Edge	
VODSEL	FPD-LINKII output <b>VOD SELECT</b>	≈350mV <b>(Default)</b>	≈700mV	
RESVRD	<b>REServeD</b>	MUST be tied low for normal operation <b>(Default)</b>		
DEN	Output Data <b>ENabled</b>	Disabled	Enabled <b>(Default)</b>	
UNUSED	UNUSED	Don't care	Don't care	

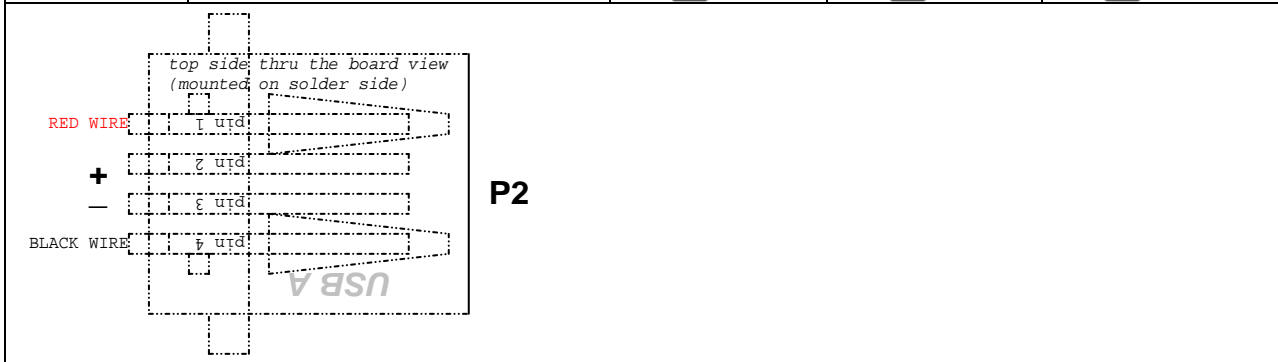


JP3: Pre-Emphasis Feature Selection

Reference	Description	OPEN (tied H)	CLOSED (tied L)	
JP3	Pre-Emphasis* – helps to increase the eye pattern opening in the FPD-LINKII stream	Disabled – no jumper <b>(Default)</b> 	Enabled – With jumper 	
*Note: Pre-emphasis is only needed for lossy cables and/or long cable runs				

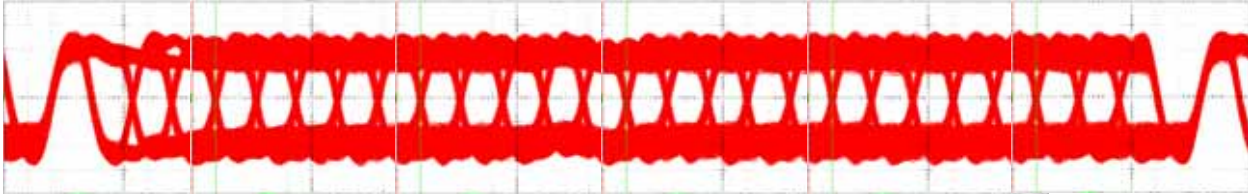
JP1, JP2: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP1	Power wire in USB cable thru P2 (and P1 not mounted) connector Jumper RED to VSS – recommended  <i>Note: Normally VDD in USB application</i>	Red wire tied to VDD  	Red wire tied to VSS <b>(Default)</b>  	Red wire floating (not recommended)  
JP2	Power wire in USB cable thru P2 (and P1 not mounted) connector Jumper BLACK to VSS – recommended  <i>Note: Normally VSS in USB application</i>	Black wire tied to VDD  	Black wire tied to VSS <b>(Default)</b>  	Black wire floating (not recommended)  



The following picture depicts a typical example of the FPD-Link II serial stream. This snapshot was taken with a differential probe across the 100 ohm termination resistor R1 on the DS99R106 Rx evaluation board. R1 is the termination resistor to the RxIN +/-.

Note: The scope was triggered, with a separate probe, on TCLK, the input clock into the DS99R105 Tx. To view the serial stream correctly, do not trigger on the probe monitoring the serial stream.



## Tx LVCMOS and FPD-LINKII Pinout by IDC Connector

The following three tables illustrate how the Tx inputs are mapped to the IDC connector J1, the FPD-LINKII outputs on the USB-A connector P2, and the mini USB P1 (not installed) pinouts. Note – labels are also printed on the demo boards for both the lvcmos input and FPD-LINKII outputs.

<b>J1</b>			
<b>LVCMOS INPUT</b>			
pin no.	name	name	pin no.
<b>1</b>	GND	DIN0	2
3	GND	DIN1	4
5	GND	DIN2	6
7	GND	DIN3	8
9	GND	DIN4	10
11	GND	DIN5	12
13	GND	DIN6	14
15	GND	DIN7	16
17	GND	DIN8	18
19	GND	DIN9	20
21	GND	DIN10	22
23	GND	DIN11	24
25	GND	DIN12	26
27	GND	DIN13	28
29	GND	DIN14	30
31	GND	DIN15	32
33	GND	DIN16	34
35	GND	DIN17	36
37	GND	DIN18	38
39	GND	DIN19	40
41	GND	DIN20	42
43	GND	DIN21	44
45	GND	DIN22	46
47	GND	DIN23	48
49	GND	TCLK	50

<b>P2</b>	
<b>(bottom side)</b>	
<b>FPD-LINKII OUTPUT</b>	
pin no.	name
<b>1</b>	JP1
2	DOUT+
3	DOUT-
4	JP2

<b>P1</b>	
<b>(topside)</b>	
<b>(not mounted)</b>	
<b>FPD-LINKII OUTPUT</b>	
pin no.	name
5	JP2
4	NC
3	DOUT-
2	DOUT+
<b>1</b>	JP1

**BOM (Bill of Materials) Serializer PCB:**

DS99R105 Tx USB Demo Board - Board Stackup Revised: Thursday, March 23, 2006

DS99R105 Tx USB Demo Board Revision: 1

Bill Of Materials March 23,2006 18:52:42

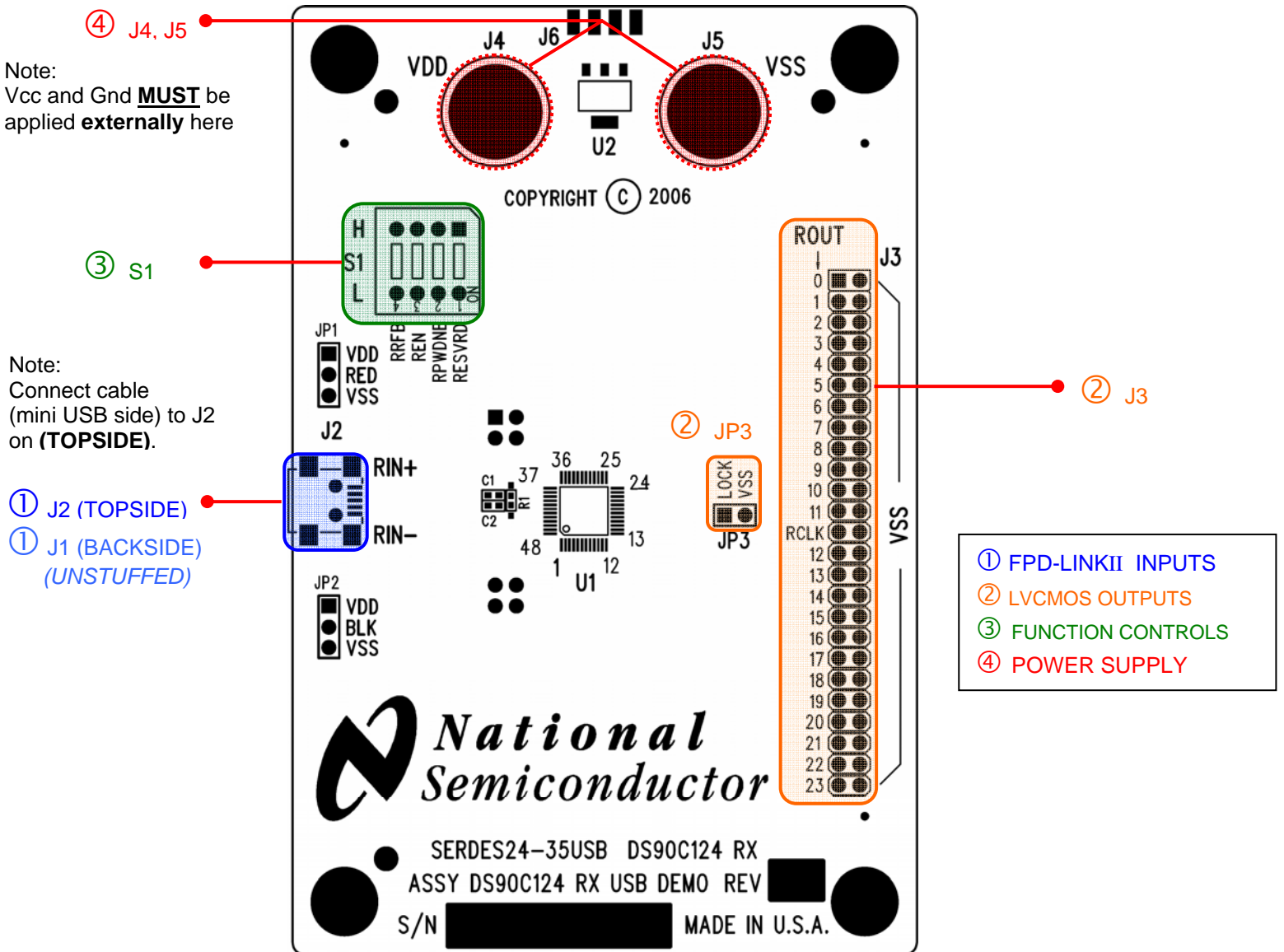
Item	Qty	Reference	Part	PCB Footprint
1	2	C1,C2	0.1uF	CAP/HDC-0402
2	1	C3	2.2uF	3528-21_EIA
3	1	C4	22uF	CAP/N
4	1	C5	0.1uF	CAP/HDC-1206
5	5	C6,C9,C10,C13,C20	22uF	CAP/EIA-B 3528-21
6	5	C7,C11,C15,C16,C19	0.01uF	CAP/HDC-0603
7	5	C8,C12,C14,C17,C18	0.1uF	CAP/HDC-0603
8	2	JP2,JP1	3-Pin Header	Header/3P
9	1	JP3	2-Pin Header	Header/2P
10	1	J1	IDC2X25_Unshrouded	IDC-50
11	2	J5,J4	BANANA	CON/BANANA-S
12	1	P1	mini USB 5pin_open	mini_USB_surface_mount
13	1	P2	USB A	USB_TYPE_A_4P
14	24	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24	49.9ohm_open	RES/HDC-0201
15	1	R25	49.9ohm_open	RES/HDC-0805
16	1	R26	5.76K (3.01K)	RES/HDC-0402
17	1	R27	100 ohm,0402	RES/HDC-0402
18	5	R28,R30,R32,R33,R35	0 Ohm,0402	RES/HDC-0402
19	8	R38,R39,R40,R41,R42,R43, R44,R45	10K	RES/HDC-0805
20	1	S1	SW DIP-8	DIP-16
21	1	U1	DS99R105	48 Id TQFP Surface Mount 4mm
22	1	VR1	SVR20K	Square

## Rx SERDES De-serializer Board:

The USB connector J2 (mini USB) on the topside of the board provides the interface connection for FPD-LINKII signals to the Serializer board. Note: J1 (mini USB) on the bottom side is un-stuffed and not used with the cable provided in the kit.

The SERDES De-serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the De-serializer to be operational, the Power Down (RPWDNB) and Receiver Enable (REN) switches on S1 must be set HIGH. Rising or falling edge reference clock is also selected by S1: HIGH (rising) or LOW (falling).

The 50 pin IDC Connector J3 provides access to the 24 bit LVCMOS and clock outputs.



## Configuration Settings for the Rx Board







### S1: De-serializer Input Features Selection

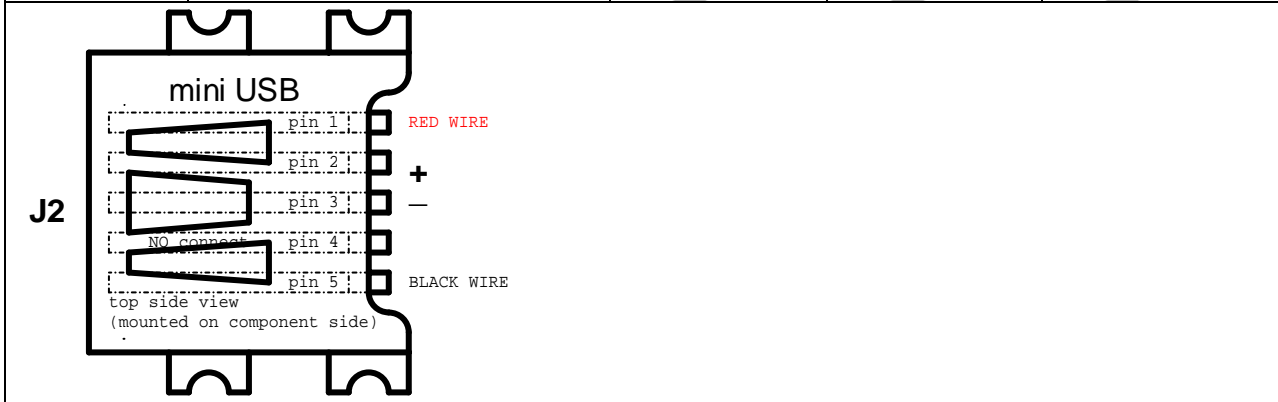
Reference	Description	Input = L	Input = H	S1
RFB	Latch output data on <b>R</b> ising or <b>F</b> alling Data Strobe of RCLK	Falling (Default)	Rising	<p>H S1 L</p> <p>RFB REN RPWDNB RESVRD</p>
REN	Receiver Output <b>EN</b> abled	Disabled	Enabled (Default)	
RPWDNB	<b>PoWerDownN Bar</b>	Power Down (Disabled)	Operational (Default)	
RESVRD	<b>RESeRVeD</b>	Don't care	Don't care	

### JP3: Output Lock Monitor

Reference	Description	Output = L	Output = H	JP3
LOCK	Receiver PLL <b>LOCK</b> <b>Note:</b> <b>DO NOT PUT A SHORTING JUMPER IN JP3.</b>	locked	unlocked	<p>LOCK VSS</p> <p>JP3</p>

JP1, JP2: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
<b>JP1</b>	Power wire in USB cable thru J2 ( <i>and J1 not mounted</i> ) connector Jumper RED to VSS – recommended  <i>Note: Normally VDD in USB application</i>	Red wire tied to VDD  JP1 	Red wire tied to VSS <b>(Default)</b>  JP1 	Red wire floating (not recommended)  JP1 
<b>JP2</b>	Power wire in USB cable thru J2 ( <i>and J1 not mounted</i> ) connector Jumper BLACK to VSS – recommended  <i>Note: Normally VSS in USB application</i>	Black wire tied to VDD  JP2 	Black wire tied to VSS <b>(Default)</b>  JP2 	Black wire floating (not recommended)  JP2 



## Rx FPD-LINKII Pinout and LVCMOS by IDC Connector

The following three tables illustrate how the Rx outputs are mapped to the IDC connector J3, the mini USB FPD-LINKII connector J2, and the mini USB FPD-LINKII connector J1 (not installed) pinouts. Note – labels are also printed on the demo boards for both the FPD-LINKII inputs and LVCMOS outputs.

<b>J3</b>			
<b>LVCMOS INPUT</b>			
<b>pin no.</b>	<b>name</b>	<b>name</b>	<b>pin no.</b>
<b>1</b>	<b>ROUT0</b>	GND	2
3	ROUT1	GND	4
5	ROUT2	GND	6
7	ROUT3	GND	8
9	ROUT4	GND	10
11	ROUT5	GND	12
13	ROUT6	GND	14
15	ROUT7	GND	16
17	ROUT8	GND	18
19	ROUT9	GND	20
21	ROUT10	GND	22
23	ROUT11	GND	24
25	RCLK	GND	26
27	ROUT12	GND	28
29	ROUT13	GND	30
31	ROUT14	GND	32
33	ROUT15	GND	34
35	ROUT16	GND	36
37	ROUT17	GND	38
39	ROUT18	GND	40
41	ROUT19	GND	42
43	ROUT20	GND	44
45	ROUT21	GND	46
47	ROUT22	GND	48
49	ROUT23	GND	50

<b>J2</b>	
<b>(topside)</b>	
<b>FPD-LINKII</b>	
<b>OUTPUT</b>	
<b>pin no.</b>	<b>name</b>
<b>1</b>	JP1
2	<b>DOUT+</b>
3	<b>DOUT-</b>
4	NC
5	JP2

<b>J1</b>	
<b>(bottom side)</b>	
<b>(not mounted)</b>	
<b>FPD-LINKII</b>	
<b>OUTPUT</b>	
<b>pin no.</b>	<b>name</b>
5	JP2
4	NC
3	<b>DOUT-</b>
2	<b>DOUT+</b>
<b>1</b>	JP1



**BOM (Bill of Materials) De-serializer PCB:**

DS99R106 Rx USB Demo Board - Board Stackup Revised: Thursday, March 23, 2006

DS99R106 Rx USB Demo Board Revision: 1

Bill Of Materials March 23,2006 19:19:22

Item	Qty	Reference	Part	PCB Footprint
1	2	C2,C1	0.1uF	CAP/HDC-0402
2	1	C3	2.2uF	3528-21_EIA
3	1	C4	22uF	CAP/N
4	1	C5	0.1uF	CAP/HDC-1206
5	26	C6,C7,C8,C9,C10,C11,C12, C13,C14,C15,C16,C17,C18, C19,C20,C21,C22,C23,C24, C25,C26,C27,C28,C29,C30, C39	open0402	CAP/HDC-0402
6	8	C31,C32,C33,C38,C43,C49, C54,C55	22uF	CAP/EIA-B 3528-21
7	8	C34,C37,C40,C44,C45,C48, C52,C53	0.1uF	CAP/HDC-0603
8	8	C35,C36,C41,C42,C46,C47, C50,C51	0.01uF	CAP/HDC-0603
9	2	JP2,JP1	3-Pin Header	Header/3P
10	1	JP3	2-Pin Header	Header/2P
11	1	J1	mini USB 5pin_open	mini_USB_surface_mount
12	1	J2	mini USB 5pin	mini_USB_surface_mount
13	1	J3	IDC2X25_Unshrouded	IDC-50
14	2	J4,J5	BANANA	CON/BANANA-S
15	1	R1	100 ohm,0402	RES/HDC-0402
16	1	R2	10K_open	RES/HDC-0805
17	3	R3,R4,R5	10K	RES/HDC-0805
18	8	R7,R8,R9,R10,R11,R12,R13, R14	0 Ohm,0402	RES/HDC-0402
19	1	S1	SW DIP-4	DIP-4
20	1	U1	DS99R106	48 pin TQFP

## Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

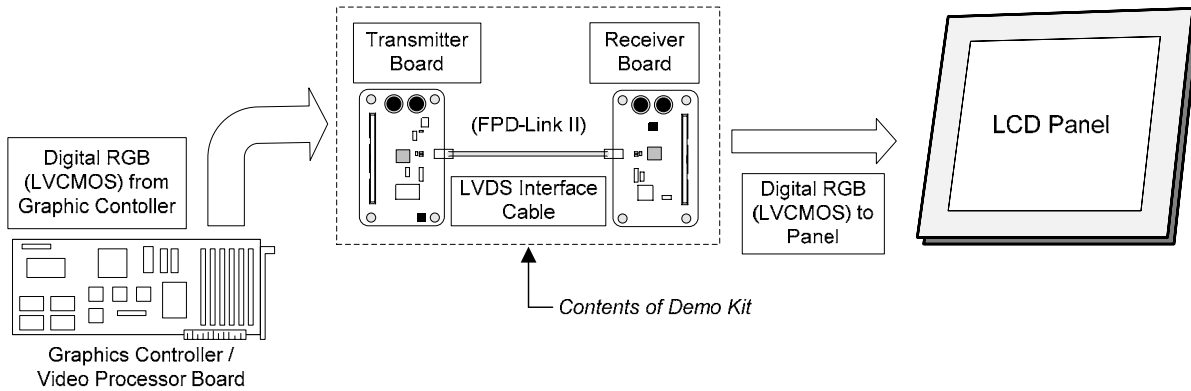
- 1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with digital RGB (LVCMOS) output.
- 2) Astro Systems VG-835 - This video generator may be used for video signal sources for 6-bit Digital LVCMOS/RGB.
- 3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
- 4) Optional – Logic Analyzer or Oscilloscope

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

- 1) LCD Display Panel which supports digital RGB (LVCMOS) inputs.
- 2) National Semiconductor DS99R105 Serializer (Tx)
- 3) Optional – Logic Analyzer or Oscilloscope
- 4) Any SCOPE with a bandwidth of at least 40MHz for LVCMOS and/or 1GHz for looking at the differential signal.

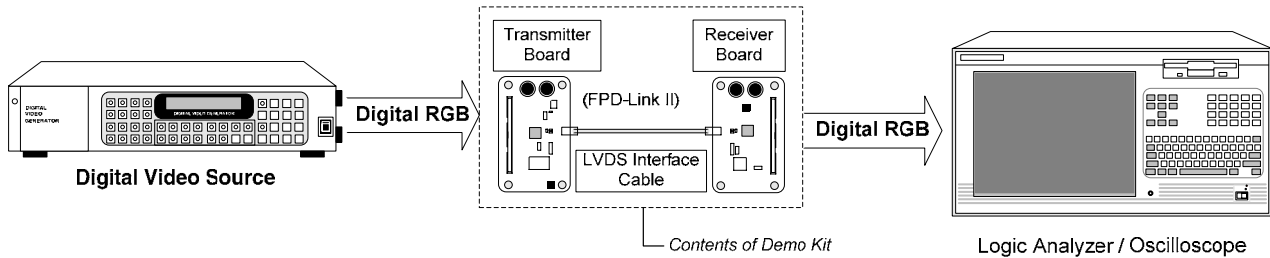
FPD-LINKII signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

The picture below shows a typical test set up using a Graphics Controller and LCD Panel.



**Figure 2. Typical SERDES Setup of LCD Panel Application**

The picture below shows a typical test set up using a generator and scope.



**Figure 3. Typical SERDES Test Setup for Evaluation**

# Troubleshooting

**NOTE: The DS99R105 and DS99R106 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.**

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

## QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards. The Serializer board should draw about 40-50mA with clock and all data bits switching at 40MHz. The De-serializer board should draw about 70-80mA with clock and all data bits switching at 40MHz.
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

## TROUBLESHOOTING CHART

Problem...	Solution...
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin.  Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly.  Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and De-serializer boards to make sure that the devices are enabled (/PD=Vcc) for operation. Also check DEN on the Serializer board and REN on the Deserializer board is set HIGH.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or hardware supplier.

## Equipment References

Digital Video Pattern Generator – Astro Systems VG-835 (or equivalent):

Astro Systems  
425 S. Victory Blvd. Suite A  
Burbank, CA 91502  
Phone: (818) 848-7722  
Fax: (818) 848-7799  
[www.astro-systems.com](http://www.astro-systems.com)

## Extra Component References

TDK Corporation of America  
1740 Technology Drive, Suite 510  
San Jose, CA 95110  
Phone: (408) 437-9585  
Fax: (408) 437-9591  
[www.component.tdk.com](http://www.component.tdk.com)  
Optional EMI Filters – TDK Chip Beads (or equivalent)

## Cable References

The FPD-LINKII interface cable included in the kit is a standard off-the-shelf high-speed USB 2.0 with a 4-pin USB A type on one end and a 5-pin mini USB on the other end and is included for demonstration purposes only.

**NOTE: The DS99R105 and DS99R106 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.**

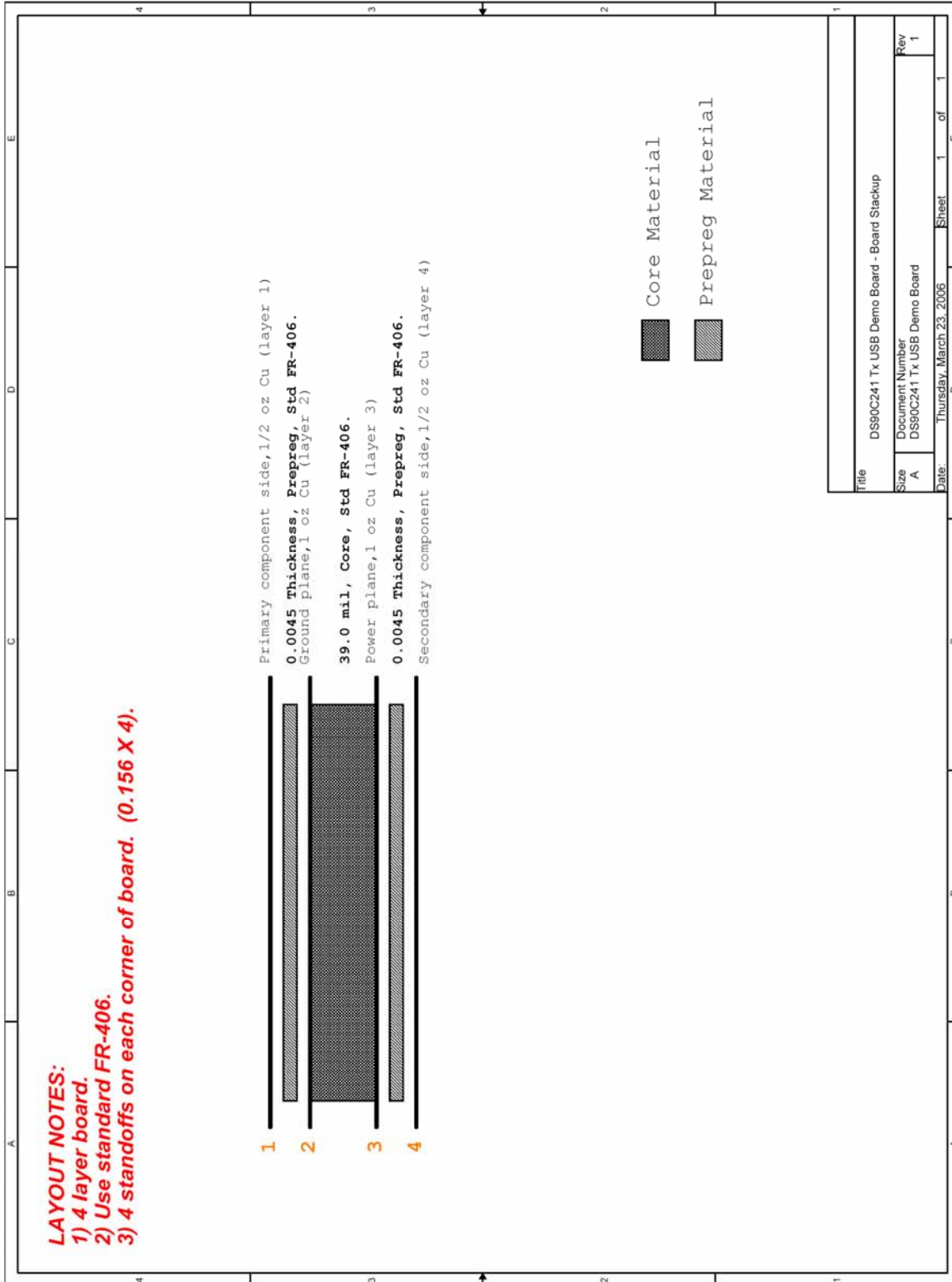
The inclusion of the USB cable in the kit is for:

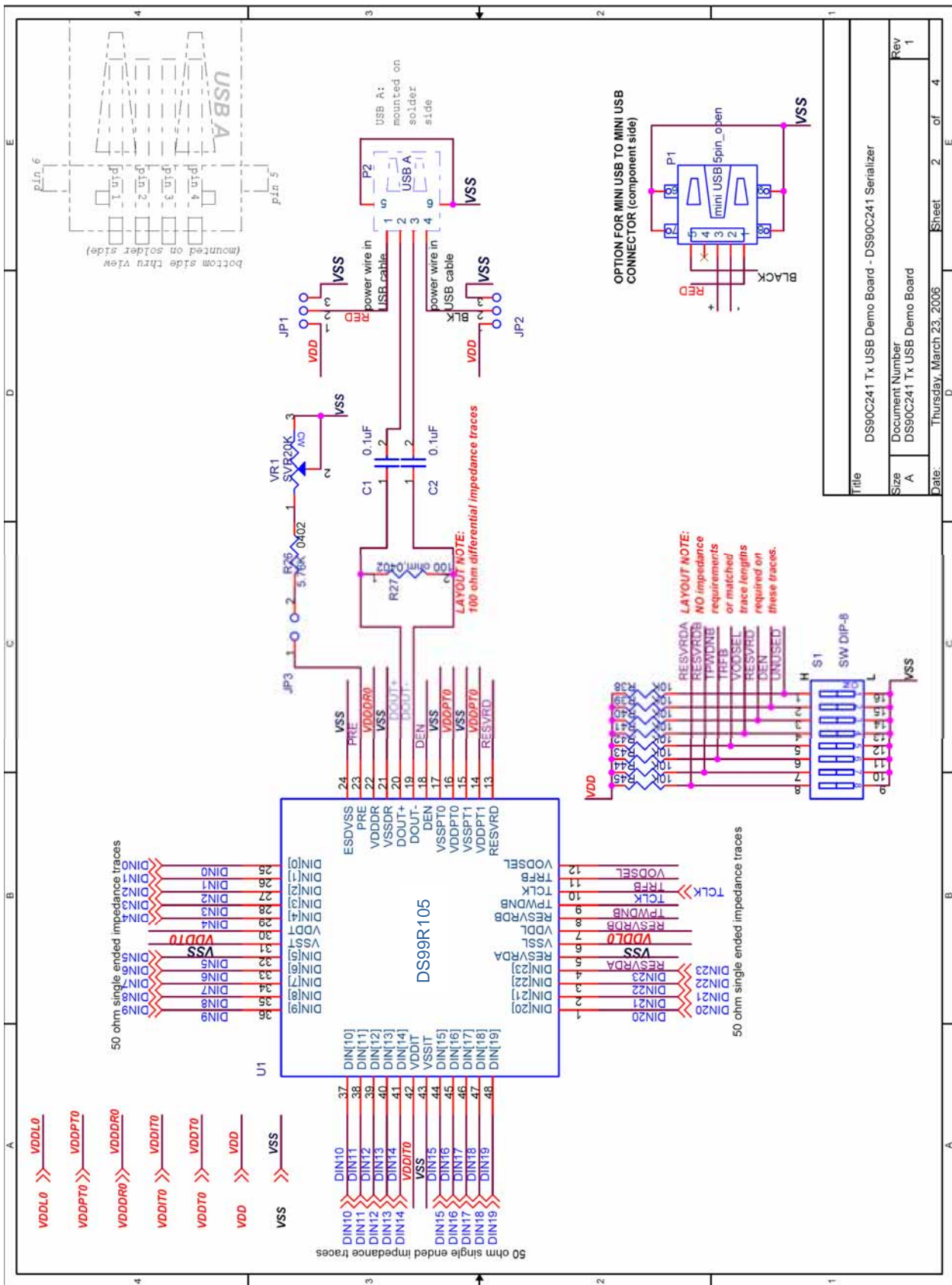
- 1) Demonstrating the robustness of the FPD-LINKII link over ordinary twisted pair data cables.
- 2) Readily available and in different lengths without having custom cables made.

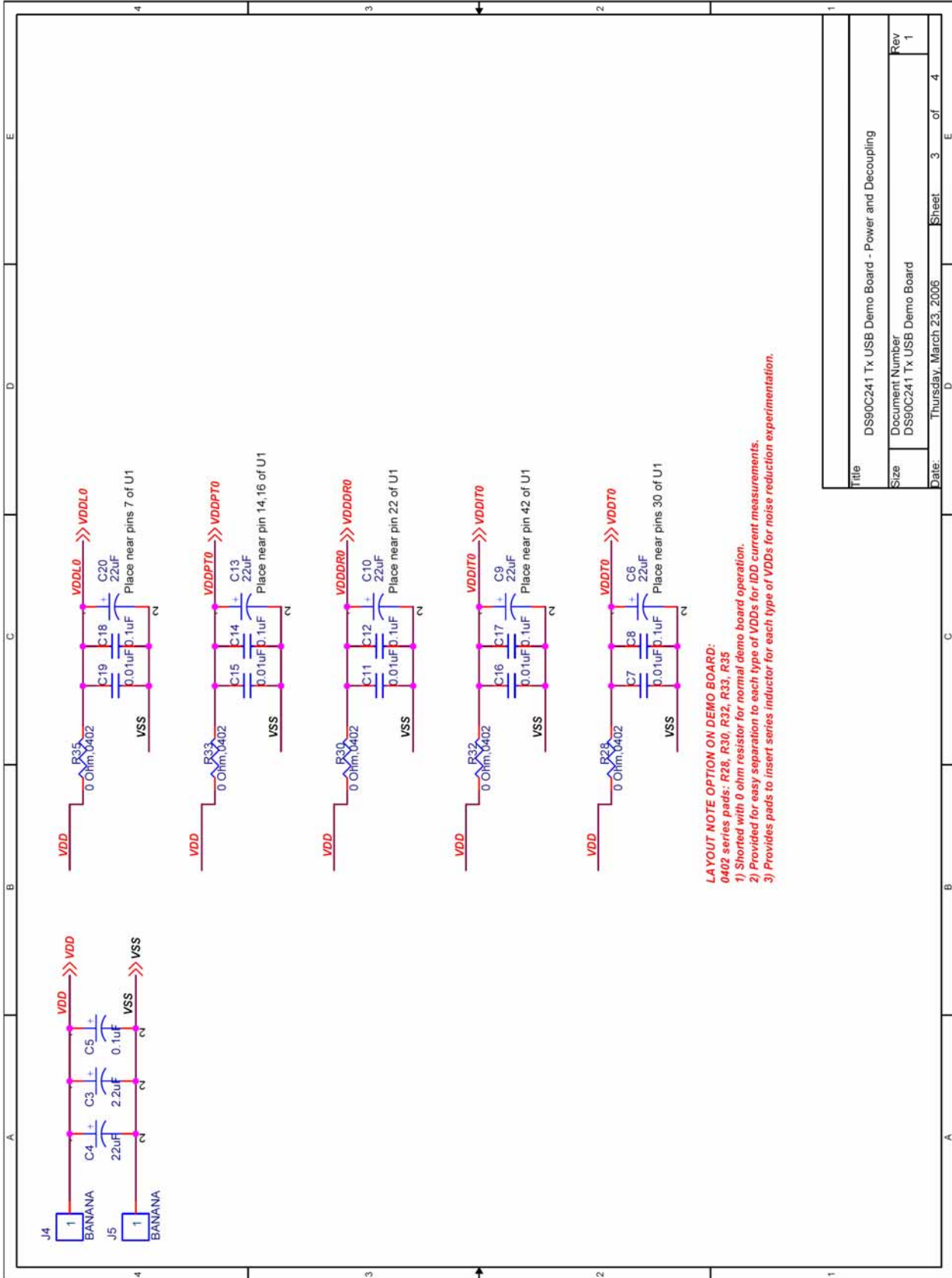
- For optimal performance, we recommend Shielded Twisted Pair (STP) 100Ω differential impedance cable for high-speed data applications.

# Appendix

## Serializer (Tx) PCB Schematic:

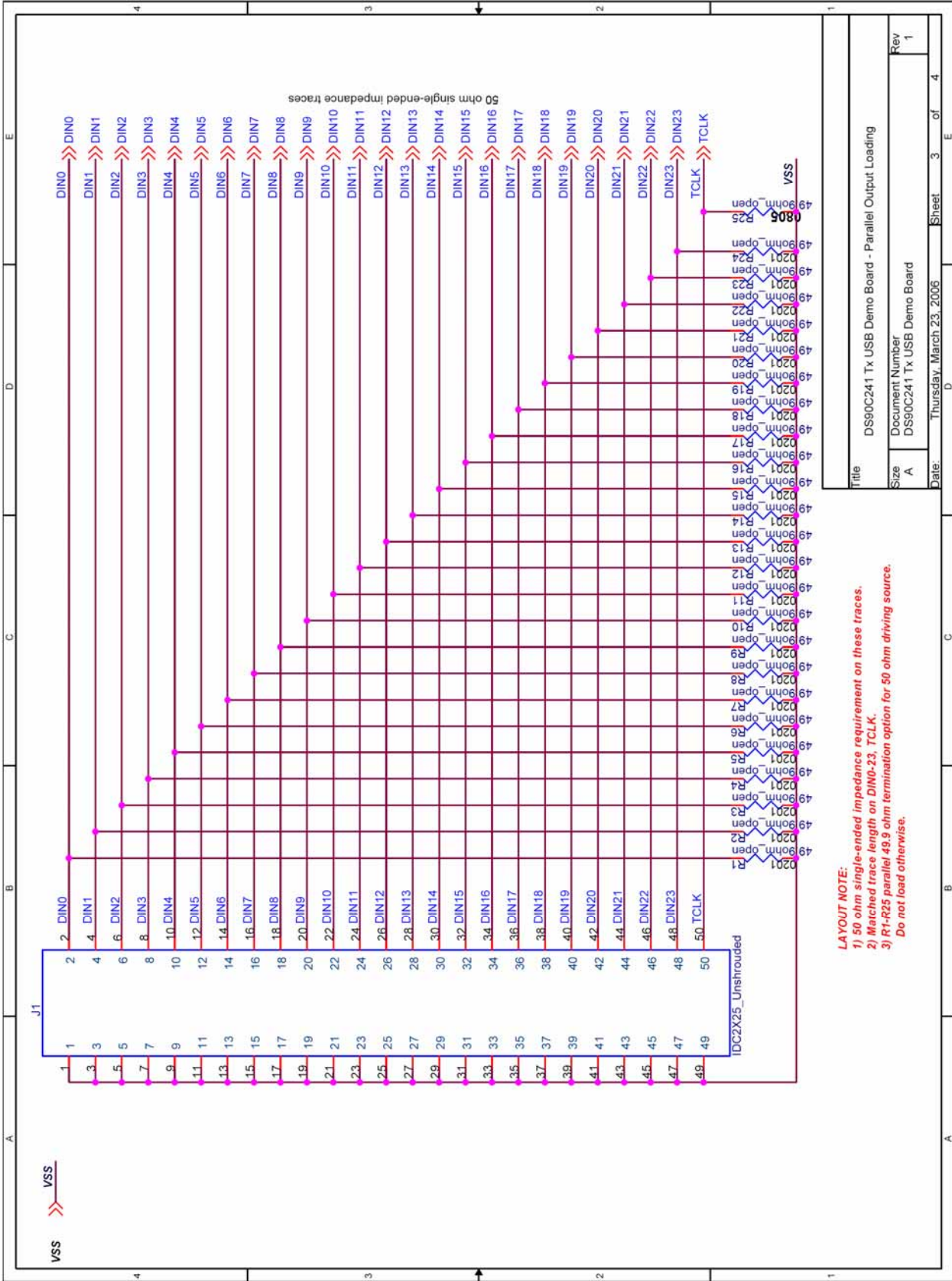




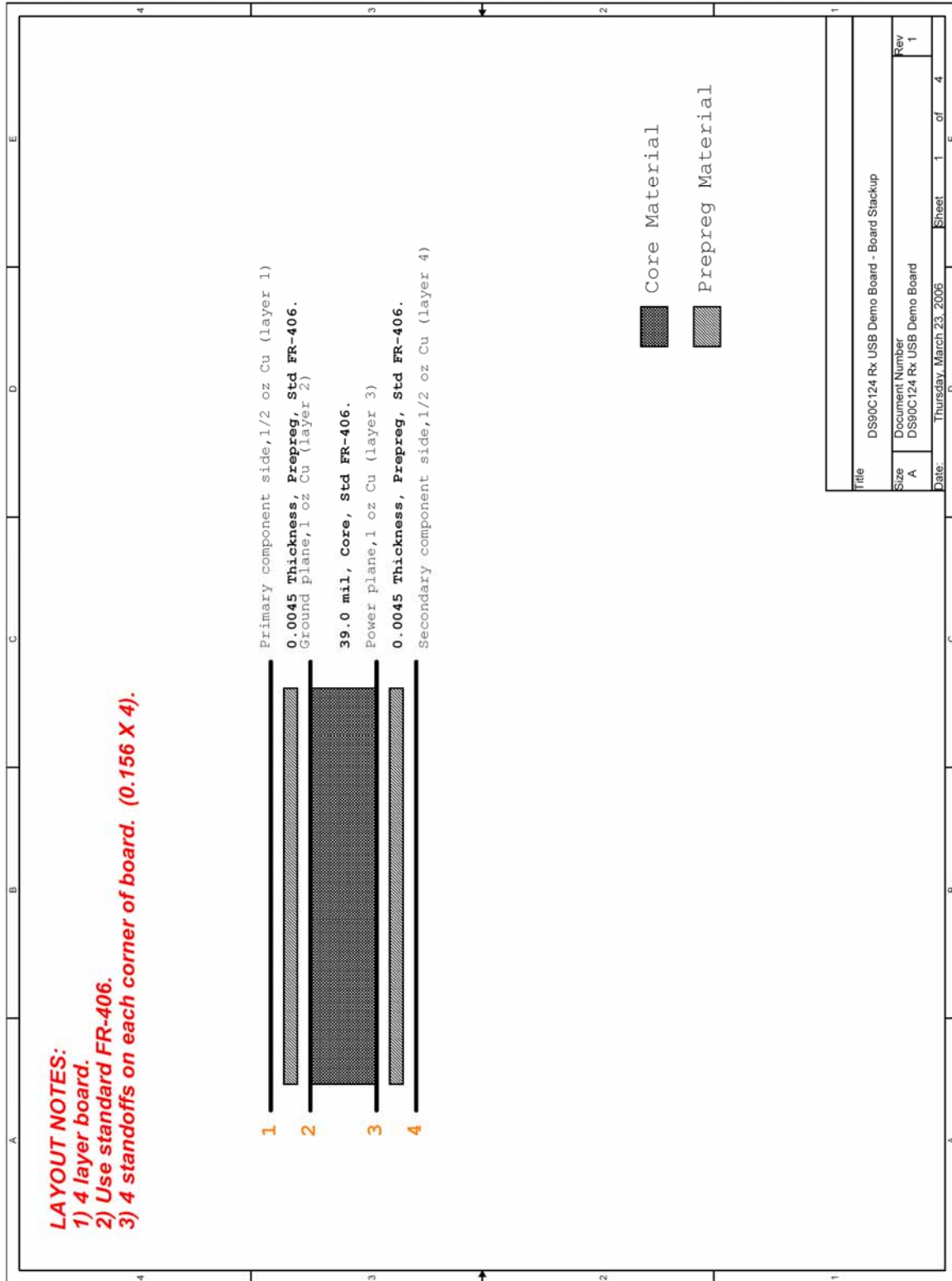


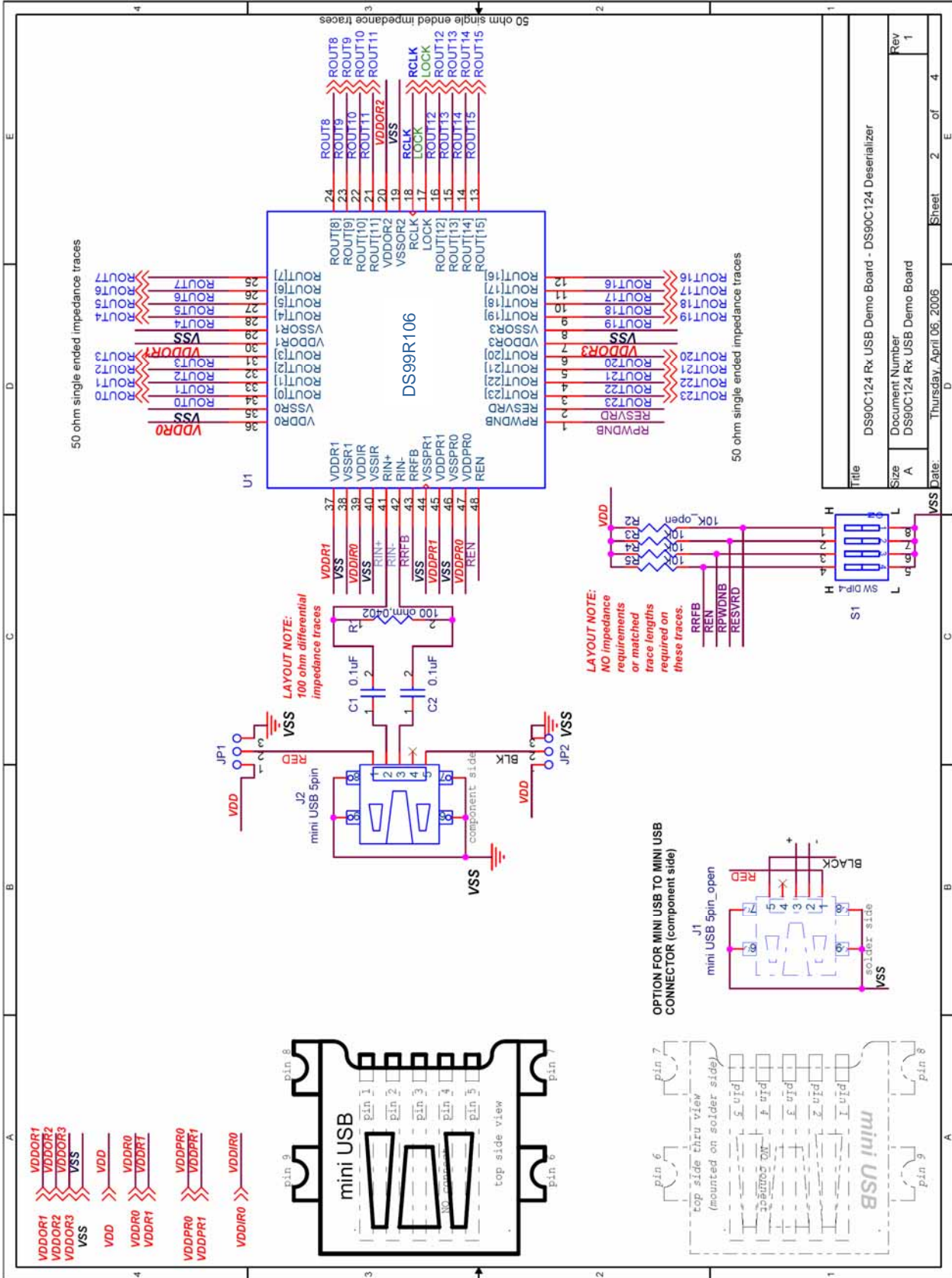
Title	DS99R105 Tx USB Demo Board - Power and Decoupling		
Size	Document Number	Rev	
	DS99R105 Tx USB Demo Board	1	
Date	Thursday, March 23, 2006	Sheet	3 of 4

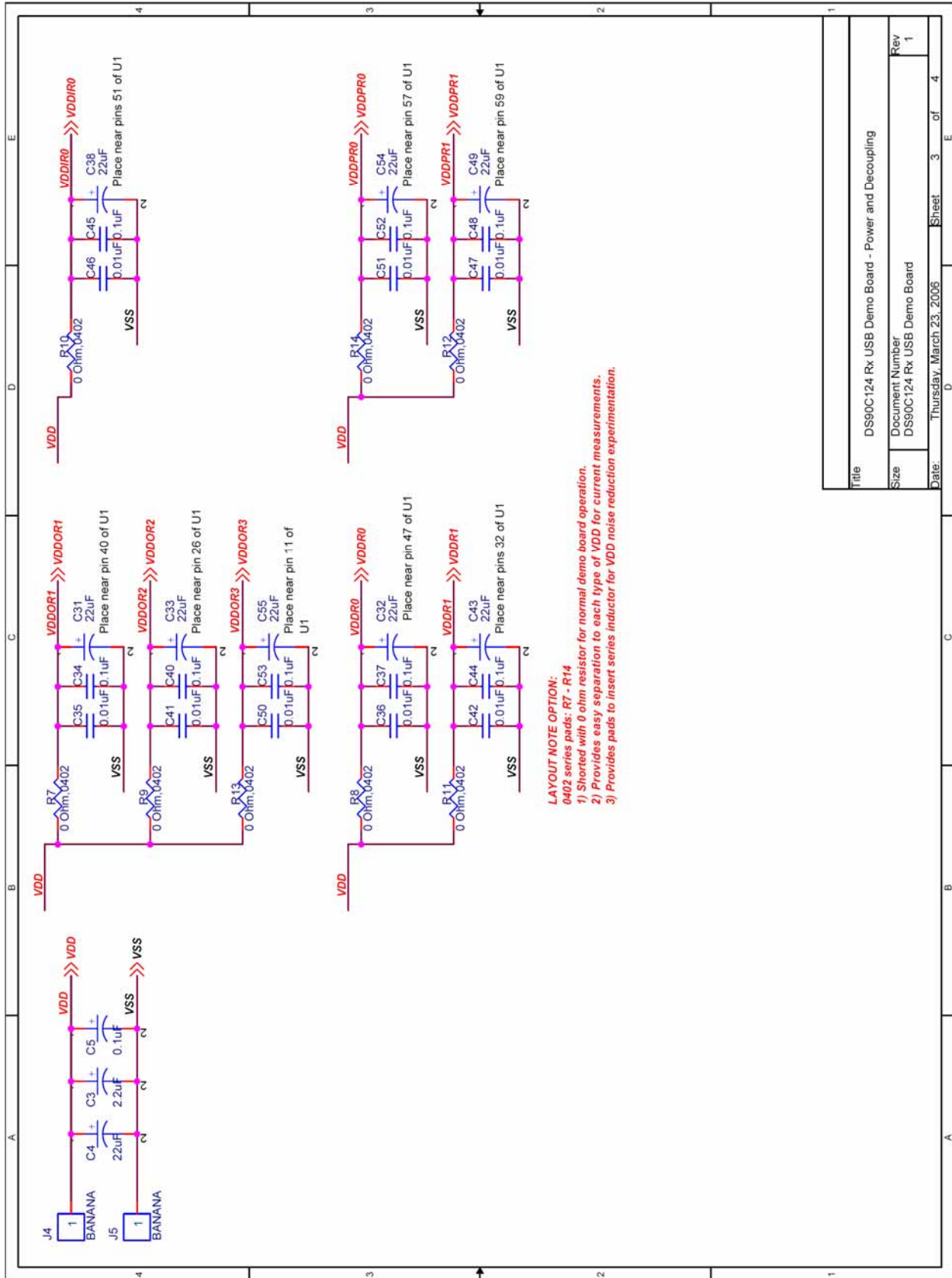




## De-serializer (Rx) PCB Schematic:

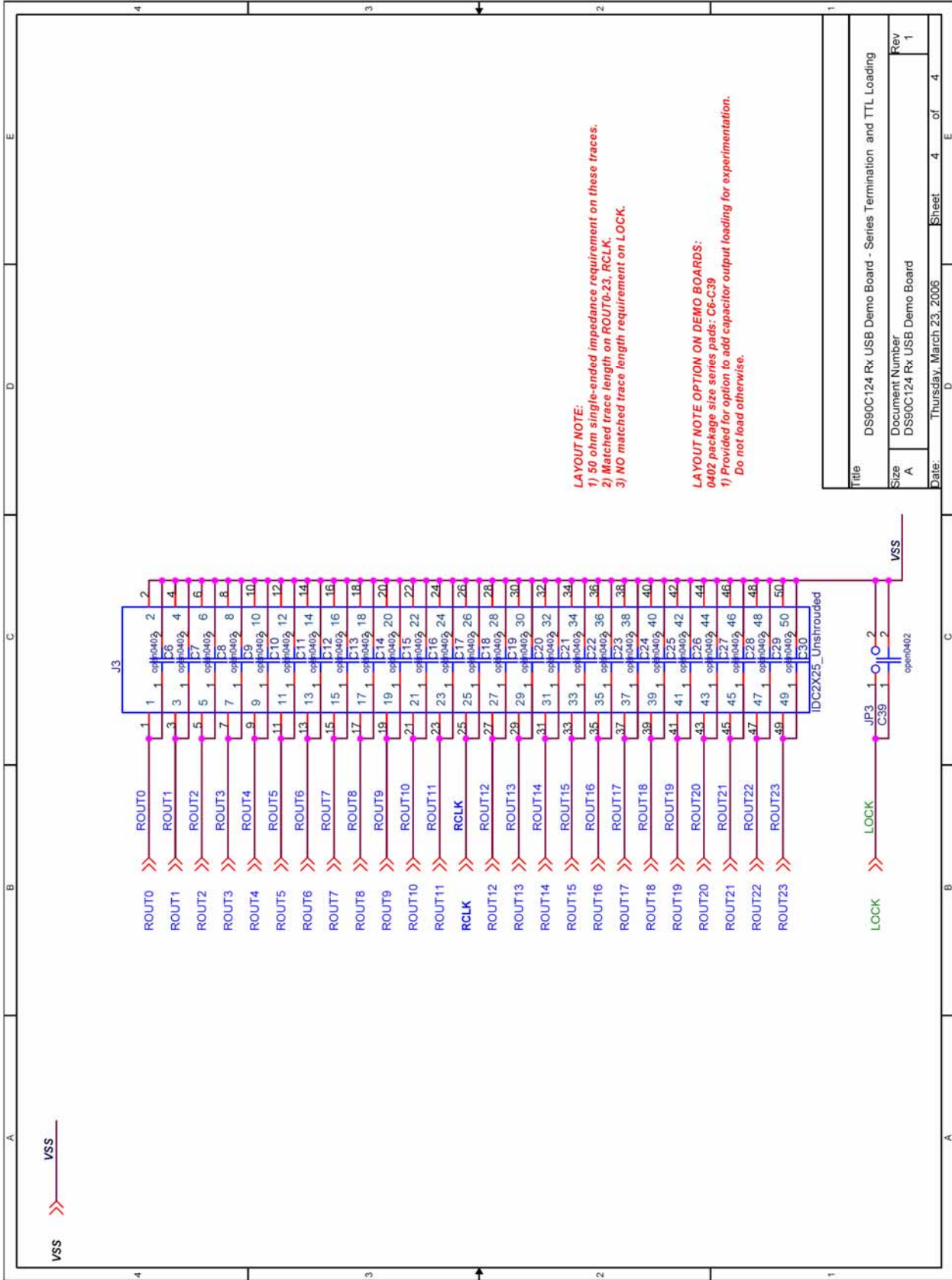






Title	DS99R105/106 USB Demo Board - Power and Decoupling		
Size	Document Number	Rev	
	DS99R105/106 USB Demo Board	1	
Date:	Thursday, March 23, 2006	Sheet	3 of 4



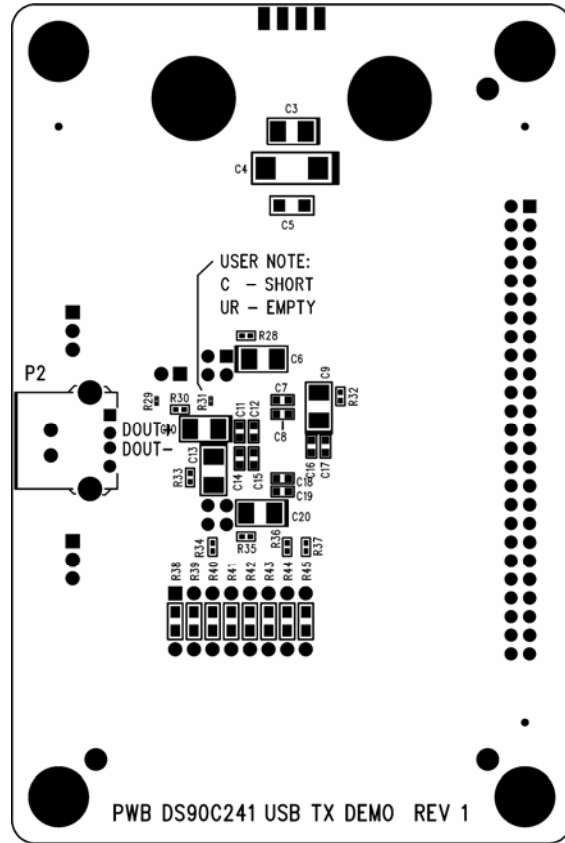
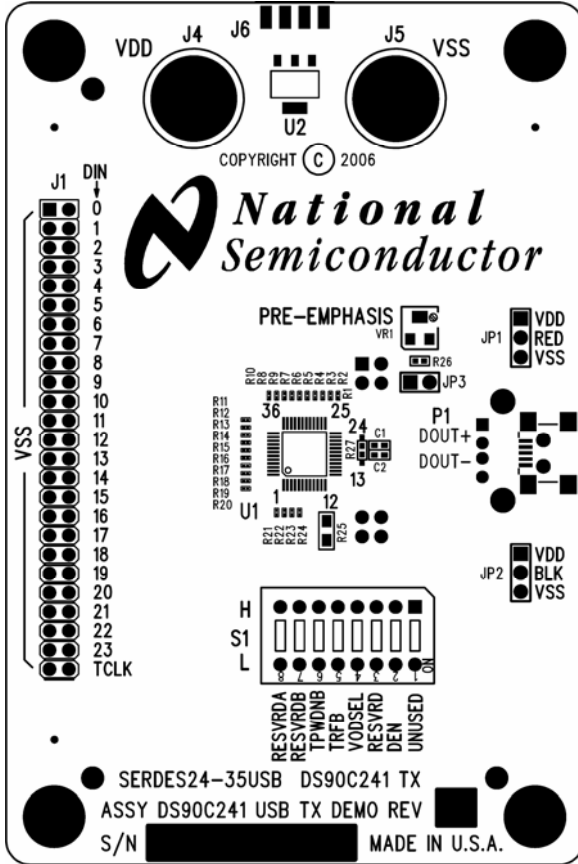


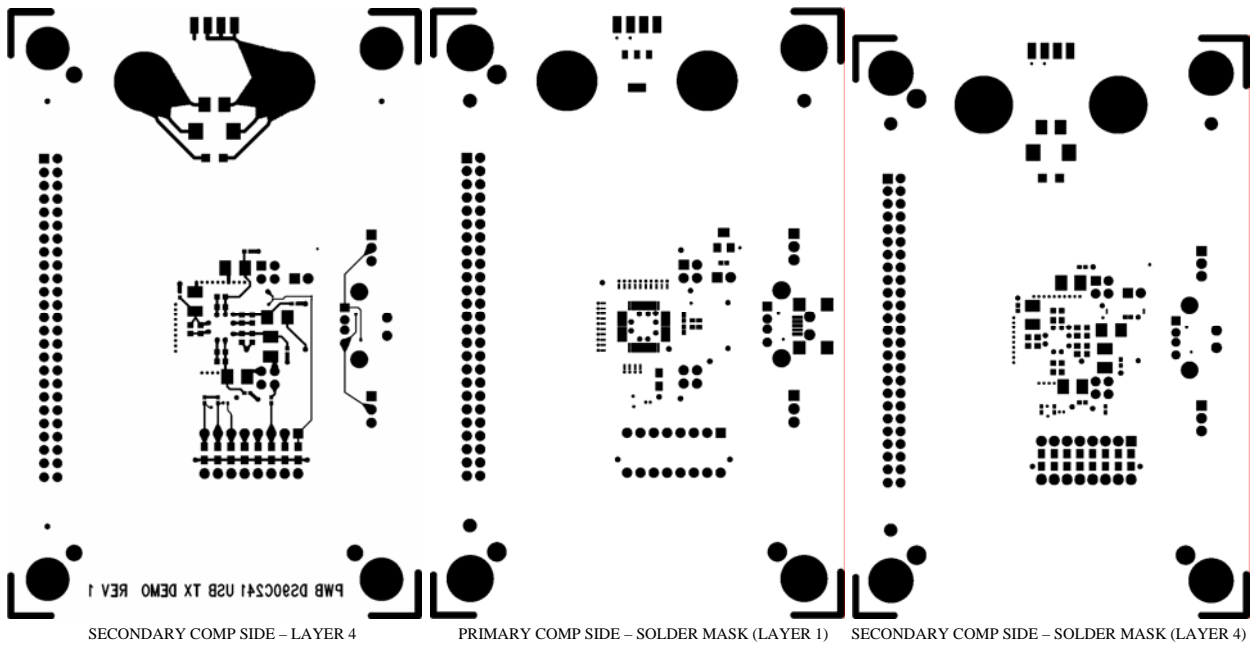
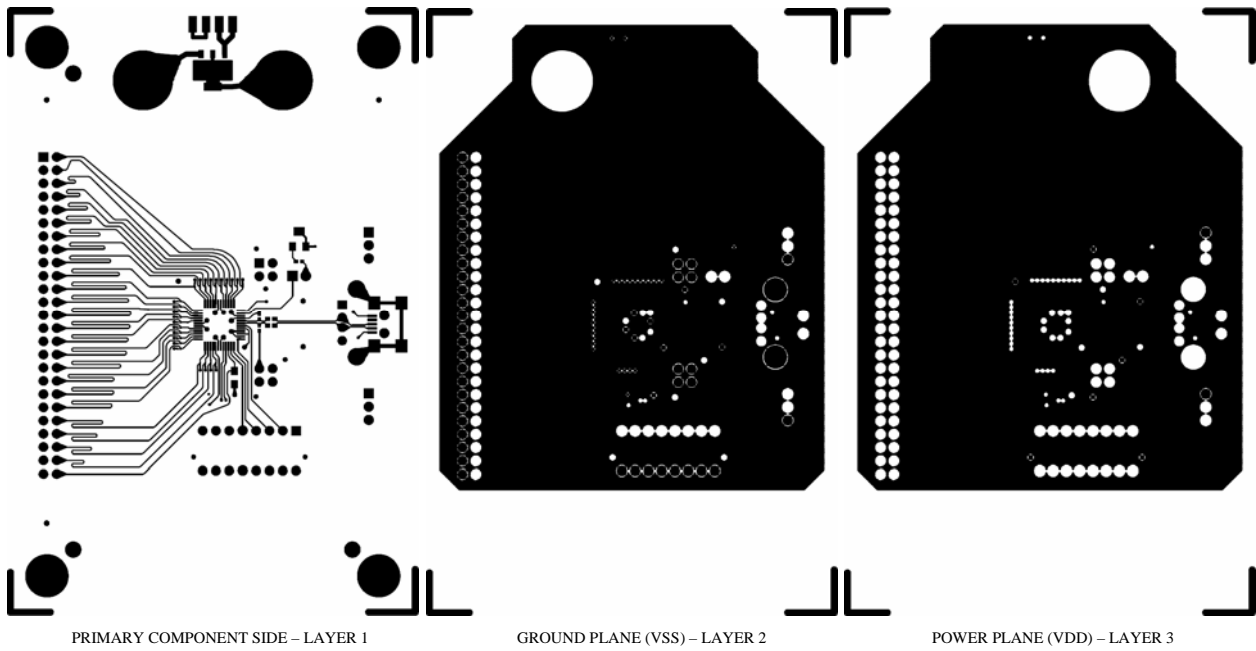
**LAYOUT NOTE:**  
 1) 50 ohm single-ended impedance requirement on these traces.  
 2) Matched trace length on ROUT0-23, RCLK.  
 3) NO matched trace length requirement on LOCK.

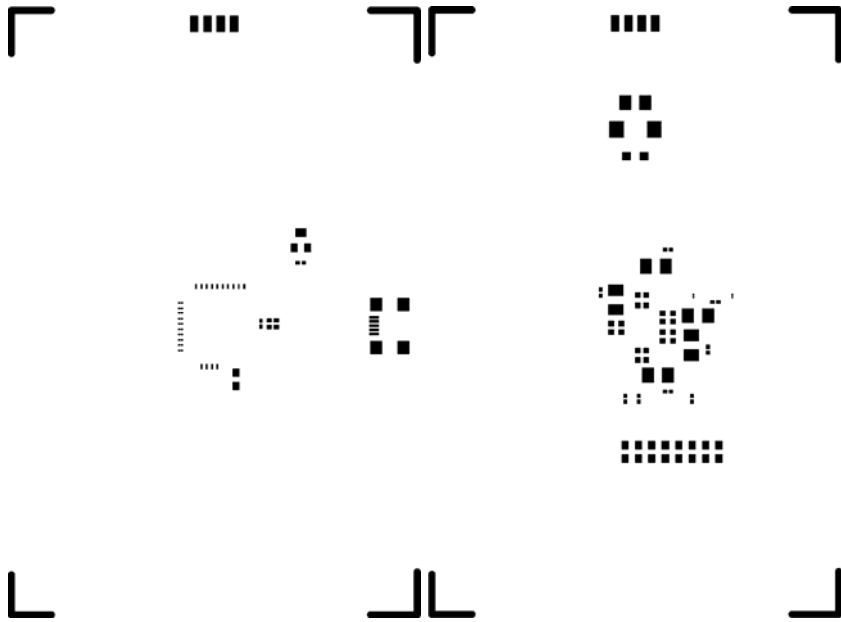
**LAYOUT NOTE OPTION ON DEMO BOARDS:**  
 0402 package size series pads: C6-C39  
 1) Provided for option to add capacitor output loading for experimentation.  
 Do not load otherwise.

Title		DS90C124 Rx USB Demo Board - Series Termination and TTL Loading	
Size	Document Number	Rev	
A	DS90C124 Rx USB Demo Board	1	
Date:	Thursday, March 23, 2006	Sheet	4 of 4

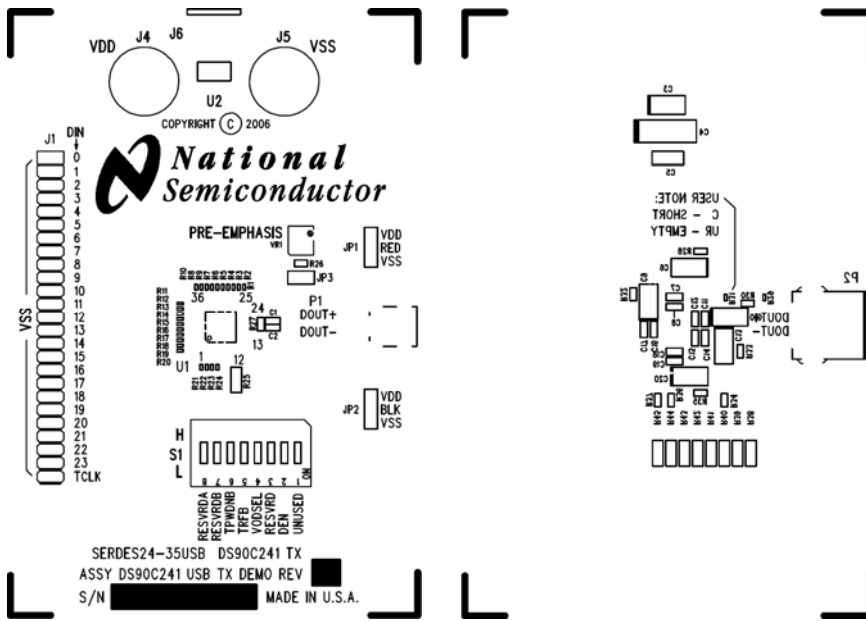
# Serializer (Tx) PCB Layout:







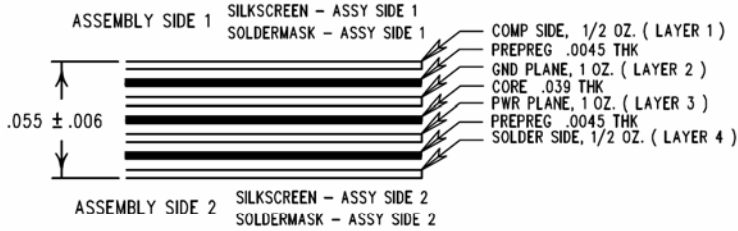
PRIMARY COMP SIDE - SOLDER PASTE (LAYER 1)      SECONDARY COMP SIDE - SOLDER PASTE (LAYER 4)



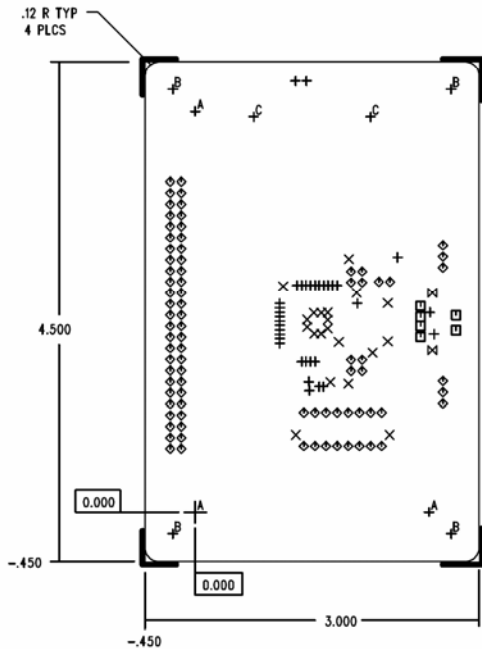
PRIMARY COMP SIDE - SILKSCREEN (LAYER 1)      SILKSCREEN COMP SIDE - SILKSCREEN (LAYER 4)



# Serializer (Tx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	34	YES	± .003
×	0.014	20	YES	± .003
□	0.036	6	YES	± .003
◇	0.043	82	YES	± .003
⊗	0.091	2	YES	± .003
A	0.125	3	NO	+ .003 - .000
B	0.156	4	YES	± .004
C	0.265	2	YES	± .005

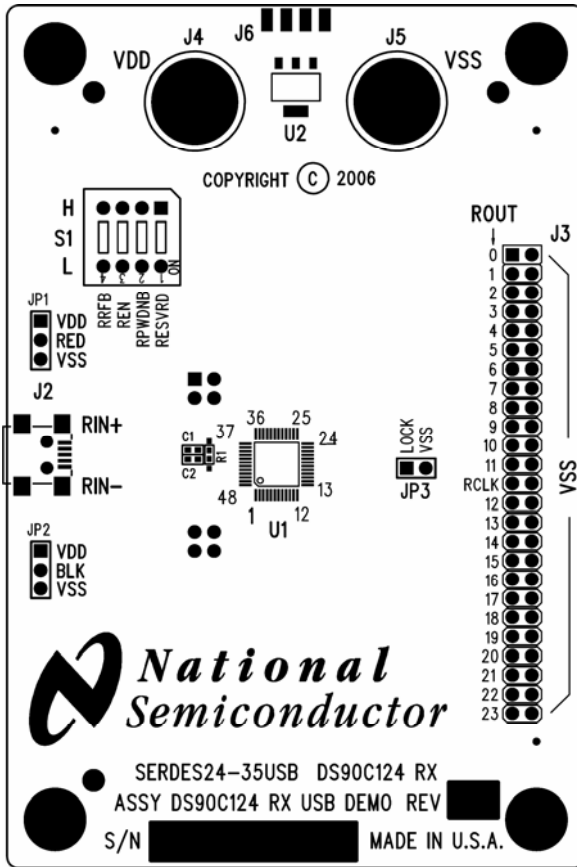


NATIONAL SEMICONDUCTOR CORP.  
 DS90C241 USB TX DEMO BOARD  
 PWB DS90C241 USB TX DEMO REV 1  
 DRILL DRAWING

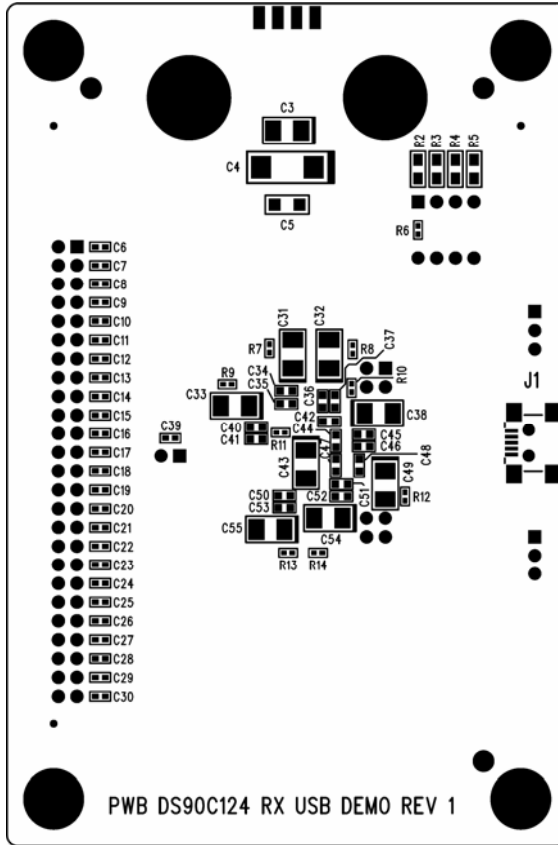
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90C241 USB TX DEMO REV 1. USE GERBER FILE A457B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR-406, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ FOR OUTSIDE LAYERS AND 1 OZ FOR INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. SURFACE FINISH: GOLD FLASH .000004 MIN.
7. FABRICATION TOLERANCES:  
 END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE, AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/- 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

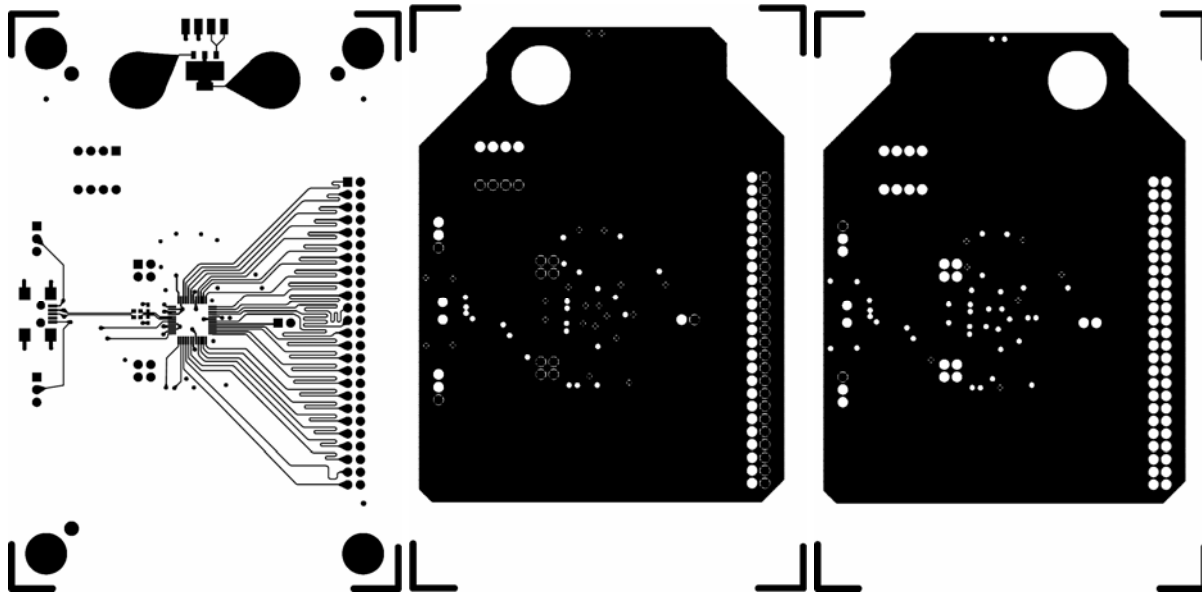
# Deserializer (Rx) PCB Layout:



TOP VIEW



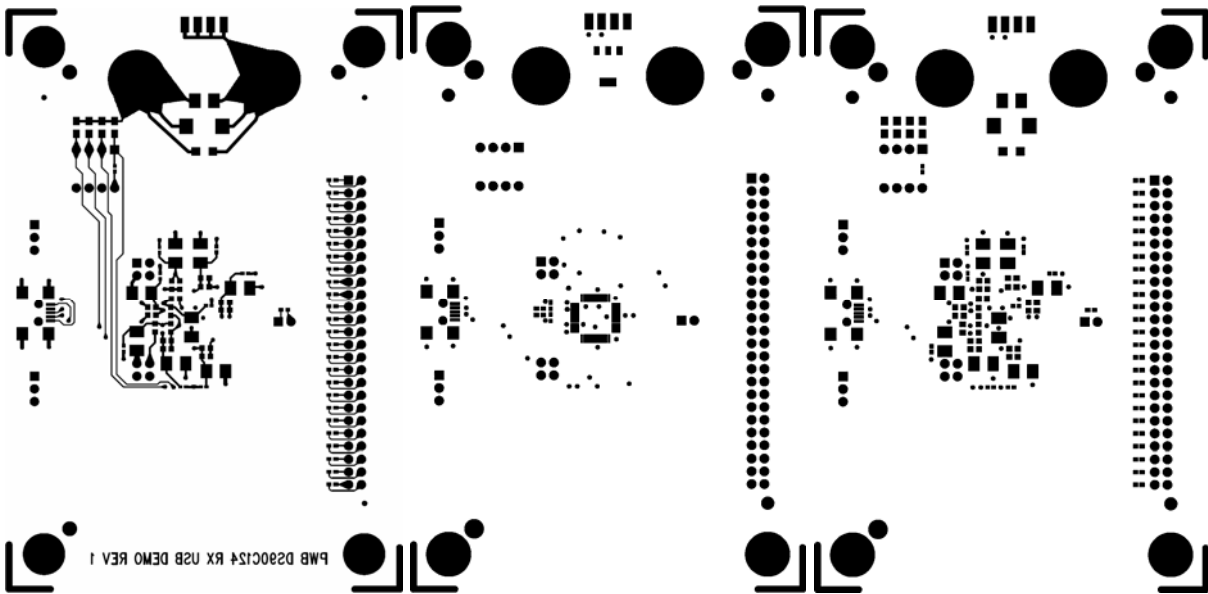
BOTTOMSIDE VIEW



PRIMARY COMPONENT SIDE – LAYER 1

GROUND PLANE (VSS) – LAYER 2

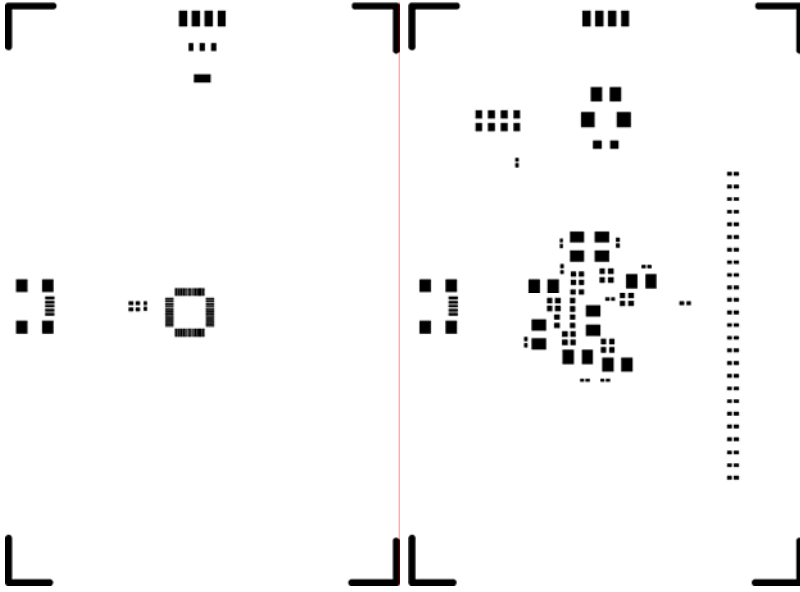
POWER PLANE (VDD) – LAYER 3



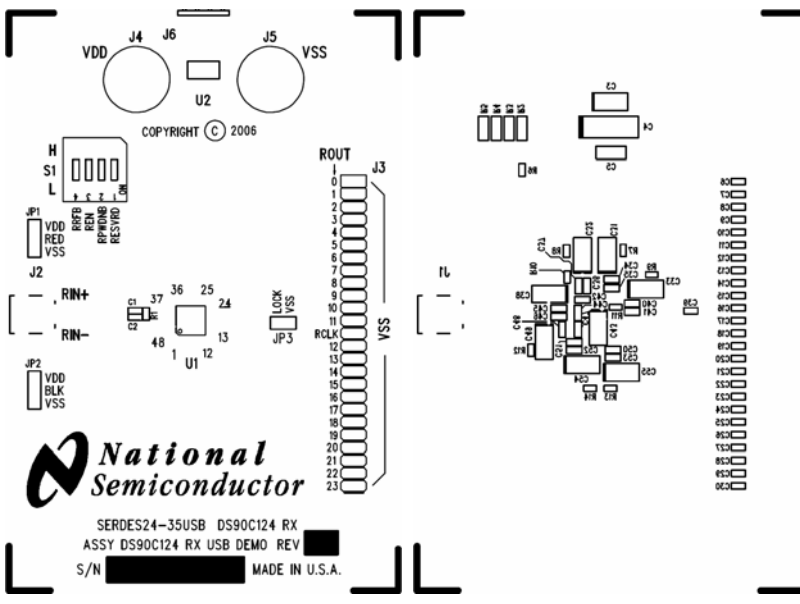
SECONDARY COMP SIDE – LAYER 4

PRIMARY COMP SIDE – SOLDER MASK (LAYER 1)

SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

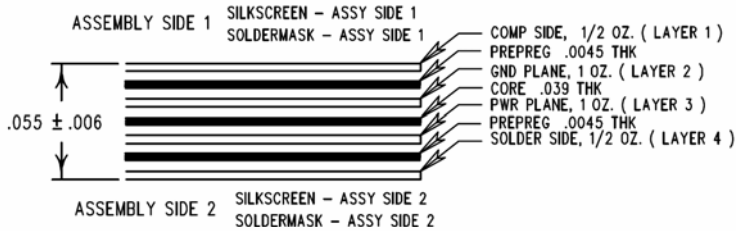


PRIMARY COMP SIDE - SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE - SOLDER PASTE (LAYER 4)

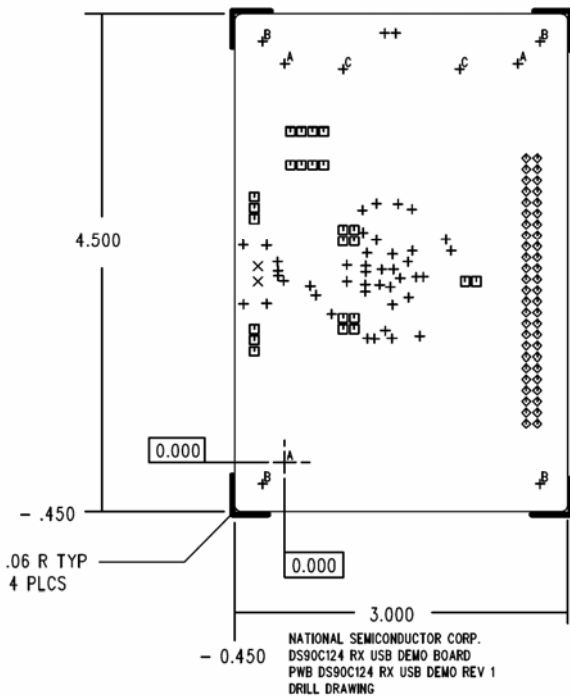


PRIMARY COMP SIDE - SILKSCREEN (LAYER 1) SILKSCREEN COMP SIDE - SILKSCREEN (LAYER 4)

# Deserializer (Rx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.012	45	YES	± .003
×	0.035	2	YES	± .003
□	0.040	24	YES	± .003
◇	0.045	50	YES	± .003
A	0.125	3	NO	+ .003 - .000
B	0.156	4	YES	± .005
C	0.265	2	YES	± .005



**NOTES: UNLESS OTHERWISE SPECIFIED**

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90C124 RX USB DEMO REV 1. USE BOARD OUTLINE FILE A459B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR-406, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ. OUTSIDE LAYERS AND 1 OZ INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. GOLD FLASH .000005 MIN.
7. FABRICATION TOLERANCES:  
END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .003 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/- 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

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