FPGA-Link BIST Instructions

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Introduction

The DS32ELX0421/DS32EL0421 and DS32ELX0124/DS32EL0124 FPGA-Link SerDes are capable of driving up to 3.125 Gbps of data across long distances though a variety of interconnects. To assist system designers with component level debug and signal integrity analysis, a Bit Internal Set Test (BIST) module was included in the FPGA-Link SerDes.

When the serializer BIST is enabled, the device can be set to generate pseudo random bit sequences (PRBS) or to output a short user defined pattern. In BIST mode, the deserializer can perform error checks on the incoming high speed data. The deserializer can also be configured to transmit BIST patterns on the parallel LVDS outputs to verify the link to the host device, typically an FPGA.

1.0 DC Balanced Custom Pattern High Speed BIST

Pattern BIST allows user to program 64 bits of data which will be DC Balanced by an 8b10b encoder. This DC balanced user defined pattern is then transmitted from the Serializer to the Deserializer where the 64 bit pattern is decoded and compared against an expected value. Users are not allowed to transmit or error check "K" characters. The Deserializer will set a register indicating that received data was correct and that receive BIST completed its operation. If there are any errors in the received patterns a bit is set indicating a problem. User can choose to send and receive 80 bits of data at a time or in a repeating fashion.

1.1 Serializer and Deserializer Device Configuration

The Serializer and Deserializer must be configured with both DC Balance and Remote Sense disabled. This is achieved by driving the DC_B* pin LOW and the RS* pin LOW. If the configuration pins are changed after power up or at any time during BIST operation, the devices must be reset.

To begin using the BIST, a valid clock must be applied to the TxCLKIN LVDS inputs of the serializer. Once a clock has been applied, the serializer and deserializer must both report lock before programming the devices to into the BIST mode.

1.2 Programming Deserializer Registers

Program register 0x20 to 0x40 (disable Data valid operation in auto link mode)
Program register: 0A, 0C, 0E, 10, 12,14,16,18 to 0x00 (Disable sending K characters)
Program register: 09, 0B, 0D, 0F, 11,13,15,17 to 80 bit of desired receive pattern
Program register: 0x36 to 0x01 (enable pattern BIST)

Program register: 0x38 to 0x0A (repeat=1) or program to 0x02 (repeat=0)
When repeat is enabled, the same pattern is received over and over again.

1.3 Programming Serializer Registers

Program register 0x21 to 0x40 (disable Data valid operation in auto link mode)
Program register: 0A, 0C, 0E, 10, 12,14,16,18 to 0x00
Program register : 09,0B,0D,0F,11,13,15,17 to 80 bit of desired send pattern, must match what's programmed in the Deserializer
Program register: 0x39 to 0x01 (enable pattern BIST)
Program register: 0x3B to 0x09 (repeat=1) or program to 0x01 (repeat=0)
When repeat is enabled, the same pattern is sent over and over again.

1.4 Checking BIST Status

Read Register 0x3B[3:1] in the Deserializer:
If repeat = 0 , 3B[3:1] = 3'b000 indicates correct reception of patterns; reg 3A=8'hff pattern is running

If repeat = 1, 3B[3:1] = 3'b111 indicates error free operation. Any other value indicates that there is a programming or pattern problem.

2.0 DC Balanced PRBS High Speed BIST

The serializer contains a linear feedback shift registers (LFSR), which can be enabled to generate three different pseudo random bit sequences for high speed BIST. While in BIST mode, the internally generated patterns are transmitted from the serializer and checked against the expected pattern in the deserializer. The serializer and deserializer support PRBS-9, 16 and 18.

2.1 Serializer and Deserializer Device Configuration

Similar to the user defined DC balanced pattern configuration Section 1.0, the serializer and deserializer must be configured with both DC Balance and Remote Sense enabled. Both the DC_B* and RS* pins must be pulled to logic LOW.

2.2 Programming Deserializer registers

First, select a pseudo random bit sequence by programming deserializer register 0x33.
lfsr 9
Program register 0x33 to 0x03
lfsr 16
Program register 0x33 to 0x00
lfsr 18
Program register 0x33 to 0x02

Program register: 0x38 to 0x0A (repeat=1) or program to 0x02 (repeat=0)
When repeat is enabled, the same pattern is received over and over again.

2.3 Programming Serializer registers

The pseudo random bit sequence generator control bits are found in register 0x39 of the serializer. Be sure to select the same pseudo random bit sequence that was programmed into the deserializer.

lfsr 9
Program register 39 to 0x06
lfsr 16
Program register 39 to 0x00
lfsr 18
Program register 39 to 0x02

Program register: 0x3B to 0xC9 (repeat=1) or program to 0xC1 (repeat=0)
When repeat is enabled, the same pattern is sent over and over again.

2.4 Checking Status

Read Register 0x3B[3:1] in the Deserializer:
If repeat = 0 , 3B[3:0] = 4'b0011 indicates correct reception of patterns
If repeat = 1, 3B[3:0] = 4'b0001 indicates error free operation. Any other value indicates that there is a programming or pattern problem.

Read Number of Errors, read register 3A keeps count up to 8'hff.

3.0 Raw Pattern BIST from TX to RX

Pattern BIST in raw mode allows user to program 80 bits of data which will be transmitted scrambled from the Serializer to the Deserializer, where it will be unscrambled and checked against the expected value. The Deserializer will set a register indicating that received data was correct and that receive BIST completed its operation. If there are any errors in the transmitted patterns a bit is set to indicate a problem. User can choose to send and receive 100 bits of data repeatedly.

3.1 Serializer and Deserializer mode selection

The Serializer and Deserializer must be configured to be in raw link mode. This is achieved by driving the following pins
MODE0 = 1
MODE1 =0
Reset must be applied to device upon any change of input MODE pins.

TX_LVDS = clock must be applied to the Serializer TX interface, with desired and valid frequency.

Upon setting the above pins user must wait for LOCK_N pins to become Zero on both Serializer and Deserializer.

3.2 Programming Deserializer registers

Following is address for the bank of registers that can be used in pattern bist
Registers {0A[1:0],09[7:0]} → 1st 10 bit ordered set to be received
Registers {0C[1:0],0B[7:0]} → 2nd 10 bit ordered set to be received
Registers {0E[1:0],0D[7:0]} → 3rd 10 bit ordered set to be received
Registers {10[1:0],0F[7:0]} → 4th 10 bit ordered set to be received
Registers {12[1:0],11[7:0]} → 5th 10 bit ordered set to be received
Registers {14[1:0],13[7:0]} → 6th 10 bit ordered set to be received
Registers {16[1:0],15[7:0]} → 7th 10 bit ordered set to be received
Registers {18[1:0],17[7:0]} → 8th 10 bit ordered set to be received

Program register: 0x36 to 0x01 (enable pattern BIST)
Program register: 0x38 to 0x0A (repeat=1) or program o 0x02 (repeat=0)
When repeat is enabled same pattern is received over and over again

3.3 Programming Serializer registers

Following is address for the bank of registers that can be used in pattern BIST. Registers {0A[1:0],09[7:0]} → 1st 10 bit ordered set to be received
Registers {0C[1:0],0B[7:0]} → 2nd 10 bit ordered set to be received
Registers {0E[1:0],0D[7:0]} → 3rd 10 bit ordered set to be received
Registers {10[1:0],0F[7:0]} → 4th 10 bit ordered set to be received
Registers {12[1:0],11[7:0]} → 5th 10 bit ordered set to be received
Registers {14[1:0],13[7:0]} → 6th 10 bit ordered set to be received
Registers {16[1:0],15[7:0]} → 7th 10 bit ordered set to be received
Registers {18[1:0],17[7:0]} → 8th 10 bit ordered set to be received

Program register: 0x39 to 0x01 (enable pattern BIST)
Program register: 0x3B to 0x09 (repeat=1) or to 0x01 (repeat=0)
When repeat enabled pattern is send over and over

3.4 Checking Status

Read Register 0x3B[3:1] in the Deserializer:
If repeat = 0 , 3B[3:1] = 3'b000 indicates correct reception of patterns; reg 3A=8'hff pattern running

If repeat = 1, 3B[3:1] = 3'b111 indicates error free operation. Any other value indicates that there is a programming or pattern problem.

4,0 8b10b Raw mode LFSR BIST from TX to RX

LFSR BIST allows internally generated patterns to be transmitted from TX and checked against the expected pattern in the Deserializer. The SerDes supports 9, 16 or 18 bit LFSR. There is an error counter which can be read for the number of mismatches.

4.1 Serializer and Deserializer mode selection

Same mode selection process of pattern BIST as in Section 3.1.

4.2 Programming Deserializer registers

lfsr 9
Program register 33 to 0x03
lfsr 16
Program register 33 to 0x00
lfsr 18
Program register 33 to 0x02

Program register: 0x38 to 0x0A (repeat=1) or program to 0x02 (repeat=0)
When repeat is enabled, the same pattern is received over and over again.

4.3 Programming Serializer registers

lfsr 9
Program register 39 to 0x06
lfsr 16
Program register 39 to 0x00
lfsr 18
Program register 39 to 0x02

Program register: 0x3B to 0xC9 (repeat=1) or program to 0xC1 (repeat=0)
When repeat is enabled, the same pattern is sent over and over again.

4.4 Checking Status

Read Register 0x3B[3:1] in the Deserializer:
If repeat = 0 , 3B[3:0] = 4'b0011 indicates correct reception of patterns
If repeat = 1, 3B[3:0] = 3'b0001 indicates error free operation. Any other value indicates programming or pattern problem.

Read Number of Errors, read register 3A keeps count up to 8'hff.

5.0 Deserializer LVDS User Defined Pattern Generator

The Deserializer has the ability to transmit an 80 bit pattern from its LVDS outputs. This configuration can be used to validate the signal integrity of the parallel links and validate the timing settings of the host device.

5.1 Serializer and Deserializer mode selection

The Serializer and Deserializer must be configured with both DC Balance and Remote Sense disabled. This is achieved by driving the following pins:
MODE0 = 1
MODE1 = 1
Reset must be applied to device upon any change of input MODE pins.
TX_LVDS = clock must be applied to the Serializer TX interface, with desired and valid frequency.

Upon setting the above pins, the user must wait for LOCK_N = 0 on both Serializer and Deserializer.

5.2 Programming Deserializer registers

Following are the addresses for the bank of registers that can be used in pattern BIST:
Registers {0A[1:0],09[7:0]} → 1st 10 bit ordered set to be received
Registers {0C[1:0],0B[7:0]} → 2nd 10 bit ordered set to be received
Registers {0E[1:0],0D[7:0]} → 3rd 10 bit ordered set to be received
Registers {10[1:0],0F[7:0]} → 4th 10 bit ordered set to be received
Registers {12[1:0],11[7:0]} → 5th 10 bit ordered set to be received
Registers {14[1:0],13[7:0]} → 6th 10 bit ordered set to be received
Registers {16[1:0],15[7:0]} → 7th 10 bit ordered set to be received
Registers {18[1:0],17[7:0]} → 8th 10 bit ordered set to be received

Program register: 0x36 to 0x01 (enable pattern BIST)
Program register: 0x38 to 0x09 (repeat=1) or program to 0x01 (repeat=0)
When repeat is enabled, the same pattern is received over and over again.