Ethernet Debug Techniques

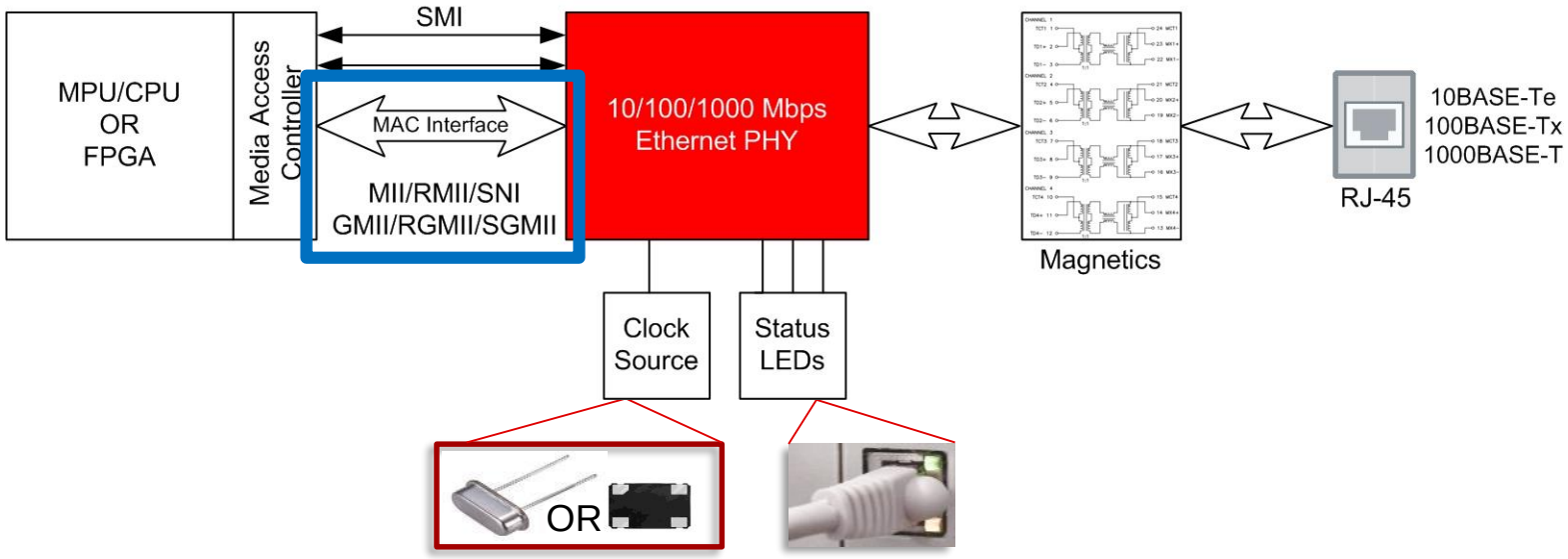
Applications Engineer

Agenda

- General PHY Configurations
- Hardware Debug Techniques
- Register Access
- Summary

General PHY Configurations

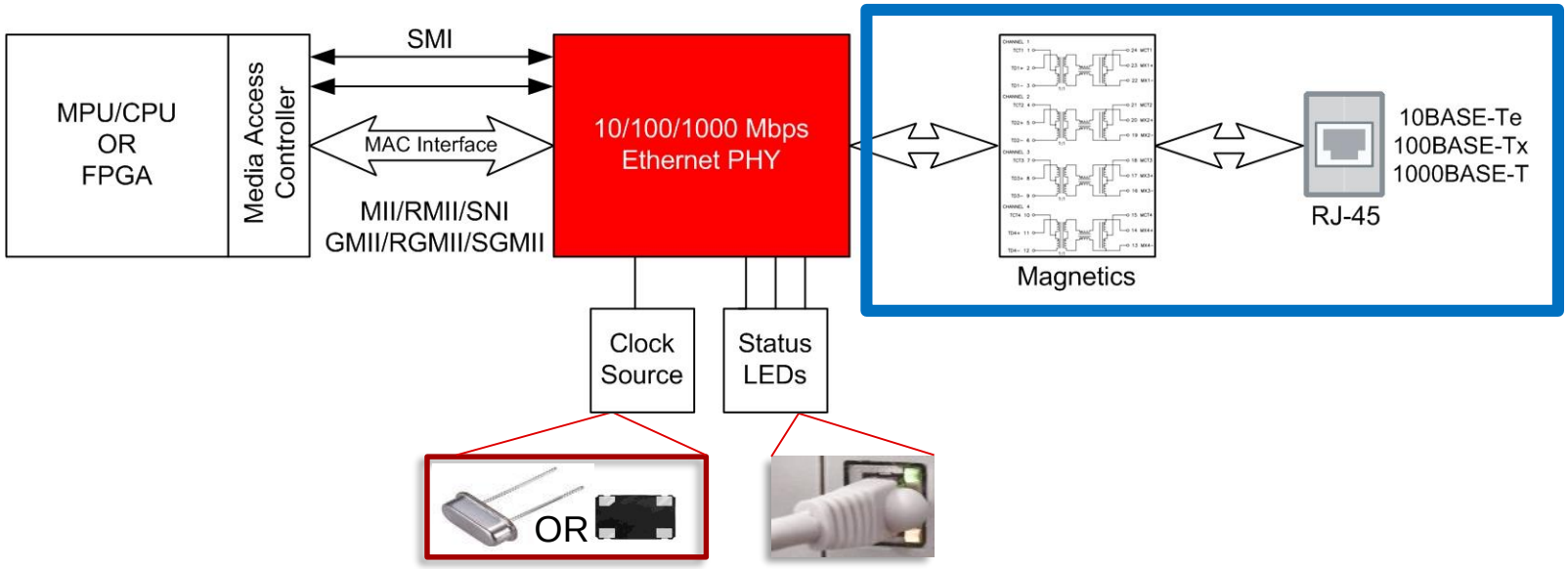
MAC Interface



MAC Interface

- Different MAC interface standards are supported by TI Ethernet PHYs
- Ethernet PHY needs to be configured for the correct MAC interface in order to achieve proper data communication with the MAC.
- MAC interface is selected based on application requirements.
- The selection is done before the board design begins.
- The PHY can be configured for the correct MAC interface option through strap or register control.

Medium Dependent Interface



Medium Dependent Interface

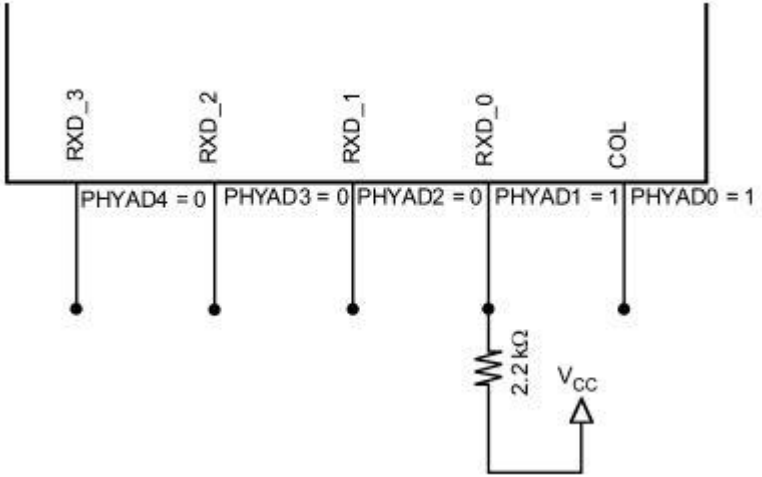
- Copper vs Fiber
  - Copper: Standard twisted pair cables, low cost, easy to replace, approx. 100m distance.
  - Fiber: Fiber cables, Fiber transceiver, Low EMI/EMC, long cable reach (in kms), high cost, high maintenance
- Speed
  - Auto-negotiate: For copper interface, PHY can auto negotiate between 10Mbps, 100Mbps, and 1000Mbps. No auto-negotiate for Fiber interface.
  - Force Mode: PHY can be force for 10M and 100M operation in Copper interface and 100M and 1000M in Fiber Interface.
  - No Force 1000M standard in copper interface.

Straps

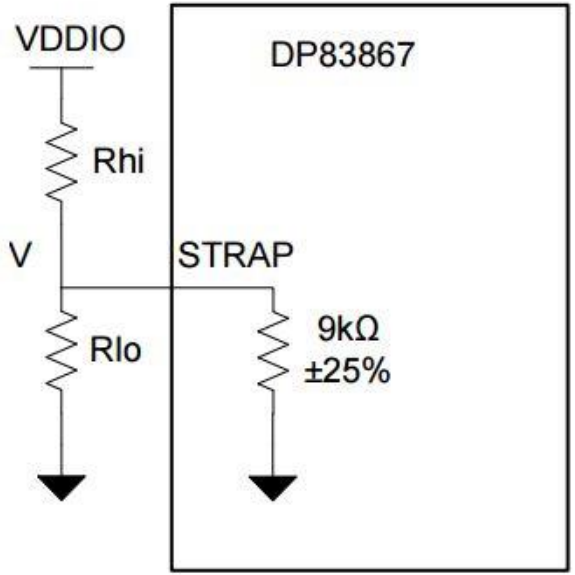
- Straps pins of the PHY are dual-functional pins.
- On Power-on or Reset, the voltage on strap pins are sampled.
- Depending on the voltage on these pins, the PHY will be configured in pre-determined functions.
- Two types of straps in TI Ethernet Portfolio devices
  - 2 level straps
  - 4 level straps
- Functions such as operating speed, Auto-MDIX, Auto-negotiation, MAC interface etc. can be controlled via straps
- Provides additional flexibility and removes needs of register writes. Faster bring up times!

2-Level vs 4-Level Straps

2-Level Straps



4-Level Straps



2-Level vs 4-Level Straps

2-Level Straps

- Relative simple, only 2 voltage levels
- One pin controls one function
- A single 2.2Kohm resistor to Vcc or GND.

4-Level Straps

- Comparatively complex, 4 voltage levels
- One pin can control 2 functions
- 2 resistor network may be needed.

Hardware Debug Techniques

Ethernet Debug Techniques

Power down the board and **verify key resistances**

1. Verify resistance to ground across the RBIAS resistor
2. Verify resistance across the transmit and receive
3. Verify resistance across the MDIO
   – Problems can occur when a very small (10's of Ohms) pull-up resistor is used.
4. Verify magnetics connections

Power up the board and **verify key voltages**

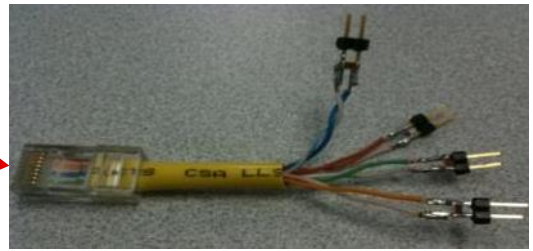
1. Probe the **Power rails**
2. Probe the **PFBOUT** and **PFBIN** pins (only for 10/100 PHYs)
   - The PFBOUT pin is a regulated 1.8V supply generated inside the device from the 3.3V supply. The device will not operate correctly if the PFBIN pins do not receive this 1.8V supply.
3. Probe the **RBIAS** pin
   - Voltage should be ~1.2V for 10/100 PHY and ~1.0V for DP83867

More information: DP83867 Troubleshooting Guide (SNLA246)

Ethernet Debug Techniques

Power up the board and **verify key signals**

1. Probe the **RESET_N** signal
   – The reset input is active low and is connected to a 10 kOhm pull down resistor. It is important to confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and will not respond.
2. Probe the **X1 clock**
   – Verify the frequency and signal integrity. For link integrity the clock needs to be within +/- 50ppm of the default (25MHz for MII / 50MHz for RMII).
3. Probe **strap pins** during initialization.
   – In some cases, other devices on the board (e.g. MAC) will pull or drive these pins unexpectedly.
4. Probe the **TD+/- transmit signals**
   – Measure the transmit voltages using a 100 Ohm terminated Pig-tail cable

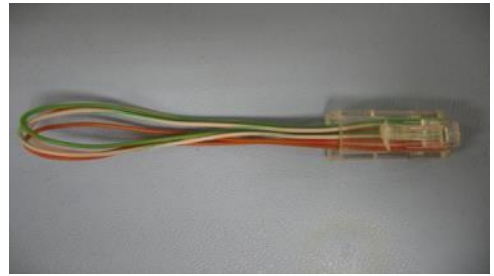


More information: DP83867 Troubleshooting Guide (SNLA246)

Ethernet Debug Techniques

Power up the board and verify link

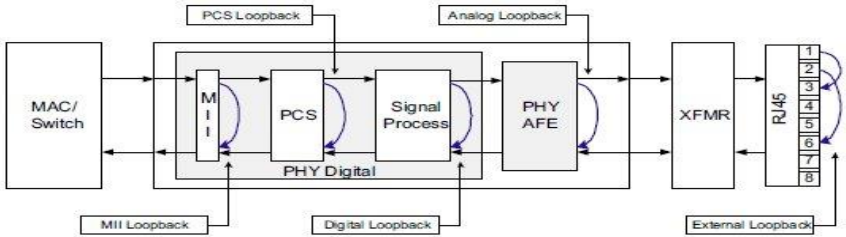
1. Verify link with known good link partner
2. For 10/100 PHYs a loopback cable can be used to verify link with itself.



Power up the board and perform packet testing

1. Packet BIST using internal loopback
2. Packet BIST using external loopback plug
3. MAC transmit and receive using internal loopback
4. MAC transmit and receive using external loopback plug
5. MAC transmit and receive with a known good partner

** Packet BIST and internal loopback are configured via register access.



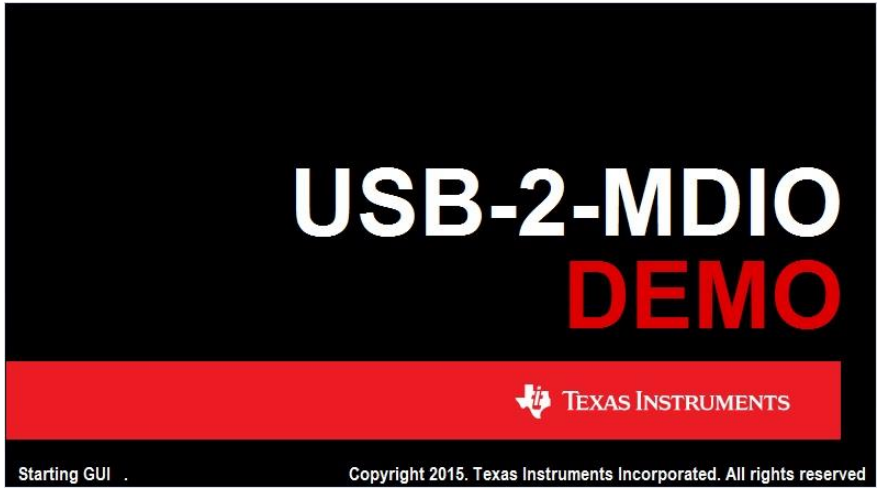
Phy loopback modes

More information: DP83867 Troubleshooting Guide (SNLA246)

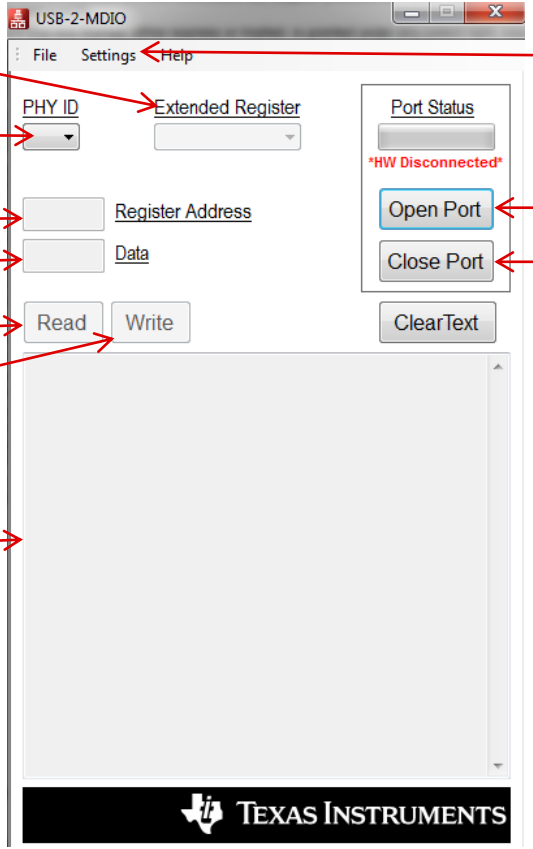
Register Access

USB2MDIO Software

- The ability to access registers of the PHY is a important debug tool and provides insight into the PHY operation
- PHY registers can be accessed through the MDIO and MDC pins.
- USB2MDIO Software uses a MSP430 Launchpad to read and write registers on TI Ethernet PHYs.
- The software can be downloaded at: http://www.ti.com/tool/usb-2-mdio
- The software comes with installation instructions and User's guide.



USB2MDIO Software



Select Extended Register Access

Set the Phy ID

Address of desired Register

Desired Data to be written

Read Command

Write Command

Text Box for displaying Register Read/Write

Select Com Port and Baud Rate

Open COM Port

Close COM Port

Register Description

- Registers serve dual purpose
  - Indicators of PHY status
  - Control functionality of the PHY
- Register tables will list the position of the bit, name, Default value, Read Only or Read Write and Bit Description.
- Using the USB2MDIO Software and Register table from Datasheets, the PHY can be configured to operate in the desired mode.

Basic Mode Status Register (BMSR)

Basic Mode Status Register (BMSR), Address 0x0001

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	100BASE-T4 Capable: 0 = Device not able to perform 100BASE-T4 mode.
14	100BASE-TX FULL DUPLEX	1, RO/P	100BASE-TX Full Duplex Capable: 1 = Device able to perform 100BASE-TX in full duplex mode.
13	100BASE-TX HALF DUPLEX	1, RO/P	100BASE-TX Half Duplex Capable: 1 = Device able to perform 100BASE-TX in half duplex mode.
12	10BASE-Te FULL DUPLEX	1, RO/P	10BASE-Te Full Duplex Capable: 1 = Device able to perform 10BASE-Te in full duplex mode.
11	10BASE-Te HALF DUPLEX	1, RO/P	10BASE-Te Half Duplex Capable: 1 = Device able to perform 10BASE-Te in half duplex mode.
10	100BASE-T2 FULL DUPLEX	0, RO/P	100BASE-T2 Full Duplex Capable: 0 = Device not able to perform 100BASE-T2 in full duplex mode.
9	100BASE-T2 HALF DUPLEX	0, RO/P	100BASE-T2 Half Duplex Capable: 0 = Device not able to perform 100BASE-T2 in half duplex mode.
8	EXTENDED STATUS	1, RO/P	1000BASE-T Extended Status Register: 1 = Device supports Extended Status Register 0x0F.
7	RESERVED	0, RO	RESERVED: Write as 0, read as 0.
6	MF PREAMBLE SUPPRESSION	1, RO/P	Preamble Suppression Capable: 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Normal management operation.
5	AUTO-NEGOTIATION COMPLETE	0, RO	Auto-Negotiation Complete: 1 = Auto-Negotiation process complete. 0 = Auto-Negotiation process not complete.
4	REMOTE FAULT	0, RO/LH	Remote Fault: 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	AUTO-NEGOTIATION ABILITY	1, RO/P	Auto Negotiation Ability: 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	LINK STATUS	0, RO/LL	Link Status: 1 = Valid link established. 0 = Link not established. The criteria for link validity is implementation specific. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read via the management interface.

Register reference for DP83867

Important Registers

- Following are some of the common registers which are important for configuration and status check:
  - Basic Mode Control Register (BMCR) Register Address 0x00h
  - Basic Mode Status Register (BMSR) Register Address 0x01h
  - Auto-Negotiation Advertisement Register (ANAR) Register Address 0x04h
  - Auto-Negotiation Link Partner Ability Register (ANLPAR) Register Address 0x05h
  - PHY Status Register (PHYSTS) Register Address 0x10h
- There will be other important registers specific to the device.
- Refer to respective datasheet for more information on registers.

Summary

- MAC IF and MDI configurations are decided before board development.
- The PHY should be configured accordingly via straps or registers.
- Hardware Level Debug
  - Schematic and Layout check
  - Verify key components
  - Verify key voltages
  - Verify Clock In, Clock Out, and MDI signals
  - Loopback testing
- Software Level Debug
  - Use TI software or application specific driver to access registers.
  - Verify register configuration matches the system requirements.

Thank You!