F75910

2-bit Bidirectional SMBus/I^{2}C Level Shifter

Jan, 2018
V0.20P

F75910 Datasheet Revision History

Version	Date	Revision History
Data Brief	2012/04	• Data Brief
V0.11P	2012/04	• Add AC/DC SPECs
V0.12P	2012/05	• High Side Output I/O SPEC correction
V0.13P	2013/07	• Update Application Circuit
V0.14P	2013/10	• Made Clarification and Correction • Added Timing Requirements Chapter
V0.15P	2014/03	• Made Clarification and Correction • Update Top Marking Specification
V0.16P	2014/06	• Made clarification and correction • In section 6.4, update dynamic characteristics • In section 10, update typical application circuit
V0.17P	2015/03	• Made clarification and correction • In section 6.4, add clock rate
V0.18P	2015/06	• Made clarification and correction • Add section 6
V0.19P	2017/03	• Made clarification and correction • Modify Dynamic Characteristics
V0.20P	Jan, 2018	• Made clarification and correction • Modify Principle and Operation Section

Table of Contents

1 General Description

The F75910 is an I²C-bus/SMBus voltage level shifter with enable (EN) input. Suitable for the application of I²C embedded in DVI / VGA interface, which is attached with long cable. The open-drain design of F75910 can help the environment with huge inductance like DVI / VGA interface to avoid I²C signal reflecting phenomenon.

The F75910 is operational from 1.1 V to [$V_{CC(H)}$ -1.0 V] on L-Port and 2.5 V to 5.5 V on H-port. The Enable (EN) input is referenced to $V_{CC(L)}$ with 5V tolerant. When F75910 is disabled, both port L and port H I/O pins became high-impedance.

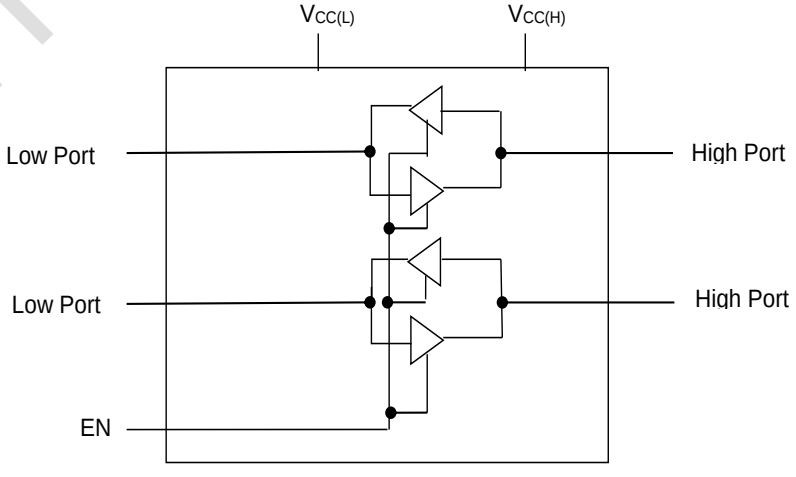
The bus port H are compliant with any digital signals, the standard I²C-bus or SMBus I/O levels, while port L uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. This results in a LOW on the port L accommodating smaller voltage swings. The output pull-down on the port L internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port L I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port H drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables port H to connect to any other I²C-bus devices or buffer.

The F75910 is not enabled unless $V_{CC(L)}$ is above 0.8 V and $V_{CC(H)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

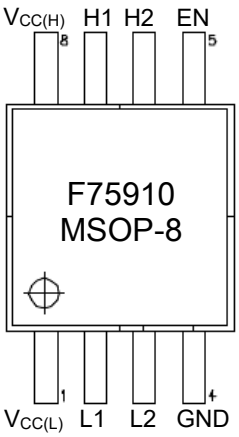
2 Feature

- Voltage level shifting from L-Port: 1.1V to ($V_{CC(H)}$ -1.0V)
- Voltage level shifting from H-Port: 2.5V to 5.5V
- Max data rates
  - 2 Mbps (Open Drain)
- High impedance bus pin when Power-off
- Open-drain I/O on high-side
- EN input circuit referenced to $V_{CC(L)}$
- 8-pin MSOP Green Package

3 Block Diagram



4 Pin Configuration



Pin Configuration of F75910

5 Pin Description

IN - input pin with schmitt trigger.
Analog - Analog I/O
P -Power.
GND -Ground

Pin No.	Pin Name	Type	Description
1	$V_{CC(L)}$	P	Port L power supply
2	L1	Analog	Input/output port L1 (lower voltage side)
3	L2	Analog	Input/output port L2 (lower voltage side)
4	GND	GND	Ground
5	EN	IN	Enable input (high active)
6	H2	Analog	Input/output port H2 (higher voltage side)
7	H1	Analog	Input/output port H2 (higher voltage side)
8	$V_{CC(H)}$	P	Port H power supply

6 Principles and Operation

6.1 Power Up

During operation, ensure that $V_{CCL} \leq V_{CCH}$ at all times. During power-up sequencing, V_{CCH} comes early than V_{CCL} will generate a leakage current from V_{CCH} to low side channel, so power supply of V_{CCH} should be ramped up first. The F75910 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCL/H}$ = 0 V or $V_{CCH/L}$ = 0 V).

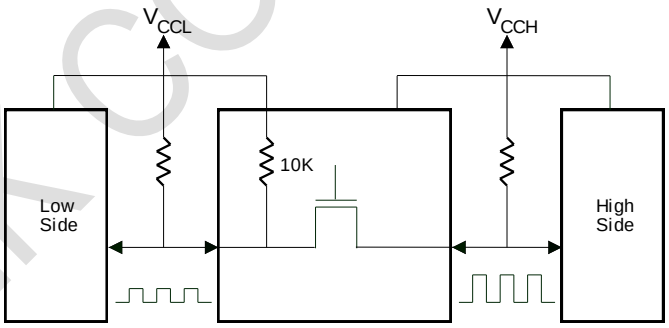
6.2 Enable and Disable

The F75910 has an EN input that is used to disable the device by setting EN = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when EN goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after EN is taken high.

6.3 Pullup and Pulldown Resistors on I/O Lines

Each L-port I/O has an internal 10-kΩ pullup resistor to V_{CCL}.

Check below for the functional block:

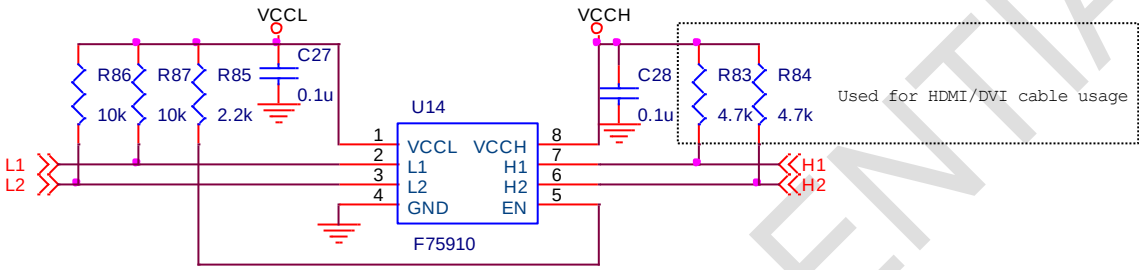


* Required power sequence $V_{CCL} \geqq V_{CCH}$

Internal Resistance Ω	Low Side Pull Up	10K
	Low Side Pull Down	-
	High Side Pull Up	-
	High Side Pull Down	-

6.4 I2C/SMBus/Open Drain systems

As with the standard I²C bus or SMBus system, the pull up resistors are required to provide the logic high levels on the buffered bus. The value of these pull up resistors are depended on the system. Based on the built in different resistors value of I²C HDMI/DVI devices, it's recommended to use the pull up resistors 4.7KΩ (typically) to V_{CCH} at the high side I/O pins.



7 Electrical Characteristics

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(H)}$	Supply voltage port High side range		-0.5	+5.5	V
$V_{CC(L)}$	Supply voltage port Low side range		-0.5	+5.5	V
$V_{I/O}$	Input/output voltage range	Port low side, enable pin (EN)	-0.5	+3.6	V
		Port high side	-0.5	+5.5	V
I_O	Continuous output current			16	mA
T_{stg}	Storage temperature range		-55	145	°C
T_{amb}	Ambient temperature (Design Guarantee)	Operating in the free air	-40	85	°C

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Static Characteristics

Typical values with $V_{CC(L)}$ = 1.1V, $V_{CC(H)}$ = 3.3V
GND = 0V; T_{amb} = -40°C to +85°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(H)}$	Supply voltage port High side		2.5		5.5	V
$V_{CC(L)}$	Supply voltage port Low side		1.1		$(V_{CC(H)}-1)\leqq 3.6$	V
$I_{CC(L)}$	Supply current port Low side	All port low side static High		0		mA
		All port low side static Low		0		mA
$I_{CC(H)}$	Supply current port High side	All port High side static High		0.25		mA

Input and output of port Low side (L1, L2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	Port Low side	0.7 $Vcc_{(L)}$		$Vcc_{(L)}$	V
V_{IL}	Low-level input voltage	Port Low side	-0.5		+0.3 $Vcc_{(L)}$	V
I_{IH}	Input leakage current	$V_I=Vcc_{(L)}$			1	uA
I_{LOH}	output High leakage current	V_O=1.1V			15	uA
C_{iO}	Input/output capacitance			5		pF

Input and output of port High side (H1, H2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	Port H	0.7 $Vcc_{(H)}$		5.5	V
V_{IL}	Low-level input voltage	Port H	-0.5		+0.3 $Vcc_{(H)}$	V
I_{IH}	Input leakage current	V_I=3.6V			1	uA
I_{IL}	Low-level input current	V_I=0.2V			1	uA
I_{LOH}	Output High leakage current	V_O=3.6V			120	uA
C_{iO}	Input/output capacitance			5		pF

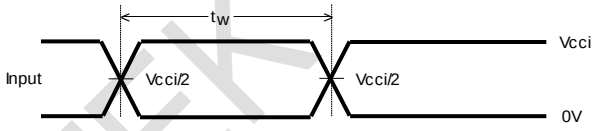
Enable

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		0.7 $Vcc_{(L)}$		$Vcc_{(L)}$	V
V_{IL}	Low-level input voltage		-0.5		+0.3 $Vcc_{(L)}$	V
I_{IH}	High-level input current				1	uA
I_{IL}	Low-level input current				1	uA
C_i	Input capacitance	V_I=3.6V or 0V		4		pF

7.3 Timing Requirements

over recommended operating free-air temperature range, **$V_{CC(L)}$ = 1.2V ± 0.05V**, **1.8V ± 0.15V, 3.3V ± 0.3V** (unless otherwise noted)

			$V_{CC(H)}$ = 2.5V		$V_{CC(H)}$ = 3.3V		$V_{CC(H)}$ = 5.0V		Unit
			Min	Max	Min	Max	Min	Max	
	Data rate			2		2		2	Mbps
t_w	Pulse duration	Data inputs	500		500		500		ns



Vcci is the Vcc associated with the input port.

Figure. Voltage Waveforms Pulse Duration

7.4 Dynamic Characteristics

over recommended operating free-air temperature range, **$V_{CC(L)}$ = 1.8V; $V_{CC(H)}$ = 3.3V** (unless otherwise noted)

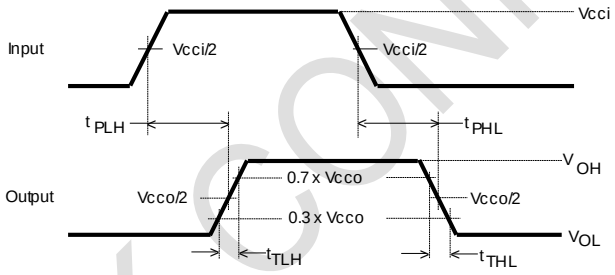
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Low to High propagation delay	Port H to port L(1)	1.5	2.8	4.3	ns
t_{PHL}	High to Low propagation delay		3.8	7.5	12	
t_{PLH}	Low to High propagation delay	Port L to port H(1)	41	80	121	ns
t_{PHL}	High to Low propagation delay		1.6	3.0	4.6	
t_{TLH}	Low to High output transition time	Port L(1)	4.6	9.0	14	ns
t_{THL}	High to Low output transition time		4.6	9.0	14	
t_{TLH}	Low to High output transition time	Port H(1)	121(2)	240(2)	361(2)	ns
t_{THL}	High to Low output transition time		6.5	12	18.5	
t_{en}	Enable time	EN high before enable condition	1.6	3.0	4.6	ns
t_{dis}	Disable time	En low after disable condition	1.6	3.0	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew		-0.8	0	0.8	ns
Max data rate					2	Mbps
Max clock rate					1(3)	MHz

(1) Max Load capacitance = 30 pF; load resistance on port H =10 kΩ.
(2) Value is determined by RC time constant of bus line.
(3) Duty cycle = 50%

over recommended operating free-air temperature range, **Vcc(L) = 1.8V; VCC(H) = 5.0V** (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Low to High propagation delay	Port H to port L(1)	1.2	2.2	3.4	ns
t_{PHL}	High to Low propagation delay		3.1	6.0	9.1	
t_{PLH}	Low to High propagation delay	Port L to port H(1)	41	80	121	ns
t_{PHL}	High to Low propagation delay		1.6	3.0	4.6	
t_{TLH}	Low to High output transition time	Port L(1)	4.1	8.0	12.1	ns
t_{THL}	High to Low output transition time		4.1	8.0	12.1	
t_{TLH}	Low to High output transition time	Port H(1)	121(2)	240(2)	361(2)	ns
t_{THL}	High to Low output transition time		5.1	10	15.1	
t_{en}	Enable time	EN high before enable condition	1.6	3.0	4.6	ns
t_{dis}	Disable time	En low after disable condition	1.6	3.0	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew		-0.8	0	0.8	ns
Max data rate					2	Mbps
Max clock rate					1(3)	MHz

(1) Max Load capacitance = 30 pF; load resistance on port H =10 kΩ.
(2) Value is determined by RC time constant of bus line.
(3) Duty cycle = 50%



A. Vcci is the Vcc associated with the input port.
B. Vcco is the Vcc associated with the output port.

Figure. Voltage Waveforms Propagation Delay times

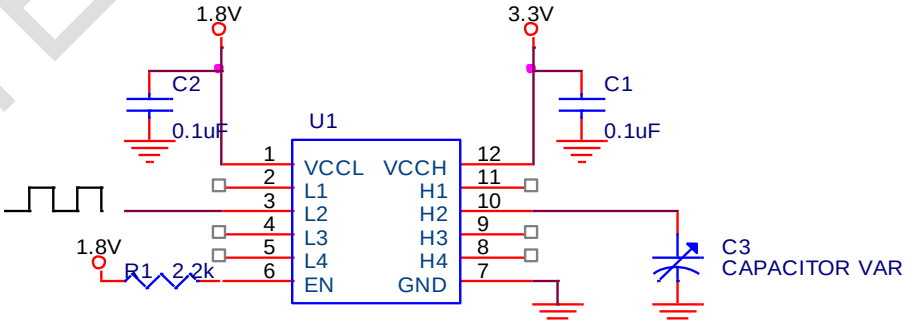


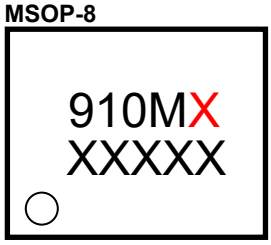
Figure. Simulated Load Capacitance Circuit

8 Ordering Information

Part Number	Package Type
F75910M	MSOP-8

9 Top Marking Specification

MSOP-8



1st Line: Device Name + **IC Version (X)** where where A means version A, B means version B, …package.

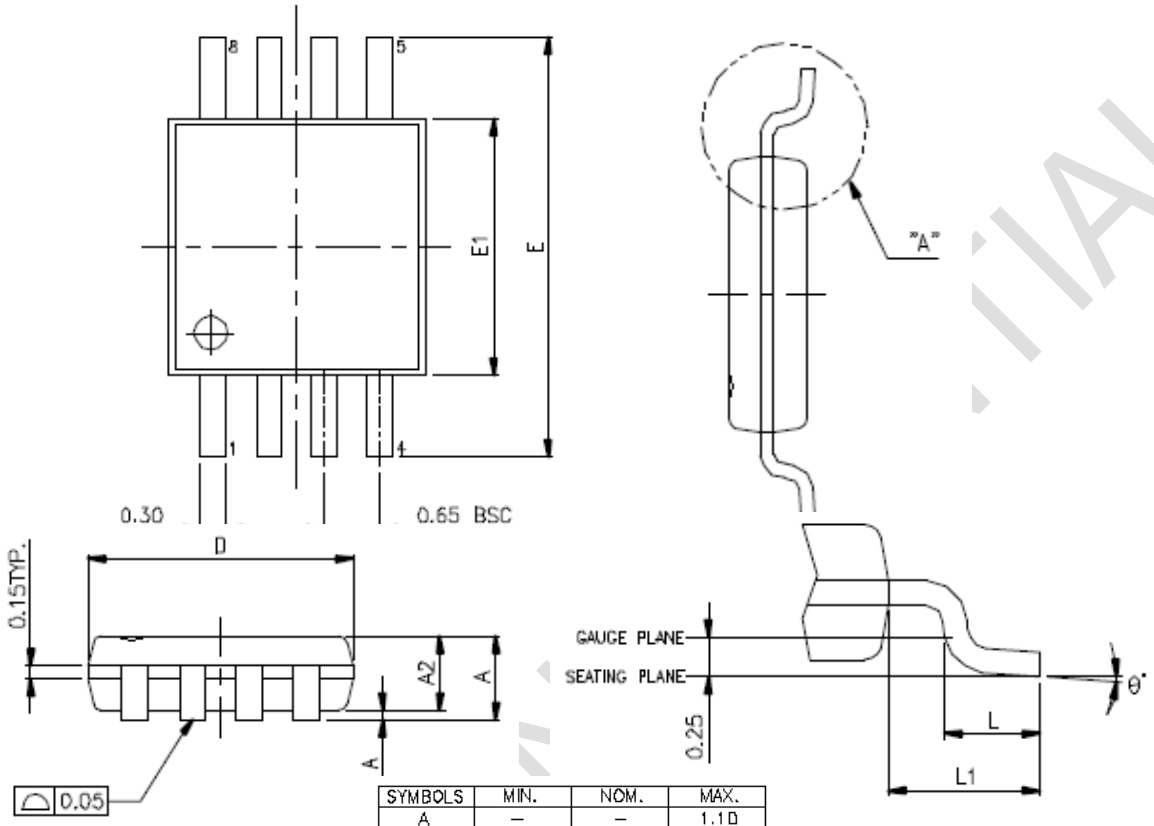
2nd Line: Trace Code (XXXXX)

◯ : Pin 1 Identifier

The version identification is shown as the bold red characters.

10 Package Dimension

MSOP-8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

NOTES:
1. JEDEC OUTLINE : MO-187 AA
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "0.22" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "0.22" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE ⊞ .

11 Typical Application Circuit