F81214E

eSPI/LPC to 2 UART

Release Date: May, 2020
Version: V0.12P

F81214E Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	May, 2018	-	Preliminary Version
V0.11P	Dec, 2019	-	Made Modification & Clarification Update Ordering Information Update Top Marking Specification Update Feature List Update General Description
V0.12P	May, 2020	-	Made Modification & Clarification Modify Package Dimension (Delete VWQFN only) Modify 9-bit Mode Broadcast Address Register -- Index FFh

Table of Content

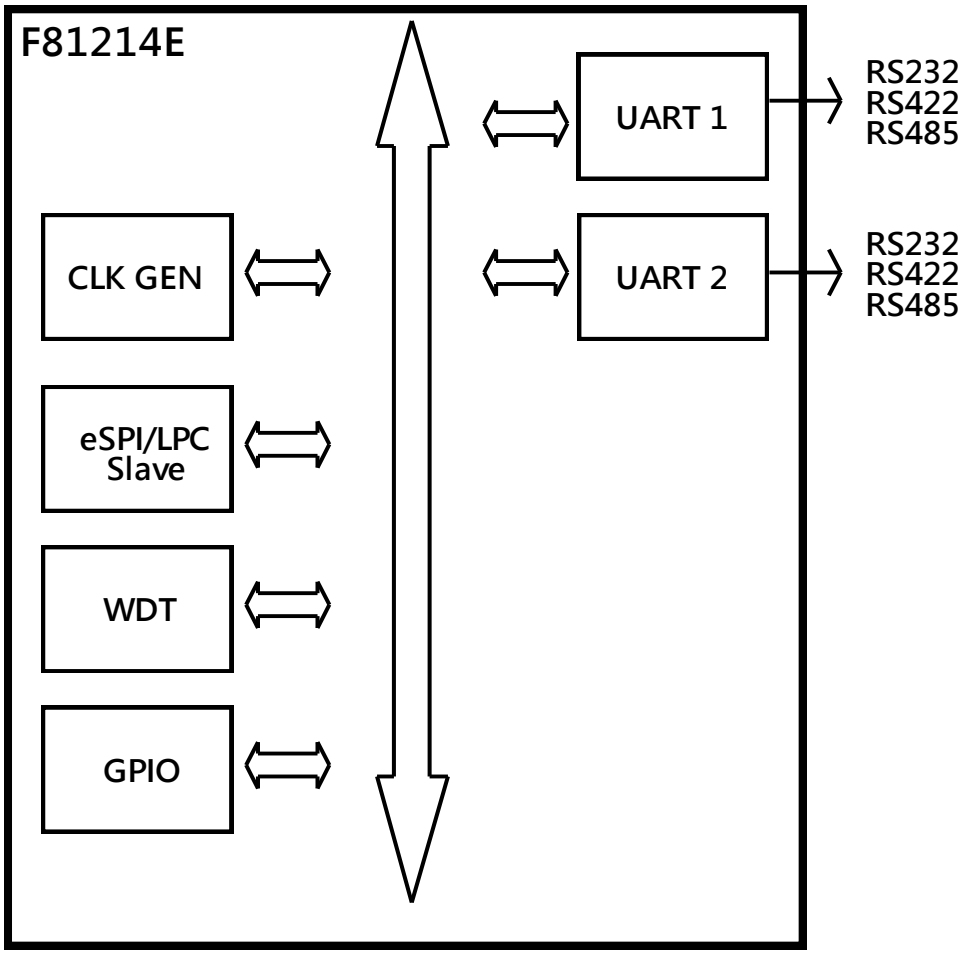
1 General Description

The F81214E mainly provides 2 pure UART ports through LPC/eSPI interface (Auto detection and powered by IFP 1.8V/3.3V). Each UART includes 128-byte transmitter/receiver FIFO, a programmable baud rate generator, complete modem control capability, auto flow control, RX/TX LED and an interrupt system. 14 GPIO pins and a watch dog timer is provided for system controlling and the time interval can be programmed by register or hardware power on setting pin. The F81214E is in the small 28 pin QFN package (4mm x 4mm).

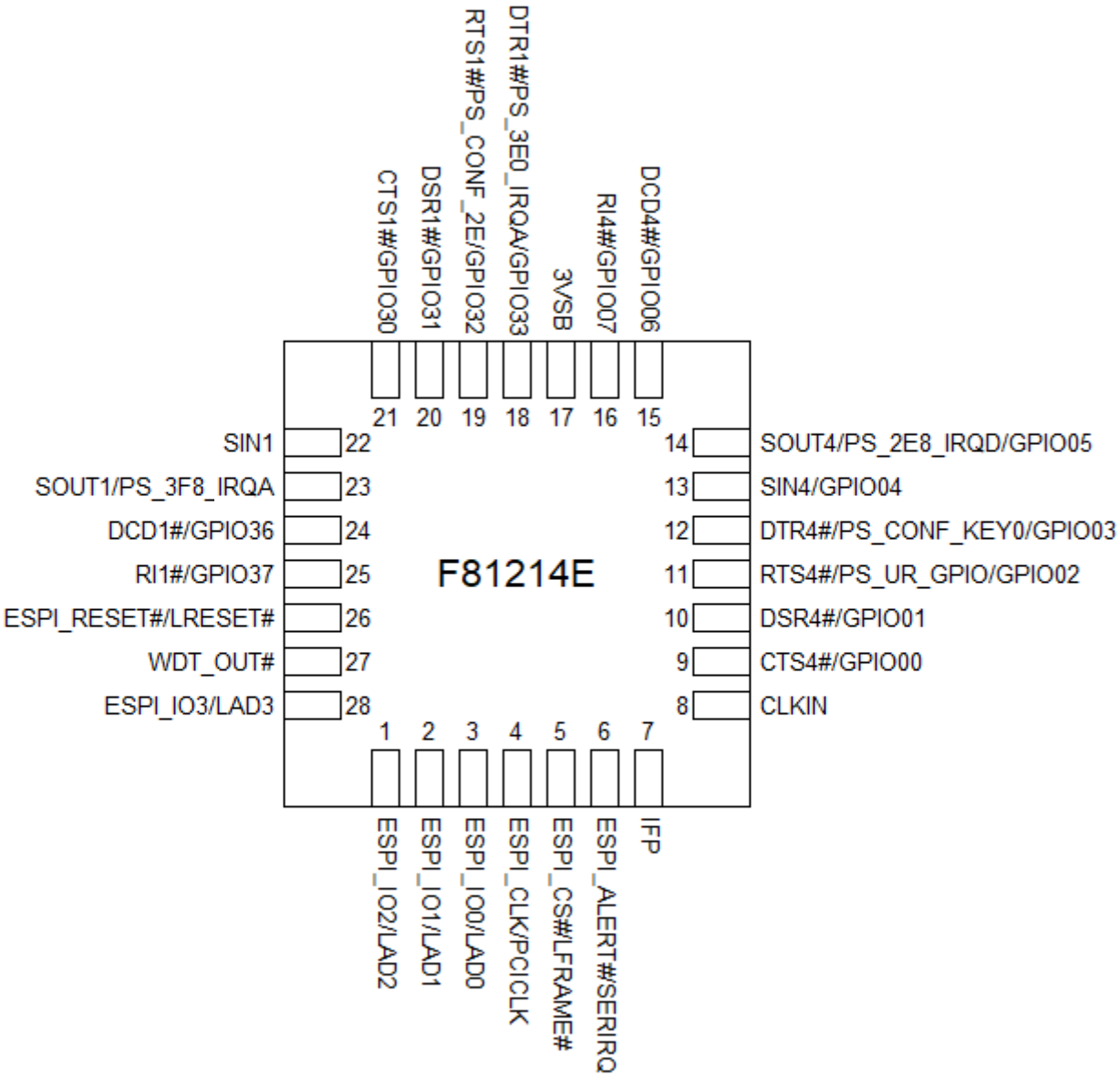
2 Feature List

- Supports LPC/eSPI auto detection interface
- Fully compatible with industry standard 16C550/16C650/16C750/16C850/16C950type UARTs
- 128/64/32/16 Bytes Transmitter/ReceiverFIFO
- LED status indication for UART TX/RX
- Auto flow control
- 1 watch dog timer with WDT_OUT# signal
- Support 9-bit protocol
- 14 pins GPIO
- 24/48MHz or programmable Clock input
- UART clock source derived by PCICLK
- F81214E package in 28-QFN (4mm*4mm)
- Operating temperature range -40°C ~ 85°C

3 Block Diagram



4 Pin Configuration



5 Pin Description

$IO_{16st,\ lv}$	Low input level bi-directional pin with 16 mA drive/sink capability
$I/OOD_{8st,5v}$	TTL level bi-directional pin and schmitttriggrt, Open-drain output with 8mA source-sink capability, 5V tolerance.
$I/O_{8t,5V,u47k}$	TTL level and schmitt trigger bi-directional pin with 8mA source-sink capability, 5V tolerance. Internla pull-up 47K during 3VCC power on.
$OD_{12,5V}$	Open-drain output pin with sink capability of 12 mA, 5V tolerance
$IN_{st,\ lv}$	Low level input pin with schmitt trigger
$IN_{st,\ 5v}$	TTL level input pin with schmitt trigger, 5v tolerance
P	Power

5.1. Power Pin

Pins	Pin Name	Type	Description
EP	GND	P	Ground.
7	IFP	P	Interface 1.8V/3.3V power supply voltage input for LPC Interface 1.8V power supply voltage input for eSPI
17	3VSB	P	Core Power. For eSPI platform it should be 3VSB; for LPC platform, it could be 3VSB or 3VCC. (If 3VSB is connected to this pin, WDT_OUT# should pull-up to 3VCC for 3VCC detection.)

5.2. eSPI Interface

Pins	Pin Name	Type	PWR	Description
28	ESPI_IO3	$I/O_{16st,lv}$	IFP	eSPI I/O: Bidirectional input/output pins used to transfer data between master & slaves.
1	ESPI_IO2	$I/O_{16st,lv}$	IFP	eSPI I/O: Bidirectional input/output pins used to transfer data between master & slaves.
2	ESPI_IO1	$I/O_{16st,lv}$	IFP	eSPI I/O: Bidirectional input/output pins used to transfer data between master & slaves.
3	ESPI_IO0	$I/O_{16st,lv}$	IFP	eSPI I/O: Bidirectional input/output pins used to transfer data between master & slaves.
4	ESPI_CLK	$IN_{st,lv}$	IFP	eSPI clock input. The reference timing for all the serial input & output operations.
5	ESPI_CS#	$IN_{st,lv}$	IFP	eSPIChip select#: driving chip select low selects a particular eSPI slave for the transaction.
6	ESPI_ALERT#	$I/O_{16st,lv}$	IFP	eSPI Alert#: Used by eSPI slave to request service from eSPI master. This pin is optional for single master single slave configuration where I/O [1] can be used to signal the Alert event.

26	ESPI_RESET#	$IN_{st,lv}$	IFP	eSPI Reset signal. Reset the eSPI interface for both master & slaves.

5.3. Clock

Pins	Pin Name	Type	PWR	Description
4	PCICLK	$IN_{st,lv}$	IFP	PCI clock 10M Hz~33M Hz input.
8	CLKIN	$IN_{st,5V}$	3VSB	Clock Input (24/48MHz)

5.4. LPC Interface

Pins	Pin Name	Type	PWR	Description
28	LAD3	$I/O_{16st,lv}$	IFP	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
1	LAD2	$I/O_{16st,lv}$	IFP	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
2	LAD1	$I/O_{16st,lv}$	IFP	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
3	LAD0	$I/O_{16st,lv}$	IFP	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
5	LFRAME#	$IN_{st,lv}$	IFP	Indicates start of a new cycle or termination of a broken cycle.
6	SERIRQ	I/O_{16st}	IFP	LPC Serial IRQ input / Output
26	LRESET#	$IN_{st,lv}$	IFP	LPC Reset Signal. It can connect to PCIRST# signal on the host.

5.5. UART

Pins	Pin Name	Type	PWR	Description
9	CTS4#	$IN_{st,5V}$	3VSB	Clear To Send is the modem control input.
10	DSR4#	$IN_{st,5V}$	3VSB	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
11	RTS4#	$I/O_{8t,5V,u47k}$	3VSB	UART 4 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
12	DTR4#	$I/O_{8t,5V,u47k}$	3VSB	UART 4 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
13	SIN4	$IN_{st,5V}$	3VSB	Serial Input. Used to receive serial data through the communication link.
14	SOUT4	$I/O_{8t,5V,u47k}$	3VSB	UART 4 Serial Output. Used to transmit serial data out to the

				communication link.
15	DCD4#	$IN_{st,5V}$	3VSB	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
16	RI4#	$IN_{st,5V}$	3VSB	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
18	DTR1#	$I/O_{8t,5V,u47k}$	3VSB	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
19	RTS1#	$I/O_{8t,5V,u47k}$	3VSB	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
20	DSR1#	$IN_{st,5V}$	3VSB	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
21	CTS1#	$IN_{st,5V}$	3VSB	Clear To Send is the modem control input.
22	SIN1	$IN_{st,5V}$	3VSB	Serial Input. Used to receive serial data through the communication link.
23	SOUT1	$I/O_{8t,5V,u47k}$	3VSB	UART 1 Serial Output. Used to transmit serial data out to the communication link.
24	DCD1#	$IN_{st,5V}$	3VSB	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
25	RI1#	$IN_{st,5V}$	3VSB	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

5.6. Configuration Straps & WDT

Pins	Pin Name	Type	PWR	Description
11	PS_UR_GPIO	$I/O_{8t,5V,u47k}$	3VSB	Power setting pin to define the UART1~4 pin function. (Internal pull up 47KΩ) PS_UR_GPIO = 0: Function as GPIO. PS_UR_GPIO = 1 (Default): Function as UART.
12	PS_CONF_KEY0	$I/O_{8t,5V,u47k}$	3VSB	Power on configuration setting pin. As for detail description, please refer to register description. Internal pull up 47KΩ.
14	PS_2E8_IRQD	$I/O_{8t,5V,u47k}$	3VSB	Power setting pin to define the UART4 base address and IRQ channel. (Internal pull up 47KΩ) PS_2E8_IRQD = 0: Base address is 0x0000, IRQ channel is 0x0 and IO decode disable. PS_2E8_IRQD = 1 (Default): UART4 base address is 0x02E8,

				IRQ channel is 0x9 and IO decode enable.
18	PS_3E0_IRQA	$I/O_{8t,5V,u47k}$	3VSB	Power setting pin to define the UART1 base address and IRQ channel. (Internal pull up 47KΩ) This trap pin only has effect when PS_3F8_IRQA is 0. PS_3E0_IRQA = 0: Base address is 0x0000, IRQ channel is 0x0 and IO decode disable. PS_3E0_IRQA = 1 (Default): UART2 base address is 0x03E0, IRQ channel is 0x3 and IO decode enable.
19	PS_CONF_2E	$I/O_{8t,5V,u47k}$	3VSB	Power on configuration setting (Internal pull up 47KΩ). PS_CONF_2E = 0, setting the configuration to 0x4E. If PS_CONF_2E =1 (Default), setting the configuration to 0x2E.
23	PS_3F8_IRQA	$I/O_{8t,5V,u47k}$	3VSB	Power setting pin to define the UART1 base address and IRQ channel. (Internal pull up 47KΩ) PS_3F8_IRQA = 0: Setting depends on PS_3E0_IRQA PS_3E0_IRQA = 1 (Default): UART1 base address is 0x03F8, IRQ channel is 0x3 and IO decode enable.
27	WDT_OUT#	$OD_{12,5V}$	IFP	Watch dog timer output. When pin 24 power on setting PS_WDT=0, Watch Dog timer time interval setting is programmed by register. Once power on setting PS_WDT=1 (Default), watch dog timer time interval will be fixed to 10 sec. This pin should external pull-up to 3VCC for 3VCC power good detection. ※Please contact Fintek for the special usage.

5.7. General-Purpose I/O

Pins	Pin Name	Type	PWR	Description
9	GPIO00	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
10	GPIO01	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
11	GPIO02	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
12	GPIO03	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
13	GPIO04	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
14	GPIO05	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
15	GPIO06	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
16	GPIO07	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
21	GPIO30	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.
20	GPIO31	$I/OOD_{8st,\ 5v}$	3VSB	General Purpose IO.

19	GPIO32	I/OOD$_{8st, 5v}$	3VSB	General Purpose IO.
18	GPIO33	I/OOD$_{8st, 5v}$	3VSB	General Purpose IO.
24	GPIO36	I/OOD$_{8st, 5v}$	3VSB	General Purpose IO.
25	GPIO37	I/OOD$_{8st, 5v}$	3VSB	General Purpose IO.

6 Functional Description

6.1 Power on Strapping Option

The F81214E provides eight pins for power on hardware strapping to select functions. See below table for detail:

Table1. Power on trap configuration

Pin No.	Symbol	Value	Description
11	PS_UR_GPIO	1	UART1, UART4 pins default function as UART.
		0	UART1, UART4 pins default function as GPIO.
12	PS_CONF_KEY0	0	Entry key is 0x87.
		1	Entry key is 0x67.
14	PS_2E8_IRQD	1	1. UART 4 default base address is 0x2E8. 2. UART 4 default IRQ channel is 0x9. 3. UART 4 default enable.
		0	1. UART 4 default base address is 0x0. 2. UART 4 default IRQ channel is 0x0. 3. UART 4 default disable.
19	PS_CONF_2E	1	Configuration Register I/O port is 0x2E. (Default, data port is 0x2F)
		0	Configuration Register I/O port is 0x4E (data port is 0x4F).
18 23	PS_3E0_IRQA PS_3F8_IRQA	11	1. UART 1 default base address is 0x3F8. 2. UART 1 default IRQ channel is 0x3. 3. UART 1 default enable.
		10	1. UART 1 default base address is 0x3E0. 2. UART 1 default IRQ channel is 0x3. 3. UART 1 default enable.
		01	1. UART 1 default base address is 0x3F8. 2. UART 1 default IRQ channel is 0x3. 3. UART 1 default enable.
		00	1. UART 1 default base address is 0x0. 2. UART 1 default IRQ channel is 0x0. 3. UART 1 default disable.

The power on strap value is latched at the rising edge of 3VCC power good (2.8V) which is detected by WDT_OUT# pin. Or latched at the rising edge of ESPI_RESET/LRESET# pin. The later could be disabled by register.

6.2 LPC Interface

The F81214E can support LPC interface serving as a bus interface between host (chipset) and peripheral (I/O chip) by hardware trapping. This interface provides much less pins and more efficient transmission. Data transfer on the LPC bus is serialized over a 4 bit bus. The general characteristics of the interface implemented in F81214E are listed as below:

- One control line, namely LFRAME#, which is used by the host to start or stop transfers. No peripherals drive this signal.
- The LAD[3:0] bus, which communicates information serially. The information conveyed is cycle type, cycle direction, chip selection, address, data, and wait states.
- PCIRST# is an active low reset signal.
- An additional 33 MHz PCI clock is needed in the F81214E for synchronization.
- Interrupt requests are issued through SERIRQ.

6.3 UART

The F81214E provides up to 2 UART ports and support IRQ sharing for system application. They are compatible with 16C550/16C650/16C750/16C850 and 16C950.The UARTs are used to convert data between parallel format and serial format. They convert parallel data into serial format on transmission and serial format into parallel data on receiver side. The serial format is formed by one start bit, followed by five to eight data bits, a parity bit if programmed and one (1.5 or 2) stop bits. The UARTs include complete modem control capability and an interrupt system that may be software trailed to the computing time required to handle the communication link. They have FIFO mode to reduce the number of interrupts presented to the host. Both receiver and transmitter have a 128-byte FIFO. The UART control register control & define the asynchronous protocol data communications including data length, stop bit, parity & baud rate selection. The below content is about the UARTs device register descriptions. All the registers are for software porting reference.

6.3.1 UART Port Register

Receiver Buffer Register – Base + 0

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	RBR[7:0]	R	The data received. Read only when LCR [7] is 0

Transmitter Holding Register – Base + 0

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	THR[7:0]	W	Data to be transmitted. Write only when LCR [7] is 0

Divisor Latch (LS) – Base + 0

Power-on default [7:0] = 0x01h.

Bit	Name	R/W	Description
7:0	DLL[7:0]	R/W	Baud generator divisor low byte.Access only when LCR [7] is 1.

Divisor Latch (MS) – Base + 1

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	DLM[7:0]	R/W	Baud generator divisor high byte. Access only when LCR [7] is 1.

Interrupt Enable Register – Base + 1

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:5	Reserved	R/W	Return 0 when read. Access only when LCR[7] is 0
4	SM2	R/WC	This bit is used only in 9-bit mode and always returns “0” when 9-bit mode is disabled. 0: The receiver could receive data byte. 1: The receiver could only receive address byte and issue an interrupt when the address is received.
3	EDSSI	R/W	Enable Modem Status Interrupt. Access only when LCR [7] is 0.
2	ELSI	R/W	Enable Line Status Error Interrupt. Access only when LCR [7] is 0.
1	ETBFI	R/W	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR [7] is 0.
0	ERBFI	R/W	Enable Received Data Available Interrupt. Access only when LCR [7] is 0

Interrupt Identification Register – Base + 2

Power-on default [7:0] = 0x01h.

Bit	Name	R/W	Description
7	FIFO_EN	R	0 : FIFO is disabled 1 : FIFO is enabled.
6	FIFO_EN	R	0 : FIFO is disabled. 1 : FIFO is enabled.

5:4	Reserved	R	Return 0 when read.
3:1	IRQ_ID[2:0]	R	000 : Interrupt is caused by Modem Status 001 : Interrupt is caused by Transmitter Holding Register Empty 010 : Interrupt is caused by Received Data Available. 110 : Interrupt is caused by Character Timeout 011 : Interrupt is caused by Line Status.
0	IRQ_PENDN	R	1 : Interrupt is not pending. 0 : Interrupt is pending.

FIFO Control Register – Base + 2

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:6	RCVR_TRIG[1:0]	W	00 : Receiver FIFO trigger level is 1. 01 : Receiver FIFO trigger level is 4. 10 : Receiver FIFO trigger level is 8. 11 : Receiver FIFO trigger level is 14.
5:3	Reserved	W	Reserved
2	CLRTX	W	1 : Reset the transmitter FIFO.
1	CLRRX	W	1 : Reset the receiver FIFO.
0	FIFO_EN	W	0 : Disable FIFO 1 : Enable FIFO

Line Control Register – Base + 3

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7	DLAB	R/W	0 : Divisor Latch can't be accessed. 1 : Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	1 : Transmit a break condition. 0 : Transmitter is in normal condition.
5:3	STKPAR EPS PEN	R/W	XX0 : Parity Bit is disable 001 : Parity Bit is odd. 011 : Parity Bit is even 101 : Parity Bit is logic 1 111 : Parity Bit is logic 0
2	STB	R/W	0 : Stop bit is one bit 1 : When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit

1:0	WLS[1:0]	R/W	00 : Word length is 5 bit 01 : Word length is 6 bit 10 : Word length is 7 bit 11 : Word length is 8 bit

MODEM Control Register – Base + 4

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:5	Reserved	R/W	Return 0 when read.
4	LOOP	R/W	0 : UART in normal condition. 1 : UART is internal loop back
3	OUT2	R/W	0 : All interrupt is disable. 1 : Interrupt is enabled/disabled by IER.
2	OUT1	R/W	Read from MSR[6] is loop back mode
1	RTS	R/W	0 : RTS# is forced to logic 1 1 : RTS# is forced to logic 0
0	DTR	R/W	0 : DTR# is forced to logic 1 1 : DTR# is forced to logic 0

Line Status Register – Base + 5

Power-on default [7:0] = 0x60h.

Bit	Name	R/W	Description
7	RCR_ERR	R	0 : No error in the FIFO when FIFO is enabled 1 : Error in the FIFO when FIFO is enabled.
6	TEMT	R	0 : Transmitter is in transmitting. 1 : Transmitter is empty.
5	THRE	R	0 : Transmitter Holding Register is not empty. 1 : Transmitter Holding Register is empty.
4	BI	R	0 : No break condition is detected. 1 : A break condition is detected.
3	FE	R	0 : Data received has no frame error. 1 : Data received has frame error.
2	PE	R	0 : Data received has no parity error. 1 : Data received has parity error.
1	OE	R	0 : No overrun condition occur. 1 : A overrun condition occur.
0	DR	R	0 : No data is ready for read. 1 : Data is received .

MODEM Status Register – Base + 6

Power-on default [7:0] = 0xX0h.

Bit	Name	R/W	Description
7	DCD	R	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	Complement of RI# input. In loop back mode, this bit is equivalent to OUT1 in MCR.
5	DSR	R	Complement of DSR# input. In loop back mode, this bit is equivalent to DTR in MCR
4	CTS	R	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	0 : No state changed at DCD#. 1 : State changed at DCD#.
2	TERI	R	0 : No Trailing edge at RI#. 1 : A low to high transition at RI#.
1	DDSR	R	0 : No state changed at DSR#. 1 : State changed at DSR#.
0	DCTS	R	0 : No state changed at CTS#. 1 : State changed at CTS#.

Scratch Register – Base + 7

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	SCR_DATA[7:0]	R/W	Scratch register.

6.3.2 Programmable Baud Rate

The below table shows the use of baud generator with the different frequency 1.8461 MHZ, 14MHz, 24MHz.

$$\text{BaudRate} = \frac{\text{COM\_CLK}}{\text{Divisor} * 16}$$

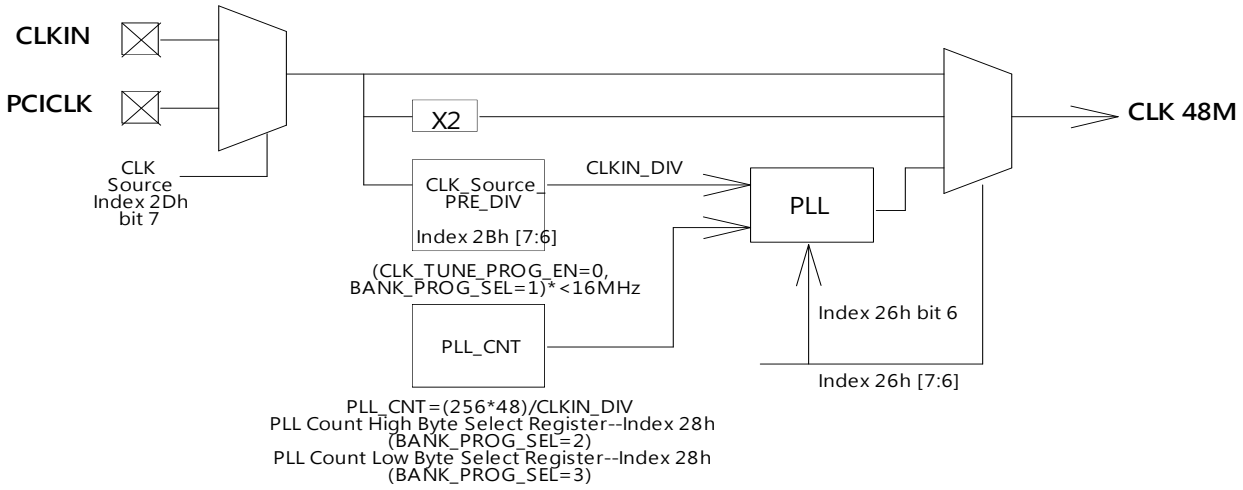
BAUD RATE FROM DIFFERENT PRE-DIVIDER					
PRE-DIV: 13 1.8461 MHz	**PRE-DIV: 1.625 14.769 MHz**	**PRE-DIV: 1.3 18.461 MHz**	**PRE-DIV: 1.0 24 MHz**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERECNTAGE**
50	400	500	650	2308	0
75	600	7500	975	1538	0
110	880	1100	1430	1049	0
135	1080	1350	1755	855	0
150	1200	1500	1950	769	0
300	2400	3000	3900	385	0
600	4800	6000	7800	192	0
1200	9600	12000	15600	96	0
1800	14400	18000	23400	64	0.01%
2000	16000	20000	26000	58	0.01%
2400	19200	24000	31200	48	0.01%
3600	28800	36000	46800	32	0.01%
4800	38400	48000	62400	24	0.01%
7200	57600	72000	93600	16	0.01%
9600	76800	96000	124800	12	0.01%
19200	153600	192000	249600	6	0.01%
38400	307200	384000	499200	3	0.01%
57600	460800	576000	748800	2	0.01%
115200	921600	1152000	1497600	1	0.01%

Example 1 : $1.5\ \text{MHz} = \frac{24}{1 * 16}$ **Example 2 :** $0.576\ \text{MHz} = \frac{18.461}{2 * 16}$

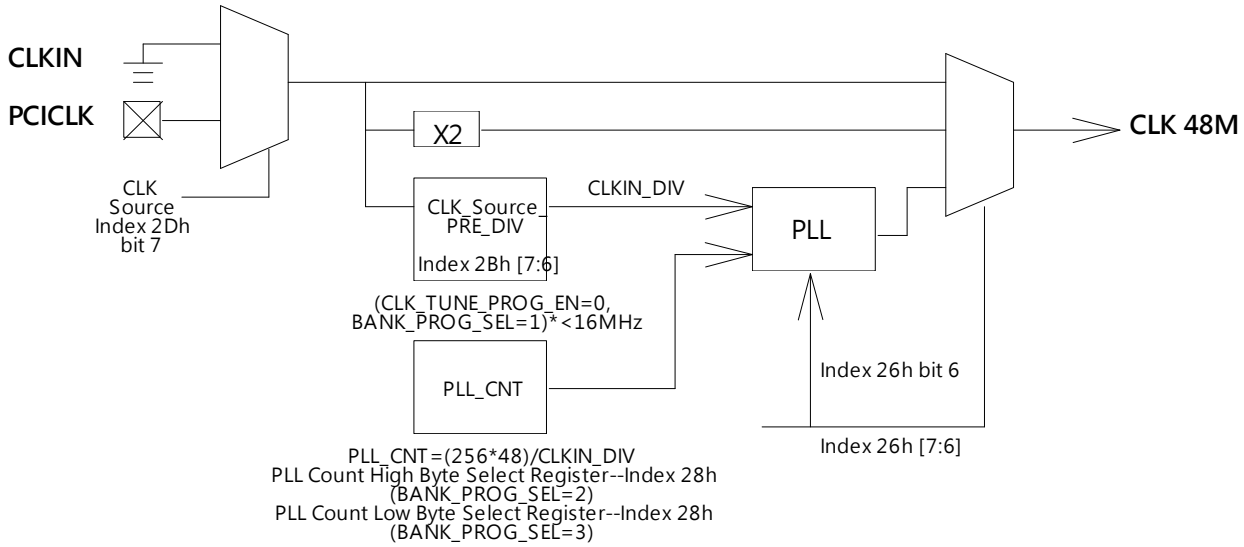
6.4 CLKIN

The clock in is programmable with the internal register. Please check below figure for the detail flow:

Option A. CLKIN input 24M/48MHz or 10M~50M Hz input ; PCI clock 10M~33 MHz input.



Option B. Without CLKIN for system clock, the system clock is programmable by the internal register(only for LPC). PCI clock 10M~33 MHz input.



6.5 Watch Dog Timer Function

Watch dog timer is provided for system controlling. After the programmed time interval elapses, WDT_OUT# will asserts a programmable low pulse with 1ms, 5ms, 125ms or 5sec. WDT-OUT# is a open drain pin which should be pull-up to 3VCC if the core power is 3VSB for eSPI platform. The setting of time interval has two ways:

1. By power on strap, the timer is automatic enabled with 10 second if PS_WDT is pull-up (default by internal pull-up).
2. By programming the registers. Two relative registers are used as mentioned below:

Timer Status and Control Register – Base + 0

Power-on default [7:0] = 0x02.

Bit	Name	R/W	Description
7:3	Reserved	R/W	Return 0 when read.
2:1	WDT_UNIT[1:0]	R/W	00 : Timer Unit is 10ms. 01 : Timer Unit is 1 second 10 : Timer Unit is 1 minute. 11 : reserved.
0	WDT_EVENT	R/W	When read 0 : no time out occur. 1 : time out has occurred. when write 0 : no action 1 : clear the time out status.

Timer Count Number Register – Base + 1

Power-on default [7:0] = 0x0Ah

Bit	Name	R/W	Description
7:0	WDT_CNT[7:0]	R/W	The number of count for watchdog timer. Write the same value to enable the timer, write 0 to disable timer.

6.6 General-Purpose Input / Output (GPIO) Ports

F81281 has 48 pins GPIO in total. All GPIO supports digit IO for Input/Output control, Output data control, input status, Open Drain/Push Pull function selection and interrupt status to assert interrupt via SIRQ. The GPIO0x also support four output mode which support normal level output, inverted level output, high pulse and low pulse.

GPIO Access Method

There are six sets of GPIO which can be accessed by three ways as below:

Configuration register port: Use 0x4E/0x4F (or 0x2E/0x2F) port with logic device number 0x09. Please refer to configuration register for detail.

Index/Data port: The index port is base address + 0 and data port is base address + 1. To access the GPIO register, user should first write index to index port and then read/write from/to all the GPIO control/status registers. The index for each register is same as the definition in configuration register.

Digital I/O: This way could access GPIO data register only. It is used for quickly control the GPIO pins. The register for each address is as below table:

GPIO Digital I/O Registers									
Offset	**Register Name**	**Default Value**							
		MSB							**LSB**
0h	Index Port	1	1	1	1	1	1	1	1
1h	Data Port	-	-	-	-	-	-	-	-
2h	GPIO0 Data Port	-	-	-	-	-	-	-	-
5h	GPIO3 Data Port	-	-	-	-	-	-	-	-

GPIO0 Data Port — Base + 2h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO0_DATA	R/W	LRESET#/ 3VCC	-	GPIO0 Data Control Write data to this byte will change the value of GPIO00_ DATA ~ GPIO07_ DATA in configuration register as writing data to index 0xF1. Read data from this byte will read the pin status of GPIO00_ST ~ GPIO07_ST as the value in index 0xF2

GPIO3 Data Port — Base + 5h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO3_DATA	R/W	LRESET#/ 3VCC	-	GPIO3 Data Control Write data to this byte will change the value of GPIO30_ DATA ~ GPIO37_ DATA in configuration register as writing data to index 0xC1. Read data from this byte will read the pin status of GPIO30_ST ~ GPIO37_ST as the value in index 0xC2

6.7 Serial IRQ

F81214E supports a serial IRQ scheme. Because more than one device may need to share the signal serial IRQ signal line, an open drain signal scheme is used. The clock source is the PCI clock. The serial interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: a start frame, several IRQ/Data frame, and one Stop frame.

6.7.1 Start Frame

There are two modes of operation for the SERIRQ Start frame: Quiet mode and Continuous mode. In the Quiet mode, the peripheral drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the states machines of the peripherals from idle to active states. The host controller will then take over driving SERIRQ signal low in the next clock and will continue driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the SERIRQ high for one clock and then tri-states it. In the Continuous mode, only the host controller initiates the START frame to update IRQ/Data line information. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start frame.

6.7.2 IRQ/Data Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase.During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the peripheral device drives the SERIRQ high. During the Turn-around phase, the peripheral device left the SERIRQ tri-stated.The IRQ/Data Frame has a number of specific order, as shown in Table 2. The F81214E is only support IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, and IRQ11.

Table 2 IRQSER Sampling periods

IRQ/Data Frame	Signal Sampled	# of clocks past Start
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

6.7.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate SERIRQ by a Stop frame. Only the host controller can initiate the Stop frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the next SERIRQ cycle's Sample mode is the Continuous mode.

7 Register Description

To enable configuration registers programming, entry key must output twice to index port continuously. The entry key is decided by the power on setting pins DTR4#/PS_CONF_KEY0 as following:

Pin 12: DTR4#/PS_CONF_KEY0	Entry key
0	0x87
1	0x67 (default)

To exit configuration registers programming, output 0xAA to index port.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	1	0	1	1	1
21	Chip ID Register	0	0	0	1	0	1	0	0
23	Vendor ID Register	0	0	0	1	1	0	0	1
24	Vendor ID Register	0	0	1	1	0	1	0	0
25	Clock Select Register	0	0	0	0	0	0	0	0
26	WDT Control Register	0	0	0	0	0	0	0	0
27	Port Select Register	-	-	-	1/0	-	-	1/0	1/0
28	Multi-function Select Register	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
29	Multi-function Select Register	0	0	0	0	0	0	0	0
2A	PLL (Programmable CLKIN) Counter High	0	0	0	0	0	0	1	1
2B	PLL (Programmable CLKIN) Counter Low	0	1	0	1	1	0	0	1
2C	Clock Control	0	0	0	0	0	0	0	0
2D	Reserved	0	0	0	0	0	0	0	0
2E	Reserved	0	0	0	0	0	0	0	0

Device Configuration Registers

"-" Reserved or Tri-State

UART1 Device Configuration Registers (LDN CR00)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	0	1/0	1/0
61	Base Address Low Register	1/0	1/0	1/0	1/0	1/0	0	0	0
70	IRQ Channel Select Register	-	0	0	0	0	0	1/0	1/0
F0	Clock Select Register	0	0	0	0	0	0	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Select Register	0	0	0	0	0	0	0	0
F7	Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART LED Enable Register	-	-	-	-	-	-	0	0
FF	9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1
UART4 Device Configuration Registers (LDN CR03)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	0	1/0	0
61	Base Address Low Register	1/0	1/0	1/0	0	1/0	0	0	0
70	IRQ Channel Select Register	-	0	0	0	1/0	0	0	1/0
F0	Clock Select Register	0	0	0	0	0	0	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Mode Select Register	0	0	0	0	0	0	0	0
F7	Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART LED Enable Register	-	-	-	-	-	-	0	0
FF	9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1
WDT Device Configuration Registers (LDN CR08)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	WDT Device Enable Register	-	-	-	-	-	-	-	1

60	Base Address High Register	0	0	0	0	0	1	0	0
61	Base Address Low Register	0	1	0	0	0	0	1	0
70	IRQ Channel Select Register	-	-	-	0	0	0	0	0
F0	Timer Status and Control Register	-	-	-	-	-	0	1	0
F1	Timer Count Number Register	0	0	0	0	1	0	1	0
GPIO Registers (LDN CR09)									
Register 0x[HEX]	**Register Name**	**Default Value MSB**							**LSB**
30	GPIO Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	IRQ Channel Select Register	0	0	0	0	0	0	0	0
F0	GPIO0 Output Enable Register	0	0	0	0	0	0	0	0
F1	GPIO0 Output Data Register	0	0	0	0	0	0	0	0
F2	GPIO0 Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO0 Drive Enable Register	0	0	0	0	0	0	0	0
F4	GPIO0 IRQ Enable Register	0	0	0	0	0	0	0	0
F5	GPIO0 Detect Edge Select Register	1	1	1	1	1	1	1	1
F6	GPIO0 IRQ Event Register	0	0	0	0	0	0	0	0
F7	GPIO0 Pulse Width Register 1	0	0	0	0	0	0	0	0
F8	GPIO0 Pulse Width Register 2	0	0	0	0	0	0	0	0
F9	GPIO0 Output Mode Register 1	0	0	0	0	0	0	0	0
FA	GPIO0 Output Mode Register 2	0	0	0	0	0	0	0	0
C0	GPIO3 Output Enable Register	0	0	-	-	0	0	0	0
C1	GPIO3 Output Data Register	1	1	-	-	1	1	1	1
C2	GPI03 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	0	0	-	-	0	0	0	0
C4	GPIO3 IRQ Enable Register	0	0	-	-	0	0	0	0
C5	GPIO3 Detect Edge Select Register	1	1	-	-	1	1	1	1
C6	GPIO3 IRQ Event Register	0	0	-	-	0	0	0	0

7.1 Global Control Registers

Software Reset Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	SOFT_RST	R/W	-	0	Write 1 to reset the register and device powered by VDD (VCC).

Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET# /3VCC	00h	00h : Select UART 1 device configuration register 03h : Select UART 4 device configuration register 08h : Select Watchdog Timer device configuration register 09h : Select GPIO device configuration register Otherwise: reserved

Chip ID Register — Index 20h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID1	R	-	17h	Chip ID 1.

Chip ID Register — Index 21h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID2	R	-	14h	Chip ID2.

Vendor ID Register — Index 23h

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID1	R	-	19h	Vendor ID 1 of Fintek devices.

Vendor ID Register — Index 24h

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID2	R	-	34h	Vendor ID 2 of Fintek devices.

Clock Select Register — Index 25h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	R/W	LRESET #/3VCC	0	Reserved for future use.
3	UR2_SOFT_PD	R/W		0	Set “1” to power down UART2.
2	UR1_SOFT_PD	R/W		0	Set “1” to power down UART1.

1-0	CLK_SEL	R/W	3VSB	0	00: The CLKIN is 24MHz. 01 : The CLKIN is 48MHz 1x : The CLKIN is as programmed. This bit must program to indicate the frequency of the clock source, or the device will not function correctly. Refer to PLL_CNT_H and PLL_CNT_L for programmable CLKIN.

WDT Control Register — Index 26h

Bit	Name	R/W	Reset	Default	Description
7	WDT_RST_EN	R/W	3VSB	0	Set “1” to enable reset registers when WDT timeout.
6	WDT_AUTO_RELOAD	R/W		0	Set “1” to auto reload timer after assertion of WDT_OUT#.
5	WDT_MODE1	R/W		0	0: Reload timer during LRESET# assertion. 1: Not reload timer during LRESET# assertion.
4	WDT_MODE0	R/W		0	0: Stop counting during LRESET# assertion. 1: Continue counting during LRESET# assertion.
3	Reserved	R/W	LRESET#/3VCC	0	Reserved for future use.
2	WDT_OUT_SEL	R/W		0	0: Timer out event low pulse. 1: Output 1KHz clock.
1	WDT_RD_RELOAD_DIS	R/W		0	0: Read WDT timer will reload the timer. 1: Read WDT timer will not reload the timer.
0	WDT_OUT_DIS	R/W		0	0: Output event select by WDT_OUT_SEL to WDT_OUT#. 1: No output to WDT_OUT#, set status only.

Port Select Register — Index 27h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	LRESET#/3VCC	-	Reserved.
4	PORT_4E_EN	-		-	The default value of this bit is decided by power on strap pin PS_CONF_2E. The trap value is inverted with the PS_CONF_2E. 0: The configuration port is 0x2E/0x2F. 1: The configuration port is 0x4E/0x4F.
3-2	Reserved	-		-	Reserved.

1-0	ENTRY_KEY_SEL	R/W		-	Configuration Entry Key Select. The default value of these bits are determined by PS_CONF_KEY0. Bit 1 default “1” after power on. 00: The entry key is 0x77. 01: The entry key is 0xA0. 10: The entry key is 0x87. 11: The entry key is 0x67.

Multi-Function Select Register — Index 28h

Bit	Name	R/W	Reset	Default	Description
7-6	UR4_GP_SEL	R/W	LRESET #/3VCC	11b/00b	Select pin function for UART4 and GPIO0. These bits are power on strap by PS_UR_GPIO. 00: All pins function as GPIO 01: Enable SIN4 and SOUT4, others function as GPIO. 10: Enable SIN4, SOUT4 and RTS4#, others function as GPIO 11: Enable all UART pins.
5-2	Reserved	R/W		11b/00b	Reserved for future use.
1-0	UR1_GP_SEL	R/W		11b/00b	Select pin function for UART1 and GPIO3 except GPIO34, GPIO35. These bits are power on strap by PS_UR_GPIO. 00: All pins function as GPIO 01: All pins function as GPIO 10: Enable RTS1#, others function as GPIO 11: Enable all UART pins.

Multi-Function Select Register — Index 29h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R/W	3VSB	0	Reserved for future use.
6	SIRQ_QM_WAIT	R/W		0	Set “1” to wait 16 cycles for next interrupt request in quiet mode.
5	SIRQ_NO_FERR	R/W		0	Set “1” to discard start frame error for SIRQ.
4	TRAP_BY_3VCC	R/W		0	0: Power on strap by LRESET# and 3VCC. 1: Power on strap by 3VCC.
3-0	Reserved	R/W		0	Reserved for future use.

PLL Count High Byte Register — Index 2Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PLL_CNT_H	R/W	3VSB	3h	PLL_CNT is composed by PLL_CNT_H and PLL_CNT_L which are used to indicate the clock generator to generate 48MHz according the CLKIN_PRE_DIV. PLL_CNT is calculated by the equation: PLL_CNT = (256*48) / CLKIN_DIV.

PLL Count Low Byte Register — Index 2Bh

Bit	Name	R/W	Reset	Default	Description
7-0	PLL_CNT_L	R/W	3VSB	5Bh	PLL_CNT is composed by PLL_CNT_H and PLL_CNT_L which are used to indicate the clock generator to generate 48MHz according the CLKIN_PRE_DIV. PLL_CNT is calculated by the equation: PLL_CNT = (256*48) / CLKIN_DIV.

Clock Control Register — Index 2Ch

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R/W	3VSB	0	Reserved for future use.
5-4	WDT_PUL_SEL	R/W		0	Select the output pulse width of WDT_OUT# 00: 1ms. 01: 25ms. 10: 125ms. 11: 5s.
3	PLT_RST_EN	R/W		0	Set “1” to enable eSPI PLTRST#. This bit has no effect in LPC platform.
2	CLK_SRC_SEL	R/W		0	Select the clock source. 0: CLKIN pin. 1: LCLK pin. The clock source can’t stop for internal PLL circuit to generate correct 48MHz clock.

1-0	CLKIN_PRE_DIV	R/W		00b	These registers are used to calculate CLKIN_DIV to generate internal 48MHz clock where the calculated CLKIN_DIV value should be under 16MHz. The equation is as follow: CLKIN_DIV = Clock Source / (CLKIN_PRE_DIV), where CLKIN_PRE_DIV value is 00: bypass 01:divided by 2 10:divided by 4 11:divided by 6

Reserved Register — Index 2Dh

Bit	Name	R/W	Reset	Default	Description
7-0	Reserved	R/W	-	0	Reserved for future use.

Reserved Register — Index 2Eh

Bit	Name	R/W	Reset	Default	Description
7-0	Reserved	R/W	3VSB	0	Reserved for future use.

7.2 UART1 Registers (CR00)

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	LRESET#/ 3VCC	-	Reserved
0	UR_EN	R/W		1/0	0: disable UART 1. 1: enable UART 1. This bit is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. Refer to power on strap configuration for default value.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR _HI	R/W	LRESET# /3VCC	3h/0h	The MSB of UART 1 base address. This byte is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. Refer to power on strap configuration for default value.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR _LO	R/W	LRESET# /3VCC	F8h/E0h/00h	The LSB of UART 1 base address. This byte is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. Refer to power on strap configuration for default value.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	LRESET#/ 3VCC	-	Reserved.
6-5	IRQ_MODE	R/W		2'b00	00 : Sharing IRQ active low Level. 01 :Sharing IRQ active high edge. 10 :Sharing IRQ active high Level. 11 :Reserved. This bit is effective at IRQ is sharing with other device (IRQ_SHAR, bit 1).
4	IRQ_SHAR	R/W		0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.
3-0	SELIRQ	R/W		3h/0h	Select the IRQ channel for UART 1. This byte is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. Refer to power on strap configuration for default value.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#/ 3VCC	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.

6	AUTO_ADDR	R/W		0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RTS_Invert	R/W		0	0: Default non function 1: When RS485_UR1 set to 1, RTS# signal will be inverted when assert out.
4	RS485	R/W		0	0: RS232 mode 1: RS485 mode: RTS# will assert high when transmitting data; otherwise, RTS# will be low.
3-2	Reserved	R/W		0	Reserved for future use.
1-0	SELCLK1 SELCLK0	R/W		00	00: UART 1 clock source is 1.8462MHz (24MHz/13) 01: UART 1 clock source is 18MHz. 10: UART 1 clock source is 24MHz. 11: UART 1 clock source is 14MHz.

9-bit Mode Slave Address Register — Index F4h

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-0</td><td>SADDR</td><td>R/W</td><td>LRESET#/
3VCC</td><td>00h</td><td>This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address.
Follow the description to determine the given address and broadcast address:
1. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care.
2. broadcast address: If bit n of ored SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address.
Ex.
<table>
<tr><td>SADDR</td><td>0101_1100b</td></tr>
<tr><td>SADEN</td><td>1111_1001b</td></tr>
<tr><td>Given Address</td><td>0101_1xx0b</td></tr>
<tr><td>Broadcast Address</td><td>1111_11x1b</td></tr>
</table>
</td></tr>
</table>

9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	SADEN	R/W	LRESET#/ 3VCC	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART1 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR_UR1 is don’t care. 1. broadcast address: If bit n of ored SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

128 Byte FIFO Control Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL	R/W	LRESET#/ 3VCC	0	TX holding register empty delay 1 txclk, when set 1
6	TX_INT_MODE	R/W		0	0: Interrupt is asserted when FIFO is empty. 1: Interrupt is asserted when FIFO and transmission register is empty.
5-4	RXFTHR_MODE	R/W		00	Set the multiple trigger level for the RCVR FIFO interrupt. 00: 1 multiple Trigger Level interrupt, when received data 01: 2 multiple Trigger Level interrupt, when received data 10: 4 multiple Trigger Level interrupt, when received data 11: 8 multiple Trigger Level interrupt, when received data
3	Reserved	R/W		00	Reserved for future use.
2	AUTO_FLOW_POL	R/W		0	0: High active. 1: Low active.

1-0	FIFO_MODE	R/W		00	Set the FIFO SIZES for TX/RX. 00: 16 Byte FIFO. 01: 32 Byte FIFO. 10: 64 Byte FIFO. 11: 128 Byte FIFO.

Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#/ 3VCC	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W		0h	Threshold for RX to request data via RTS# or DTR#. When RX FIFO is under this threshold, RX asserts RTS# or DTR# to request new data.

Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_PIN _SEL	R/W	LRESET#/ 3VCC	0	Select pin for auto flow control. 0: DTR#/DSR#. 1: RTS#/CTS#.
6-0	XOFF_THR	R/W		0h	When RX FIFO exceeds this threshold, RX de-asserts RTS# or DTR# to inform TX to stop transmitting data.

LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	RX_LED_EN	R/W	LRESET# /3VCC	0	Set “1” to enable RX LED to DSR#. When data is received, a 50ms pulse output to DSR#. The maximum frequency is 5Hz.
0	TX_LED_EN	R/W		0	Set “1” to enable TX LED to DTR#. When data is sent, a 50ms pulse outputs to DTR#. The maximum frequency is 5Hz.

9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET# /3VCC	FFh	Broadcast address for 9-bit mode. Write the byte to set broadcast address instead of the one calculated by SADDR.

7.3 UART4 Registers (CR03)

UART 4 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UR_EN	R/W	LRESET# /3VCC	1/0	0: disable UART 4. 1: enable UART 4. This bit is determined by SOUT4/PS_2E8_IRQD. Refer to power on configuration table for default.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#/ 3VCC	2h/0h	The MSB of UART 4 base address. This byte is determined by SOUT4/PS_2E8_IRQD. Refer to power on configuration table for default.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#/ 3VCC	E8h/00h	The LSB of UART 4 base address. This byte is determined by SOUT4/PS_2E8_IRQD. Refer to power on configuration table for default.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6-5	IRQ_MODE	R/W	LRESET#/ 3VCC	2'b00	00 : Sharing IRQ active low Level mode. 01 :Sharing IRQ active high edge mode. 10 :Sharing IRQ active high Level mode. 11 :Reserved. This bit is effective at IRQ is sharing with other device (IRQ_SHAR, bit 1).
4	IRQ_SHAR	R/W		0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.
3-0	SELIRQ	R/W		9h/0h	Select the IRQ channel for UART 4. This byte is determined by SOUT4/PS_2E8_IRQD. Refer to power on configuration table for default.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#/ 3VCC	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit..
6	AUTO_ADDR	R/W		0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RTS_Invert	R/W		0	0: Default non function 1: When RS485 set to 1, RTS# signal will be inverted when assert out.
4	RS485	R/W		0	0: RS232 mode 1: RS485 mode: RTS# will assert high when transmitting data; otherwise, RTS# will be low.
3-2	Reserved	R/W		0	Reserved for future use.
1-0	SELCLK1 SELCLK0	R/W		00	00: UART 4 clock source is 1.8462MHz (24MHz/13) 01: UART 4 clock source is 18MHz. 10: UART 4 clock source is 24MHz. 11: UART 4 clock source is 14MHz.

9-bit Mode Slave Address Register — Index F4h

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-0</td><td>SADDR_URD</td><td>R/W</td><td>LRESET#/
3VCC</td><td>00h</td><td>This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address.
Follow the description to determine the given address and broadcast address:
3. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care.
4. broadcast address: If bit n of ored SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address.
Ex.
<table>
<tr><td>SADDR</td><td>0101_1100b</td></tr>
<tr><td>SADEN</td><td>1111_1001b</td></tr>
<tr><td>Given Address</td><td>0101_1xx0b</td></tr>
<tr><td>Broadcast Address</td><td>1111_11x1b</td></tr>
</table>
</td></tr>
</table>

9-bit Mode Slave Address Mask Register — Index F5h

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-0</td><td>SADEN</td><td>R/W</td><td>LRESET#/
3VCC</td><td>00h</td><td>This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address.
Follow the description to determine the given address and broadcast address:
1. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care.
2. broadcast address: If bit n of ored SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address.
Ex.
<table>
<tr><td>SADDR</td><td>0101_1100b</td></tr>
<tr><td>SADEN</td><td>1111_1001b</td></tr>
<tr><td>Given Address</td><td>0101_1xx0b</td></tr>
<tr><td>Broadcast Address</td><td>1111_11x1b</td></tr>
</table>
</td></tr>
</table>

128 Byte FIFO Control Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL	R/W	LRESET#/3VCC	0	TX holding register empty delay 1 txclk, when set 1
6	TX_INT_MODE	R/W		0	0: Interrupt is asserted when FIFO is empty. 1: Interrupt is asserted when FIFO and transmission register is empty.
5-4	RXFTHR_MODE	R/W		00	Set the multiple trigger level for the RCVR FIFO interrupt. 00: RX trigger level is 1, 4, 8, 14 bytes. 01: RX trigger level is 2, 8, 16, 28 bytes. 10: RX trigger level is 4, 16, 32, 56 bytes. 11: RX trigger level is 8, 32, 64, 112 bytes.
3	Reserved	R/W		00	Reserved for future use.
2	AUTO_FLOW_POL	R/W		0	0: High active. 1: Low active.
1-0	FIFO_MODE	R/W		00	Set the FIFO Sizes for TX/RX. 00: 16 Byte FIFO. 01: 32 Byte FIFO. 10: 64 Byte FIFO. 11: 128 Byte FIFO.

Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#/3VCC	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W		0h	Threshold for RX to request data via RTS# or DTR#. When RX FIFO is under this threshold, RX asserts RTS# or DTR# to request new data.

Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_PIN_SEL	R/W	LRESET#/3VCC	0	Select pin for auto flow control. 0: DTR#/DSR#. 1: RTS#/CTS#.
6-0	XOFF_THR	R/W		0h	When RX FIFO exceeds this threshold, RX de-asserts RTS# or DTR# to inform TX to stop transmitting data.

LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	RX_LED_EN	R/W	LRESET#/ 3VCC	0	Set “1” to enable RX LED to DSR#. When data is received, a 50ms pulse output to DSR#. The maximum frequency is 5Hz.
0	TX_LED_EN	R/W		0	Set “1” to enable TX LED to DTR#. When data is sent, a 50ms pulse outputs to DTR#. The maximum frequency is 5Hz.

9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET# /3VCC	FFh	Broadcast address for 9-bit mode. Write the byte to set broadcast address instead of the one calculated by SADDR.

7.4 Watchdog Timer Registers (CR08)

WDT Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	WDT_EN	R/W	LRESET#/ 3VCC	1	0: disable WDT. 1: enable WDT.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#/ 3VCC	4h	The MSB of WDT base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#/ 3VCC	42h	The LSB of WDT base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.

4	WDTIRQ_EN	R/W	LRESET#/ 3VCC	0	0 : Disable WDT IRQ. 1 : Enable WDT IRQ.
3-0	SELWDTIRQ	R/W		0h	Select the IRQ channel for WDT.

Timer Status and Control Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
2-1	WDT_UNIT	R/W	LRESET#/ 3VCC	01	00 : Timer Unit is 10ms. 01 : Timer Unit is 1 second 10 : Timer Unit is 1 minute. 11 : reserved. Change unit will reload the timer.
0	WDT_EVENT	R/W	3VCC	0	0 : no time out occur. 1 : time out has occurred. Write “1” to this bit will clear the status.

Timer Count Number Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7-0	WDT_CNT	R/W	LRESET#/ 3VCC	Ah	The number of count for watchdog timer. Write the same non-zero value twice to enable the timer, otherwise will disable timer.

7.5 GPIO Registers (CR09)

GPIO Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	GPIO_EN	R/W	LRESET#/ 3VCC	0	0: disable GPIO IO Port. 1: enable GPIO IO Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#/ 3VCC	0	The MSB of GPIO base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description

7-0	BASE_ADDR_LO	R/W	LRESET#/ 3VCC	0	The LSB of GPIO base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELWDTIRQ	R/W	LRESET#/ 3VCC	0h	Select the IRQ channel for GPIO.

GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_OE	R/W	LRESET# /3VCC	0	0: GPIO07 is input. 1: GPIO07 is output.
6	GPIO06_OE	R/W		0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W		0	0: GPIO05 is input. 1: GPIO05 is output.
4	GPIO04_OE	R/W		0	0: GPIO04 is input. 1: GPIO04 is output.
3	GPIO03_OE	R/W		0	0: GPIO03 is input. 1: GPIO03 is output.
2	GPIO02_OE	R/W		0	0: GPIO02 is input. 1: GPIO02 is output.
1	GPIO01_OE	R/W		0	0: GPIO01 is input. 1: GPIO01 is output.
0	GPIO00_OE	R/W		0	0: GPIO00 is input. 1: GPIO00 is output.

GPIO0 Output Data Register — Index F1h (This byte could also be written by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DATA	R/W	LRESET#/ 3VCC	0	This bit is used to control the GPIO07 output in output mode. The output value depends on the setting of GPIO07_MODE.

6	GPIO06_DATA	R/W		0	This bit is used to control the GPIO06 output in output mode. The output value depends on the setting of GPIO06_MODE.
5	GPIO05_DATA	R/W		0	This bit is used to control the GPIO05 output in output mode. The output value depends on the setting of GPIO05_MODE.
4	GPIO04_DATA	R/W		0	This bit is used to control the GPIO04 output in output mode. The output value depends on the setting of GPIO04_MODE.
3	GPIO03_DATA	R/W		0	This bit is used to control the GPIO03 output in output mode. The output value depends on the setting of GPIO03_MODE.
2	GPIO02_DATA	R/W		0	This bit is used to control the GPIO02 output in output mode. The output value depends on the setting of GPIO02_MODE.
1	GPIO01_DATA	R/W		0	This bit is used to control the GPIO01 output in output mode. The output value depends on the setting of GPIO01_MODE.
0	GPIO00_DATA	R/W		0	This bit is used to control the GPIO00 output in output mode. The output value depends on the setting of GPIO00_MODE.

GPIO0 Pin Status Register — Index F2h (This byte could also be read by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_ST	R/W	-	-	The pin status of GPIO07.
6	GPIO06_ST	R/W		-	The pin status of GPIO06.
5	GPIO05_ST	R/W		-	The pin status of GPIO05.
4	GPIO04_ST	R/W		-	The pin status of GPIO04.

3	GPIO03_ST	R/W		-	The pin status of GPIO03.
2	GPIO02_ST	R/W		-	The pin status of GPIO02.
1	GPIO01_ST	R/W		-	The pin status of GPIO01.
0	GPIO00_ST	R/W		-	The pin status of GPIO00.

GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DRV	R/W	LRESET#/ 3VCC	0	0: GPIO07 is open drain. 1: GPIO07 is push pull.
6	GPIO06_DRV	R/W		0	0: GPIO06 is open drain. 1: GPIO06 is push pull.
5	GPIO05_DRV	R/W		0	0: GPIO05 is open drain. 1: GPIO05 is push pull.
4	GPIO04_DRV	R/W		0	0: GPIO04 is open drain. 1: GPIO04 is push pull.
3	GPIO03_DRV	R/W		0	0: GPIO03 is open drain. 1: GPIO03 is push pull.
2	GPIO02_DRV	R/W		0	0: GPIO02 is open drain. 1: GPIO02 is push pull.
1	GPIO01_DRV	R/W		0	0: GPIO01 is open drain. 1: GPIO01 is push pull.
0	GPIO00_DRV	R/W		0	0: GPIO00 is open drain. 1: GPIO00 is push pull.

GPIO0 IRQ Enable Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_IRQ_EN	R/W	LRESET#/ 3VCC	0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO07_IRQ_ST is set.
6	GPIO06_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO06_IRQ_ST is set.
5	GPIO05_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO05_IRQ_ST is set.
4	GPIO04_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO04_IRQ_ST is set.

3	GPIO03_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO03_IRQ_ST is set.
2	GPIO02_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO02_IRQ_ST is set.
1	GPIO01_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO01_IRQ_ST is set.
0	GPIO00_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO00_IRQ_ST is set.

GPIO0 Detect Edge Select Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DET_SEL	R/W	LRESET#/ 3VCC	1	Select the edge for GPIO07_IRQ_ST. 0: Rising edge. 1: Falling edge.
6	GPIO06_DET_SEL	R/W		1	Select the edge for GPIO06_IRQ_ST. 0: Rising edge. 1: Falling edge.
5	GPIO05_DET_SEL	R/W		1	Select the edge for GPIO05_IRQ_ST. 0: Rising edge. 1: Falling edge.
4	GPIO04_DET_SEL	R/W		1	Select the edge for GPIO04_IRQ_ST. 0: Rising edge. 1: Falling edge.
3	GPIO03_DET_SEL	R/W		1	Select the edge for GPIO03_IRQ_ST. 0: Rising edge. 1: Falling edge.
2	GPIO02_DET_SEL	R/W		1	Select the edge for GPIO02_IRQ_ST. 0: Rising edge. 1: Falling edge.
1	GPIO01_DET_SEL	R/W		1	Select the edge for GPIO01_IRQ_ST. 0: Rising edge. 1: Falling edge.

0	GPIO00_DET_SEL	R/W		1	Select the edge for GPIO00_IRQ_ST. 0: Rising edge. 1: Falling edge.

GPIO0 IRQ Event Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_IRQ_ST	R/WC	LRESET#/3VCC	0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO07_DET_SEL is detected and GPIO07 is in input mode. Write “1” to clear this bit.
6	GPIO06_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO06_DET_SEL is detected and GPIO06 is in input mode. Write “1” to clear this bit.
5	GPIO05_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO05_DET_SEL is detected and GPIO05 is in input mode. Write “1” to clear this bit.
4	GPIO04_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO04_DET_SEL is detected and GPIO04 is in input mode. Write “1” to clear this bit.
3	GPIO03_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO03_DET_SEL is detected and GPIO03 is in input mode. Write “1” to clear this bit.

2	GPIO02_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO02_DET_SEL is detected and GPIO02 is in input mode. Write “1” to clear this bit.
1	GPIO01_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO01_DET_SEL is detected and GPIO01 is in input mode. Write “1” to clear this bit.
0	GPIO00_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO00_DET_SEL is detected and GPIO00 is in input mode. Write “1” to clear this bit.

GPIO0 Pulse Width Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO03_PW_SEL	R/W	LRESET#/ 3VCC	0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms
5-4	GPIO02_PW_SEL	R/W		0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms
3-2	GPIO01_PW_SEL	R/W		0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms

1-0	GPIO00_PW_SEL	R/W		0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms

GPIO0 Pulse Width Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_PW_SEL	R/W	LRESET#/ 3VCC	0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms
5-4	GPIO06_PW_SEL	R/W		0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms
3-2	GPIO05_PW_SEL	R/W		0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms
1-0	GPIO04_PW_SEL	R/W		0	Select the pulse width for pulse output mode. 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms

GPIO0 Output Mode Register 1 — Index F9h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO03_MODE	R/W	LRESET#/ 3VCC	0	Select the output mode for GPIO03 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
5-4	GPIO02_MODE	R/W		0	Select the output mode for GPIO02 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
3-2	GPIO01_MODE	R/W		0	Select the output mode for GPIO01 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
1-0	GPIO00_MODE	R/W		0	Select the output mode for GPIO00 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.

GPIO0 Output Mode Register 2 — Index FAh

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_MODE	R/W	LRESET#/ 3VCC	0	Select the output mode for GPIO07 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.

5-4	GPIO06_MODE	R/W		0	Select the output mode for GPIO06 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
3-2	GPIO05_MODE	R/W		0	Select the output mode for GPIO05 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
1-0	GPIO04_MODE	R/W		0	Select the output mode for GPIO04 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.

GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_OE	R/W	LRESET#/ 3VCC	0	0: GPIO37 is input. 1: GPIO37 is output.
6	GPIO36_OE	R/W		0	0: GPIO36 is input. 1: GPIO36 is output.
5-4	Reserved	R/W		0	Reserved for future use.
3	GPIO33_OE	R/W		0	0: GPIO33 is input. 1: GPIO33 is output.
2	GPIO32_OE	R/W		0	0: GPIO32 is input. 1: GPIO32 is output.
1	GPIO31_OE	R/W		0	0: GPIO31 is input. 1: GPIO31 is output.
0	GPIO30_OE	R/W		0	0: GPIO30 is input. 1: GPIO30 is output.

GPIO3 Output Data Register — Index C1h (This byte could also be written by base address + 5)

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DATA	R/W	LRESET#/ 3VCC	1	0: output low. 1: output high.
6	GPIO36_DATA	R/W		1	0: output low. 1: output high.
5-4	Reserved	R/W		11	Reserved for future use.
3	GPIO33_DATA	R/W		1	0: output low. 1: output high.
2	GPIO32_DATA	R/W		1	0: output low. 1: output high.
1	GPIO31_DATA	R/W		1	0: output low. 1: output high.
0	GPIO30_DATA	R/W		1	0: output low. 1: output high.

GPIO3 Pin Status Register — Index C2h (This byte could also be read by base address + 5)

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_ST	R/W	-	-	The pin status of GPIO37.
6	GPIO36_ST	R/W		-	The pin status of GPIO36.
5-4	Reserved	R/W		-	Reserved.
3	GPIO33_ST	R/W		-	The pin status of GPIO33.
2	GPIO32_ST	R/W		-	The pin status of GPIO32.
1	GPIO31_ST	R/W		-	The pin status of GPIO31.
0	GPIO30_ST	R/W		-	The pin status of GPIO30.

GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DRV	R/W	LRESET#/ 3VCC	0	0: GPIO37 is open drain. 1: GPIO37 is push pull.
6	GPIO36_DRV	R/W		0	0: GPIO36 is open drain. 1: GPIO36 is push pull.
5-4	Reserved	R/W		0	Reserved for future use.

3	GPIO33_DRV	R/W		0	0: GPIO33 is open drain. 1: GPIO33 is push pull.
2	GPIO32_DRV	R/W		0	0: GPIO32 is open drain. 1: GPIO32 is push pull.
1	GPIO31_DRV	R/W		0	0: GPIO31 is open drain. 1: GPIO31 is push pull.
0	GPIO30_DRV	R/W		0	0: GPIO30 is open drain. 1: GPIO30 is push pull.

GPIO3 IRQ Enable Register — Index C4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_IRQ_EN	R/W	LRESET#/3VCC	0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO37_IRQ_ST is set.
6	GPIO36_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO36_IRQ_ST is set.
5-4	Reserved	R/W		0	Reserved for future use.
3	GPIO33_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO33_IRQ_ST is set.
2	GPIO32_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO32_IRQ_ST is set.
1	GPIO31_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO31_IRQ_ST is set.
0	GPIO30_IRQ_EN	R/W		0	0: Disable IRQ. 1: Enable IRQ via SIRQ if GPIO30_IRQ_ST is set.

GPIO3 Detect Edge Select Register — Index C5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DET_SEL	R/W	LRESET#/3VCC	1	Select the edge for GPIO37_IRQ_ST. 0: Rising edge. 1: Falling edge.
6	GPIO36_DET_SEL	R/W		1	Select the edge for GPIO36_IRQ_ST. 0: Rising edge. 1: Falling edge.
5-4	Reserved	R/W		0	Reserved for future use.

3	GPIO33_DET_SEL	R/W		1	Select the edge for GPIO33_IRQ_ST. 0: Rising edge. 1: Falling edge.
2	GPIO32_DET_SEL	R/W		1	Select the edge for GPIO32_IRQ_ST. 0: Rising edge. 1: Falling edge.
1	GPIO31_DET_SEL	R/W		1	Select the edge for GPIO31_IRQ_ST. 0: Rising edge. 1: Falling edge.
0	GPIO30_DET_SEL	R/W		1	Select the edge for GPIO30_IRQ_ST. 0: Rising edge. 1: Falling edge.

GPIO3 IRQ Event Register — Index C6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_IRQ_ST	R/WC	LRESET#/3VCC	0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO37_DET_SEL is detected and GPIO37 is in input mode. Write “1” to clear this bit.
6	GPIO36_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO36_DET_SEL is detected and GPIO36 is in input mode. Write “1” to clear this bit.
5-4	Reserved	R/W		0	Reserved.
3	GPIO33_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO33_DET_SEL is detected and GPIO33 is in input mode. Write “1” to clear this bit.

2	GPIO32_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO32_DET_SEL is detected and GPIO32 is in input mode. Write “1” to clear this bit.
1	GPIO31_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO31_DET_SEL is detected and GPIO31 is in input mode. Write “1” to clear this bit.
0	GPIO30_IRQ_ST	R/WC		0	0: No IRQ event. 1: IRQ event occurred. This bit is set when an edge as specified in GPIO30_DET_SEL is detected and GPIO30 is in input mode. Write “1” to clear this bit.

8 Electrical Characteristic

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	-40 to +85	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC Characteristics

(Ta = -40° C to 85° C, VDD = 3.3V ± 10%, VSS = 0V)

Parameter	MIN	TYP	MAX	Unit
Voltage range	3.0	3.3	3.6	3VSB
Average operating current		20		mA

PARAMETER	SYM.	MIN	TYP	MAX.	UNIT	CONDITIONS
$IN_{st,\ 5v}$ - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = 3VSB
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,lv}$ - Low level input pin with schmitt trigger, low level.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Input High Leakage	ILIH			+1	μA	VIN = 3VSB
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/O_{16st,lv}$-Low level bi-directional pin with schmitt trigger, output with 16 mA sink capability, low level.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+16		mA	VOH = 0.7*IFP
Output Low Current	IOL		-16		mA	VOL = 0.3*IFP
Input High Leakage	ILIH			+1	μA	VIN = IFP
Input Low Leakage	ILIL	-1				

$I/OOD_{8st,5v}$-TTL level bi-directional pin and schmitt trigger, programmable open-drain output with 8mA source-sink capability, 5V tolerance.						
Input Low Threshold Voltage	VIL			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	VIH	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-8		mA	VOL = 0.4V
Output High Current	IOH		+8		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/O_{8t,5V,,u47}$ - TTL level bi-directional pin with 8 mA source-sink capability, 5V tolerance, pull-up 47KΩ						
Input Low Voltage	VIL			0.8	V	VDD = 3.3 V
Input High Voltage	VIH	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-8		mA	VOL = 0.4V
Output High Current	IOH		+8		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$OD_{12,5V}$ - Open-drain output pin with sink capability of 12 mA, 5V tolerance						
Output Low Current	IOL		12		mA	VOL = 0.4V

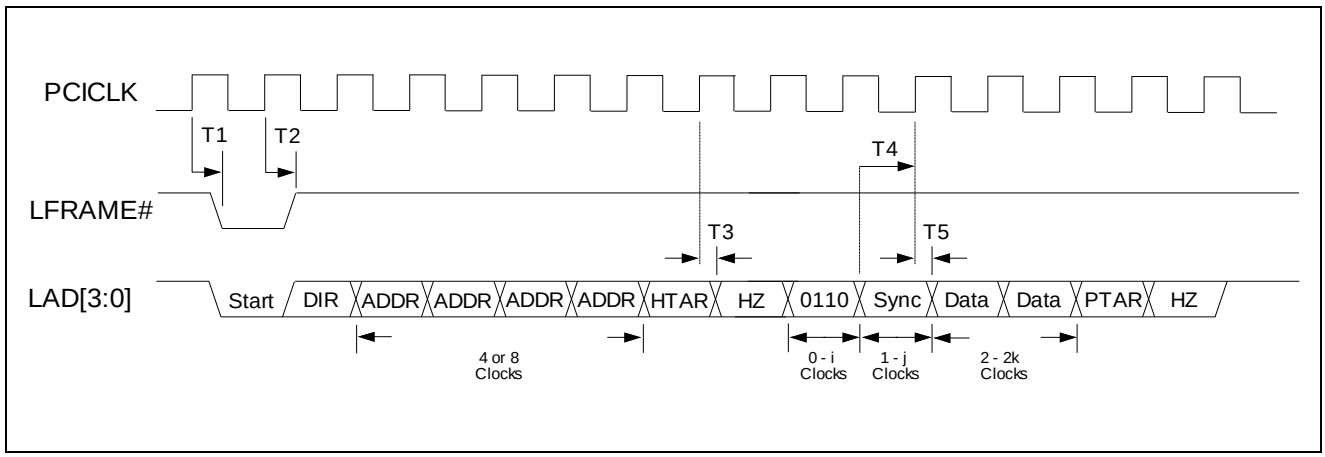
8.3 AC Characteristics

8.3.1 LPC Interface

LPC interface timing table

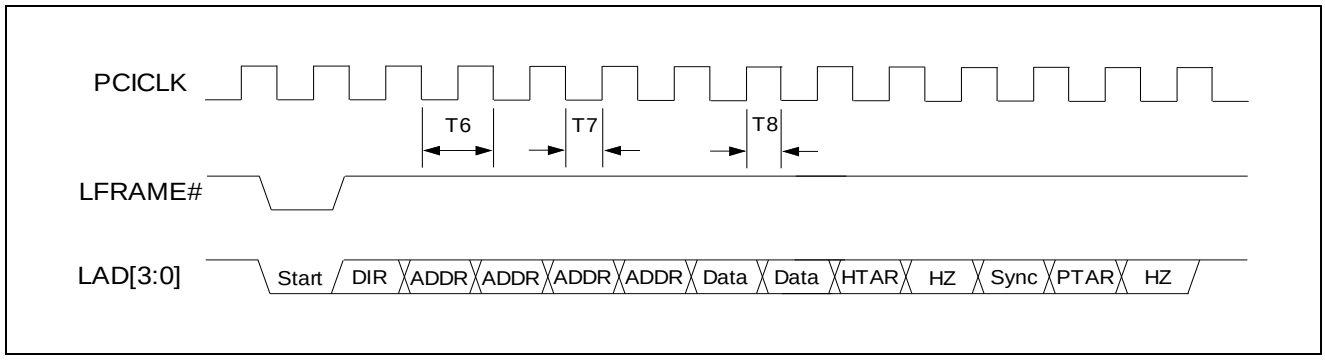
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	LFRAME# drive low after rising edge of PCICLK	2	12	nS
T2	LFRAME# drive high after rising edge of PCICLK	2	12	nS
T3	LAD [3:0] floating after rising edge of PCICLK		28	nS
T4	LAD [3:0] setup time to rising edge of PCICLK	7		nS
T5	LAD [3:0] hold time from rising edge of PCICLK	0		nS
T6	Period of PCICLK	27	33	nS
T7	Duration of PCICLK low	12		nS
T8	Duration of PCICLK high	12		nS

Typical Timing for Host Read



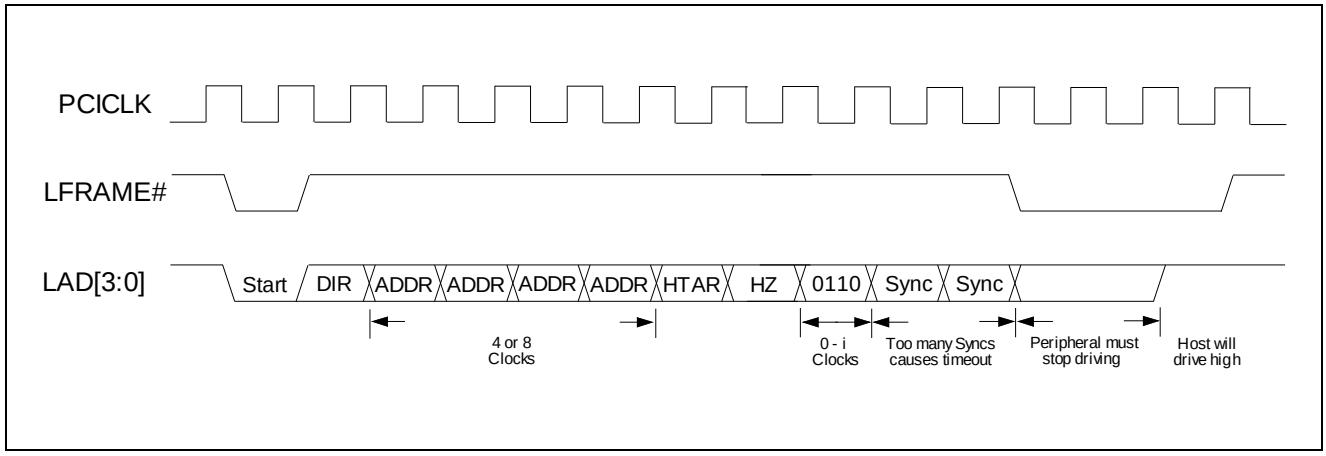
Host read timing diagram

Typical Timing for Host Write



Host write timing diagram

Timing for Aboart Mechanism



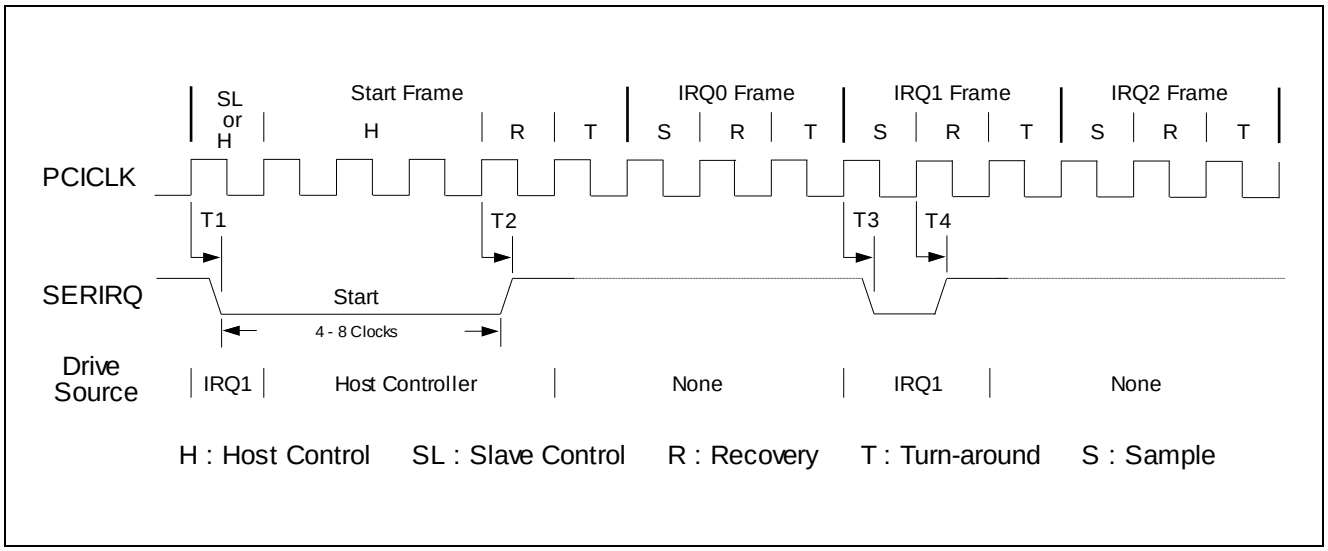
Host abort timing diagram

8.3.2 Serialized IRQ Interface

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Host drive SERIRQ low after rising edge of PCICLK	2	12	nS
T2	Host drive SERIRQ high after rising edge of PCICLK	2	12	nS
T3	Slave drive SERIRQ low after rising edge of PCICLK	2	12	nS
T4	Slave drive SERIRQ high after rising edge of PCICLK	2	12	nS
T5	Period of PCICLK	27	33	nS
T6	Duration of PCICLK low	12		nS
T7	Duration of PCICLK high	12		nS

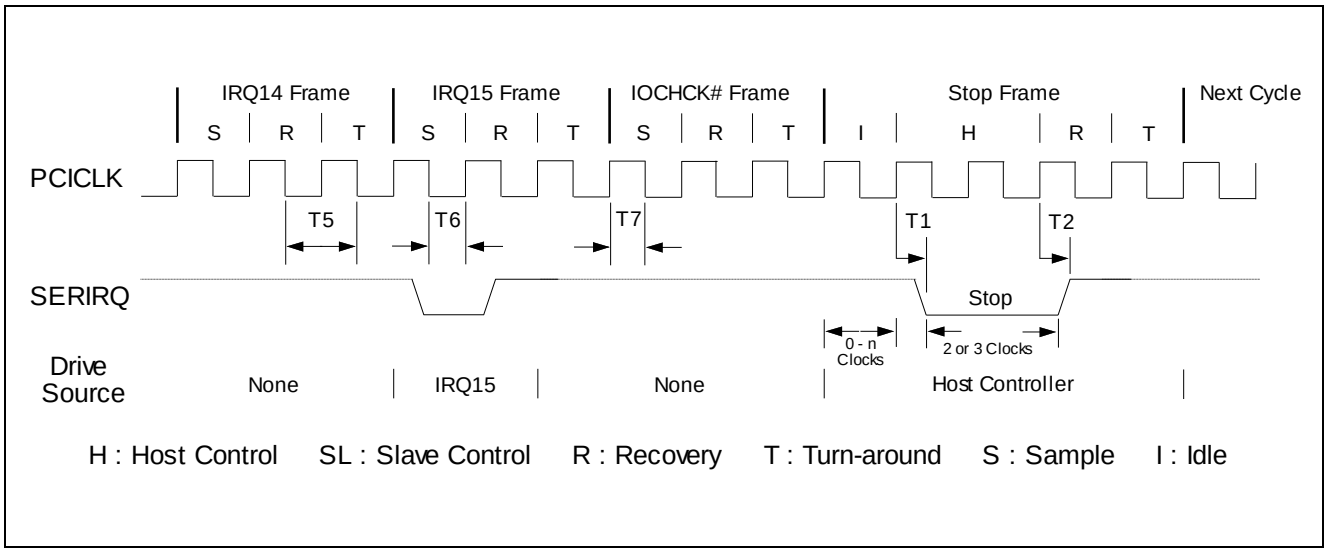
SIRQ interface timing table

Start Frame Timing



SIRQ start frame timing diagram

Stop Frame Timing



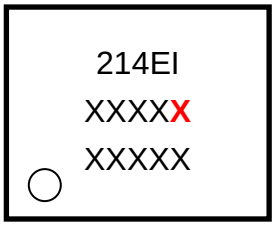
SIRQ stop frame timing diagram

9 Ordering Information

Part Number	Package Type	Production Flow
F81214EN-I	28 pin QFN	-40°C to +85°C

10Top Marking Specification

The version identification is shown as the bold red characters. Please refer to below for detail:



1nd Line: Device Name (214E) + Industrial Item (I).

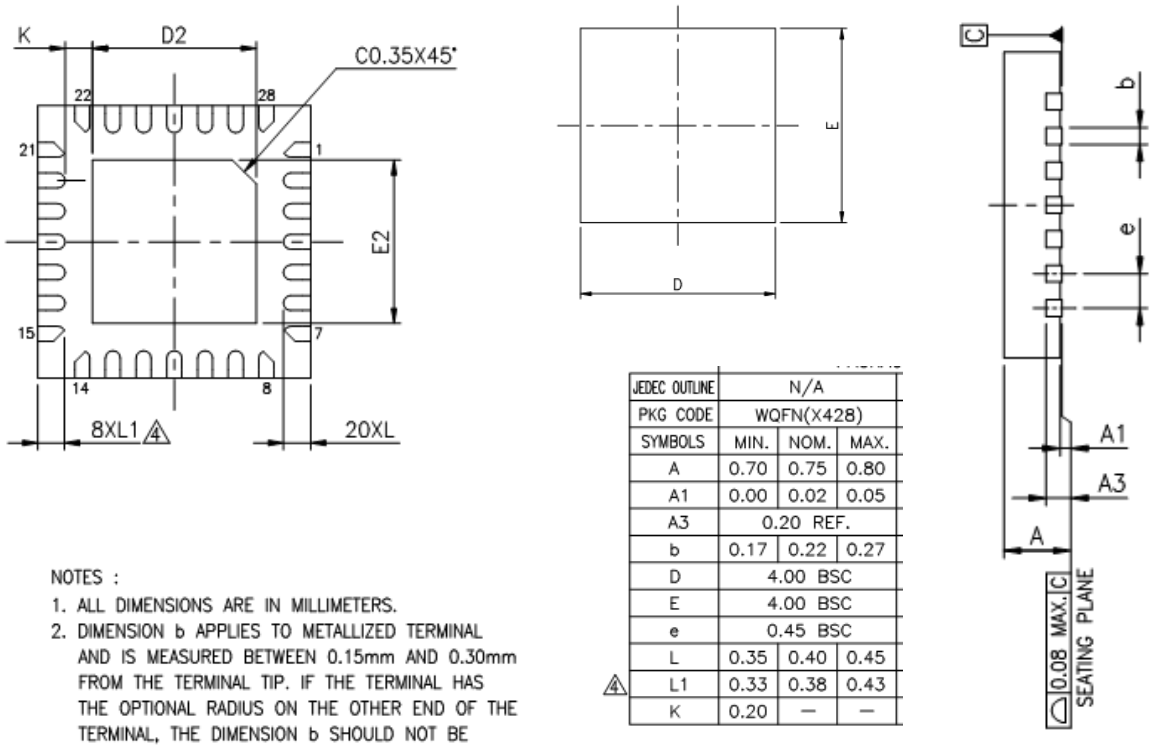
2rdLine:Assembled Year Code (X) + Week Code (XX) + Internal Trace Code (X) + IC Version (X) where “A” means A version, “B” means B version … etc

3thLine: Wafer Lot Number (XXXXX)

◯ : Pin 1 Identifier

11Package Dimensions

28pin-QFN(4mm*4mm)



NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X428)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.17	0.22	0.27
D	4.00 BSC		
E	4.00 BSC		
e	0.45 BSC		
L	0.35	0.40	0.45
④ L1	0.33	0.38	0.43
K	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X114 MIL	2.30	2.40	2.45	2.30	2.40	2.45	V	X	N/A

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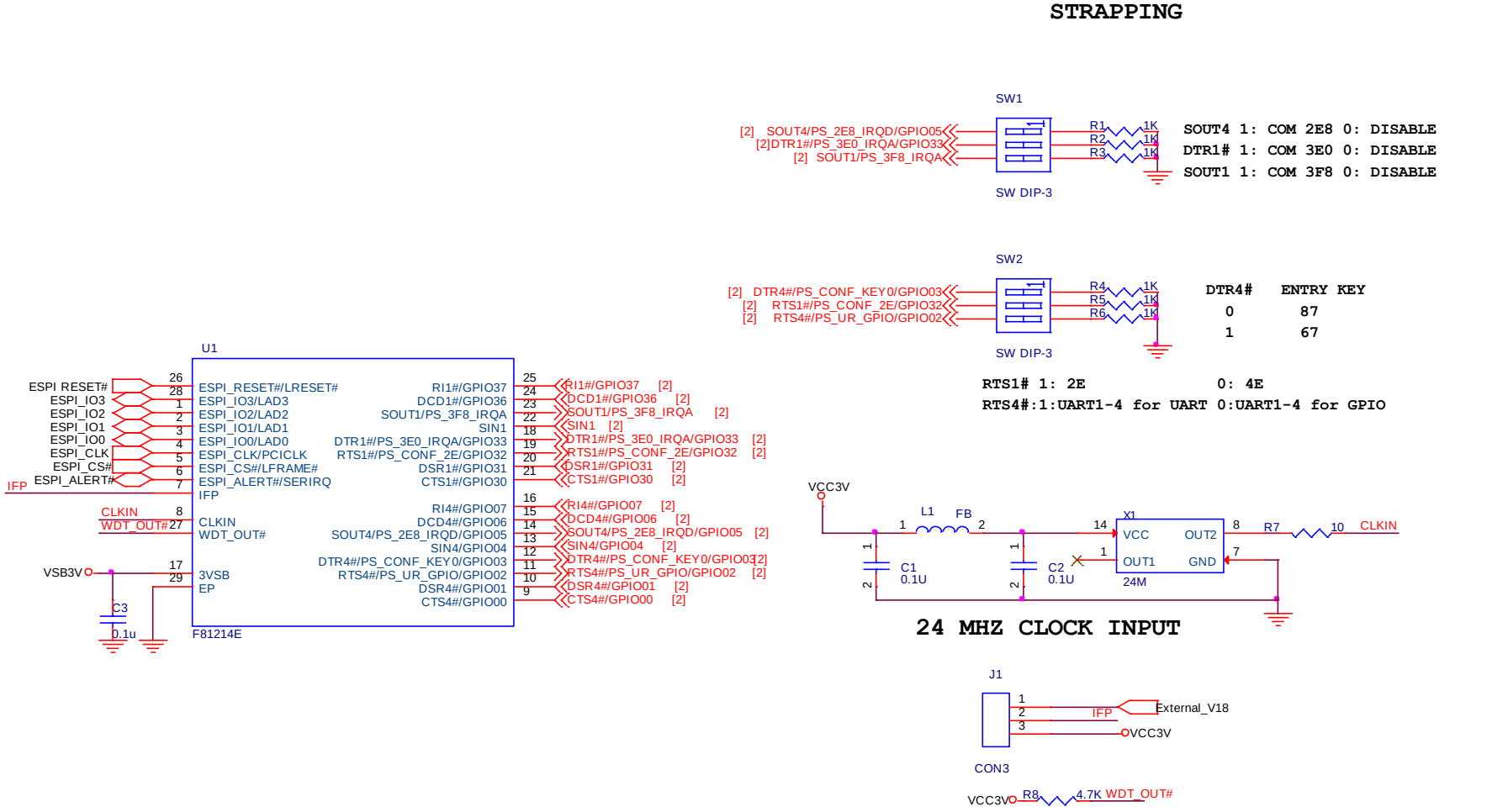
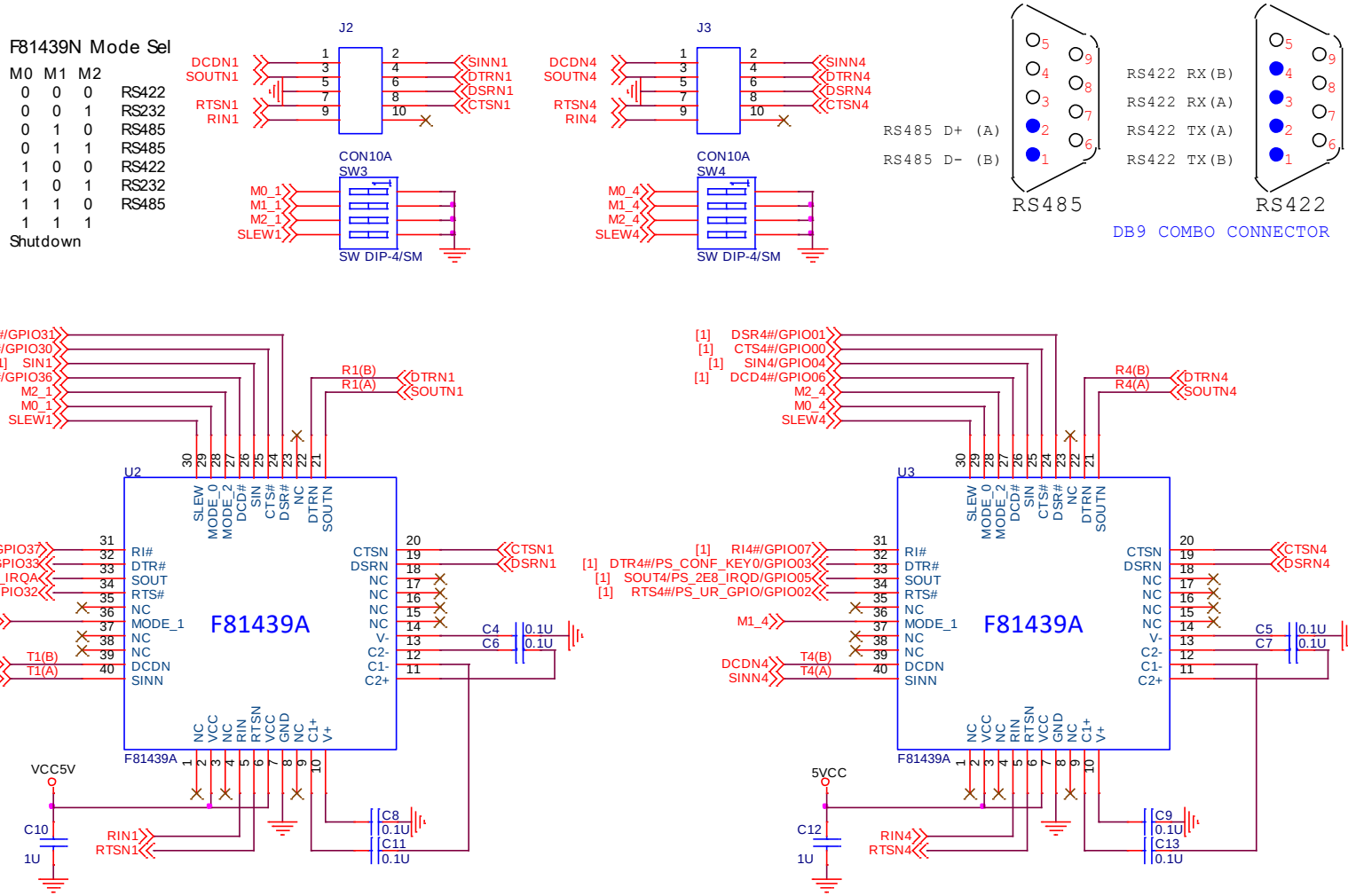
12Application Circuit



Title	F81214E application circuit		
Size A4	Document Number Feature Integration Technology Inc.		Rev 1.0
Date: Tuesday, April 24, 2018	Sheet 1 of 2		



Title	F81214E application circuit		
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May,2020
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