F81251

High Speed CAN Transceiver

Release Date: Feb 2023
Version: V0.16P

F81251 Datasheet Revision History

Version	Date	Revision History
V0.10P	2018/07	Preliminary Version
V0.11P	2019/01	Update Block Diagram Update Function Description Update DC Characteristic Update Absolute Maximum Rating
V0.12P	2019/02	Update Application without SPLIT circuit
V0.13P	2019/05	Update AC Waveform
V0.14P	2020/09	Made Modification & Clarification Update Pin Description Update Electrical Characteristic Update Top Marking Specification Update Application Circuit
V0.15P	2022/08	Made Modification & Clarification Update Electrical Characteristic
V0.16P	2023/02	Made Modification & Clarification

Table of Content

1. General Description

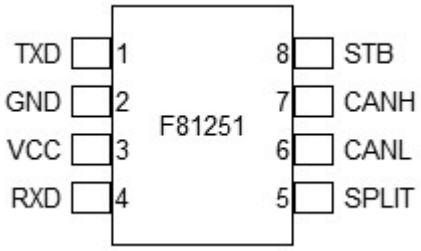
The F81251 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus.

It is primarily intended for high speed applications, up to 1 Mbps, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. The F81251 also features a very low current standby mode with remote wake up capability via the bus.

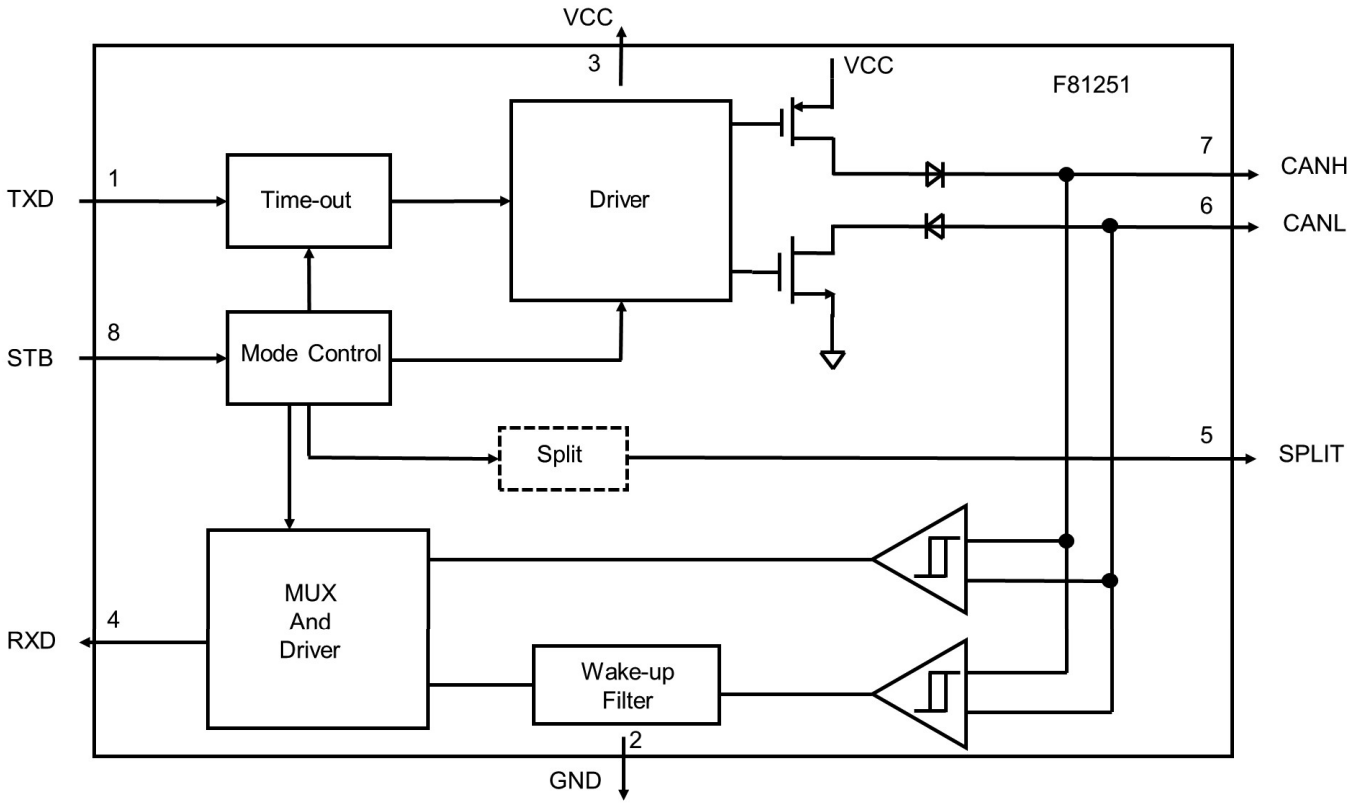
2. Feature List

- Fully compatible with the ISO 11898 standard
- Support High speed up to 1 Mbps
- Very low-current standby mode with remote wake-up capability via the bus
- Differential receiver with high common-mode range for Electro Magnetic Immunity (EMI)
- Transceiver in unpowered state disengages from the bus (zero load)
- Input levels compatible 3.3 V & 5 V devices
- Voltage source for stabilizing the recessive bus level if split termination is used (further improvement of EME)
- At least 110 nodes can be connected
- Transmit Data (TXD) dominant time-out function
- Bus pins protected against transients in automotive environments
- Bus pins and pin SPLIT short-circuit proof to battery and ground
- SOP 8 package
- Operating temperature -40° C to 85° C

3. Pin Configuration



4. Block Diagram



5. Pin Description

I - Input
O - Output
P - Power
AO - Anlog Output
I/O - Input / Output

Pin No.	Pin Name	Type	Description
1	TXD	I	Transmit data input
2	GND	P	Ground supply
3	VCC	P	5V supply voltage
4	RXD	O	Receive data output, reads out data from the bus lines
5	SPLIT	AO	Common-mode stabilization output
6	CANL	I/O	Low level CAN bus line
7	CANH	I/O	High level CAN bus line
8	STB	I/O	Standby mode control pin

6. Functional Description

6.1 Operating modes

The F81251 supports two operating modes, Normal mode and Standby mode, which are selectable via pin STB. See Table 1 for a description of the operating modes under normal supply conditions.

Table1. Operating modes

MODE	PIN STB	PIN RXD	
		LOW	HIGH
Normal	LOW	Bus dominant	Bus recessive
Standby	HIGH	Wake-up request detected	No wake-up request detected

NORMAL MODE

In Normal mode, the transceiver be able to transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD via the multiplexer (MUX). The slope of the output signals on the bus lines is fixed and optimized in a way that lowest Electro Magnetic Emission (EME) is guaranteed.

STANDBY MODE

In Standby mode, the transmitter and receiver are switched off, and the low-power differential receiver will monitor the bus lines. A HIGH level on pin STB activates this low-power receiver and the wake-up filter, and after t_{BUS} the state of the CAN bus is reflected on pin RXD. The system supply current is reduced to a minimum in such a way that Electro Magnetic Immunity (EMI) is guaranteed and a wake-up event on the bus lines will be recognized.

In Standby mode, the bus lines are the bus lines are biased to ground to minimize the system supply current (ICC). A diode is added in series with the high-side driver of pin RXD to prevent a reverse current from pin RXD to VCC in the unpowered state. In normal mode, this diode is bypassed. This diode is not bypassed in standby mode to reduce current consumption.

6.2 Split circuit

SPLIT provides a DC stabilized voltage of 0.5 VCC. It is turned on only in normal mode. In Standby mode, pin SPLIT out is floating. The split circuit can be used to stabilize the recessive common-mode voltage by connecting pin SPLIT to the center tap of the split termination. In case of a recessive bus voltage < 0.5 VCC, due to the presence of an unsupplied transceiver in the network with a significant leakage current from the bus lines to ground, the split circuit will stabilize this recessive voltage to 0.5 VCC. Therefore, a start of transmission does not cause a step in the common-mode signal which would lead to poor Electro Magnetic Emission (EME) behavior.

6.3 Wake-up

In standby mode, the bus lines are monitored via a low-power differential comparator. Once the low-power differential comparator has detected a dominant bus level for more than t_{BUS}, pin RXD will become LOW.

6.4 TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value (tdom), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10K Baud.

6.5 Fail-safe features

Pin TXD provides a pull-up towards VCC in order to force a recessive level in case pin TXD is unsupplied. Pin STB provides a pull-up towards VCC in order to force the transceiver into standby mode in case pin STB is unsupplied. In the event that the VCC is lost, pins TXD, STB and RXD will become floating to prevent reverse supplying conditions via these pins.

7. Electrical Characteristic

7.1. Absolute Maximum Ratings

PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Power Supply Voltage		-0.3	7.0	V
DC Voltage On Pin TXD		-0.3	Vcc+0.3	V
DC Voltage On Pin RXD		-0.3	Vcc+0.3	V
DC Voltage On Pin STB		-0.3	Vcc+0.3	V
DC Voltage On Pin CANH		-27	+40	V
DC Voltage On Pin CANL		-27	+40	V
DC Voltage On Pin SPLIT		-27	+40	V
Electrostatic Discharge Voltage	IEC 61000-4-2, 150 pF, 330 Ω CANH and CANL	-8	+8	KV
	Human Body Model (HBM) 100 pF,1.5 kΩ CANH and CANL	-8	+8	KV
	at any pin pins	-4	+4	KV
	Machine Model (MM) 200 pF, 0.75 μH, 10 Ω at any pin	-200	+200	V
Operating Temperature*		-40	+85	℃
Storage Temperature		-65	+150	℃
Lead Temperature (soldering, 10s)			+300	℃

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

*Design Guarantee

7.2. DC Characteristics

(Ta = 25° C, VCC = 4.75 to 5.25 V, GND = 0V)

Symbol	Parameter	Condition	Min.	Typ.	MAX.	Unit
V_{CC}	Supply Voltage	Operating	4.75		5.25	V
Supply (V_{cc})						
I_{cc}	Supply Current	Standby mode	5	15	20	µA
		Normal mode				
		Recessive; $V_{TXD}=V_{cc}$	2.5	6	10	mA
		Dominant; V_{TXD}=0V	30	35	70	mA
Transmit Data Input (TXD)						
V_{IH}	HIGH-Level Input Voltage		2		V_{CC}+0.3	V
V_{IL}	LOW-Level Input Voltage		-0.3		0.8	V
I_{IH}	HIGH-Level Input Current	$V_{TXD}=V_{CC}$	-5		+5	µA
I_{IL}	LOW-Level Input Current	Normal mode; V_{TXD}=0V	-5	-10	-20	µA
C_i	Input Capacitance	Not tested			10	pF
Standby Mode Control Input (STB)						
V_{IH}	HIGH-Level Input Voltage		2		V_{CC}+0.3	V
V_{IL}	LOW-Level Input Voltage		-0.3		0.8	V
I_{IH}	HIGH-Level Input Current	$V_{STB}=V_{CC}$	-5		+5	µA
I_{IL}	LOW-Level Input Current	V_{STB}=0V	-5	-10	-20	µA
Receive Data Output (Pin RXD)						
V_{OH}	HIGH-Level Input Voltage	Standby Mode; I_{RXD}=-100*u*A	0.8 V_{CC}		V_{CC}	V
I_{OH}	HIGH-Level Output Current	Normal Mode; $V_{RXD}=V_{CC}$-0.4V	1	2		mA
I_{OL}	LOW-Level Output Current	V_{RXD}=0.4V	2	6		mA
Common-Mode Stabilization Output (Pin SPLIT)						
V_O	Output Voltage	Normal Mode; -500*u*A < I_O < +500*u*A	0.3 V_{CC}	0.5 V_{CC}	0.7 V_{CC}	V
$\|I_L\|$	Leakage Current	Standby Mode; -22V < V_{SPLIT} < 35V	0		20	µA
Bus Lines (Pin CANH & CANL)						
$V_{O(dom)}$	Dominant Output Voltage, see Fig 1	V_{TXD} = 0 V				
		pin CANH	3	3.8	4.25	V
		pin CANL	0.5	1.4	1.75	V

$V_{O(dom)(m)}$	Matching Of Dominant Output Voltage (V_{cc}- V_{CANH}- V_{CANL})		-100	0	+150	mV
$V_{O(dif)(bus)}$	Differential Bus Output Voltage (V_{CANH}- V_{CANL})	V_{TXD} = 0 V; dominant; 45 Ω < R_L < 65 Ω	1.5	2.3	3	V
		V_{TXD} = V_{CC}; recessive; no load	-50	0	+50	mV
$V_{O(reces)}$	Recessive Output Voltage, see Fig 1	Normal mode; V_{TXD} = V_{CC}; no load	2	2.5	3	V
		Standby mode; no load	-0.1	0	+0.1	V
$I_{O(sc)}$	Short-Circuit Output Current	V_{TXD} = 0 V pin CANH; V_{CANH} = 0 V pin CANL; V_{CANL} = 40 V	 -40 40	 -50 60	 -95 100	 mA mA
$I_{O(reces)}$	Recessive Output Current	-27 V < V_{CAN} < +32 V	-2.5		+2.5	mA
$V_{dif(th)}$	Differential Receiver Threshold Voltage	-7V ≤ V_{CANH}, V_{CANL} ≤ 12 V Normal Mode (Rise/Fall)	0.5	0.7	0.9	V
		-7V≤ V_{CANH}, V_{CANL} ≤ 12 V Standby Mode	0.4	0.7	1.15	V
$V_{hys(dif)}$	Differential Receiver Hysteresis Voltage	Normal Mode. -7V ≤ V_{CANH} ≤ 12 V -7V ≤ V_{CANL} ≤ 12 V	50		100	mV
I_{LI}	Input Leakage Current	V_{CC} = 0 V; V_{CANH} = V_{CANL} = 5 V	-5		+5	μA
$R_{i(cm)}$	Common-Mode Input Resistance		6	25	50	kΩ
$R_{i(cm)(m)}$	Common-Mode Input Resistance Matching	V_{CANH} = V_{CANL}	-3		+3	%
$R_{i(dif)}$	Differential Input Resistance	Standby Or Normal Mode	12	50	100	kΩ
$C_{i(cm)}$	Common-Mode Input Capacitance	V_{TXD} = V_{CC}; Not Tested			20	pF
$C_{i(dif)}$	Differential Input Capacitance	V_{TXD} = V_{CC}; Not Tested			10	pF

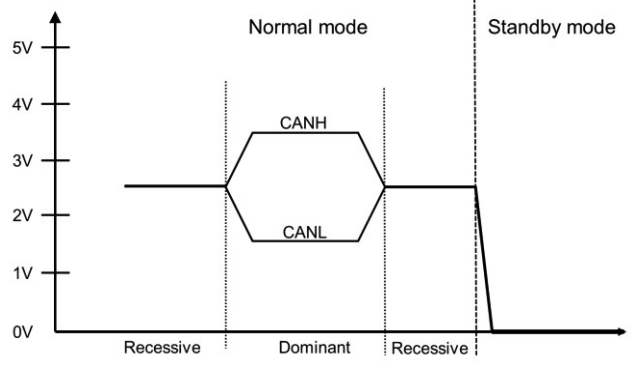


Fig 1. Normal & Standby Mode Waveform

7.3. AC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	MAX.	Unit
Timing Characteristics (see Fig 2)						
$t_{d(TXD-BUSon)}$	Delay TXD To Bus Active	Normal Mode	25	60	110	ns
$t_{d(TXD-BUSoff)}$	Delay TXD To Bus Inactive		10	80	95	ns
$t_{d(BUSon-RXD)}$	Delay Bus Active To RXD		10	50	115	ns
$t_{d(BUSoff-RXD)}$	Delay Bus Inactive To RXD		35	50	160	ns
$t_{PD((TXD-RXD)}$	Propagation Delay TXD To RXD	V_{STB}=0V (Rise/Fall)	40		255	ns
$t_{dom(TXD)}$	TXD Dominant Time-Out	V_{TXD}=0V	600	1400	2000	µs
t_{BUS}	Dominant Time For Wake-Up Via Bus	Standby Mode	0.75	1.75	5	µs
$t_{d(stb-norm)}$	Delay Standby Mode To Normal Mode	Normal Mode		1.5	10	µs

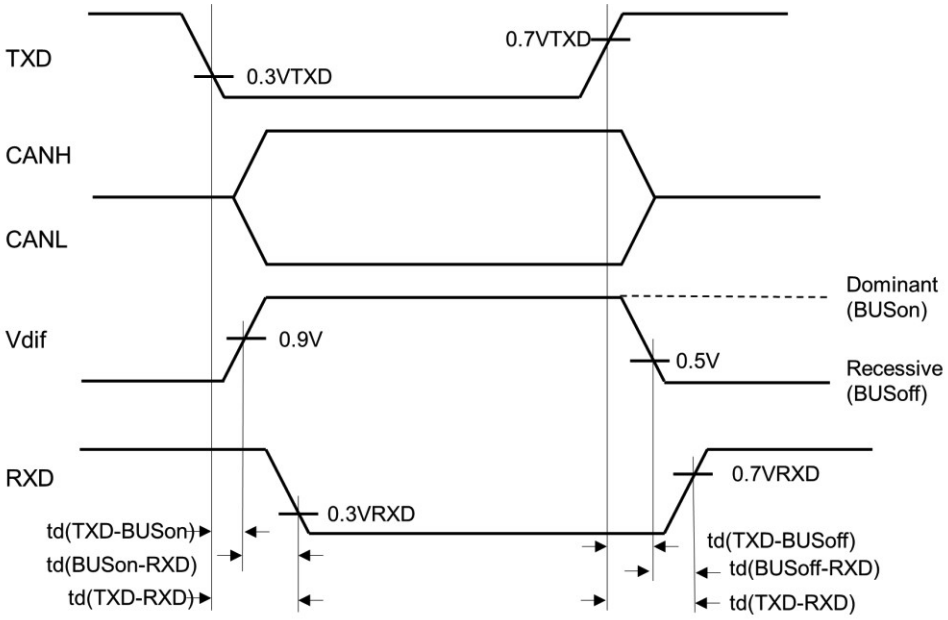


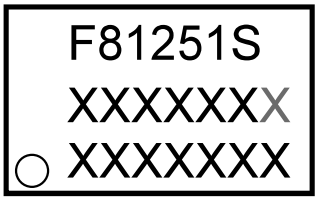
Fig 2. Timing Waveform

8. Ordering Information

Part Number	Package Type	MSL
F81251S	8 pin SOP (150 mil)	3

9. Top Marking Specification

The version identification is shown as the bold red characters. Please refer to below for detail:



1st Line: Device Name: F81251S

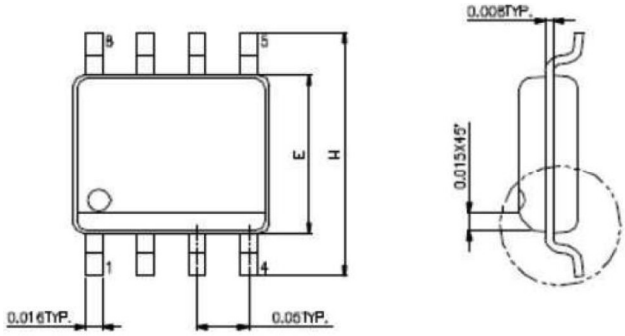
2nd Line: Assembly Plant Code (x) + Assembled Year Code (x) + Week Code (xx) + Fintek Internal Code (xx) + **IC Version (x)** where A means version A, B means version B, …

3rd Line: Wafer Lot Number (XXXX…XX)

○: Pin 1 Identifier

10. Package Dimensions

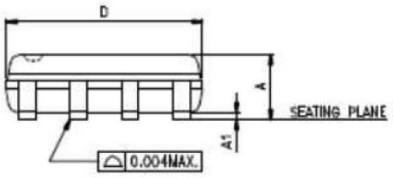
SOP8, 150 mil

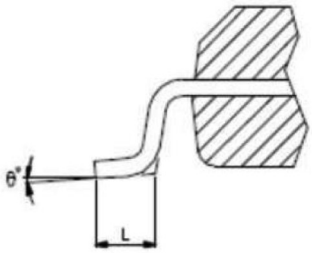


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AA / E.P. VERSION : N/A
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.





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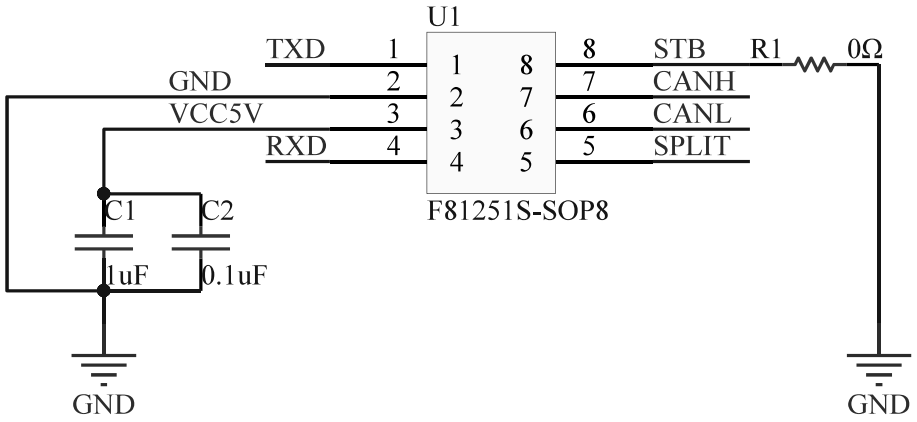
11. Application Circuit



SPLIT:
It can help to stabilize the recessive voltage on the bus. Using the SPLIT pin in conjunction with a spilt termination network.
It is turned on only in normal mode. In standby mode pin SPLIT is floating.