FPD23DAEVM User's Guide

User's Guide

Literature Number: SNLU144
may 2013

Introduction

1.1 FPD23DAEVM

FPD23DAEVM is designed to directly adapt to one of the following types of RGB data and source HDMI/DVI compatible video output.

- FPD-Link I (Four LVDS data/control streams and one LVDS clock pair)
  OR
- Parallel LVCMOS (RGB888) signals and clock.

Hence, it act as a powerful tool to evaluate performance of **FPD-Link II/III Serial link Devices**.

The adapter has an on board *PanelBus* Digital Transmitter, TFP410 which is DVI 1.0-compliant solution. DVI and HDMI have the same electrical specifications for their TMDS and VESA/DDC links, output of TFP410 is routed to 19-pin HDMI type-A connector. Hence, hooking up this board with one of the deserializer in FPD-Link II/III family allows evaluation of the serial link through direct observation of the video data on HDMI/DVI compatible display.

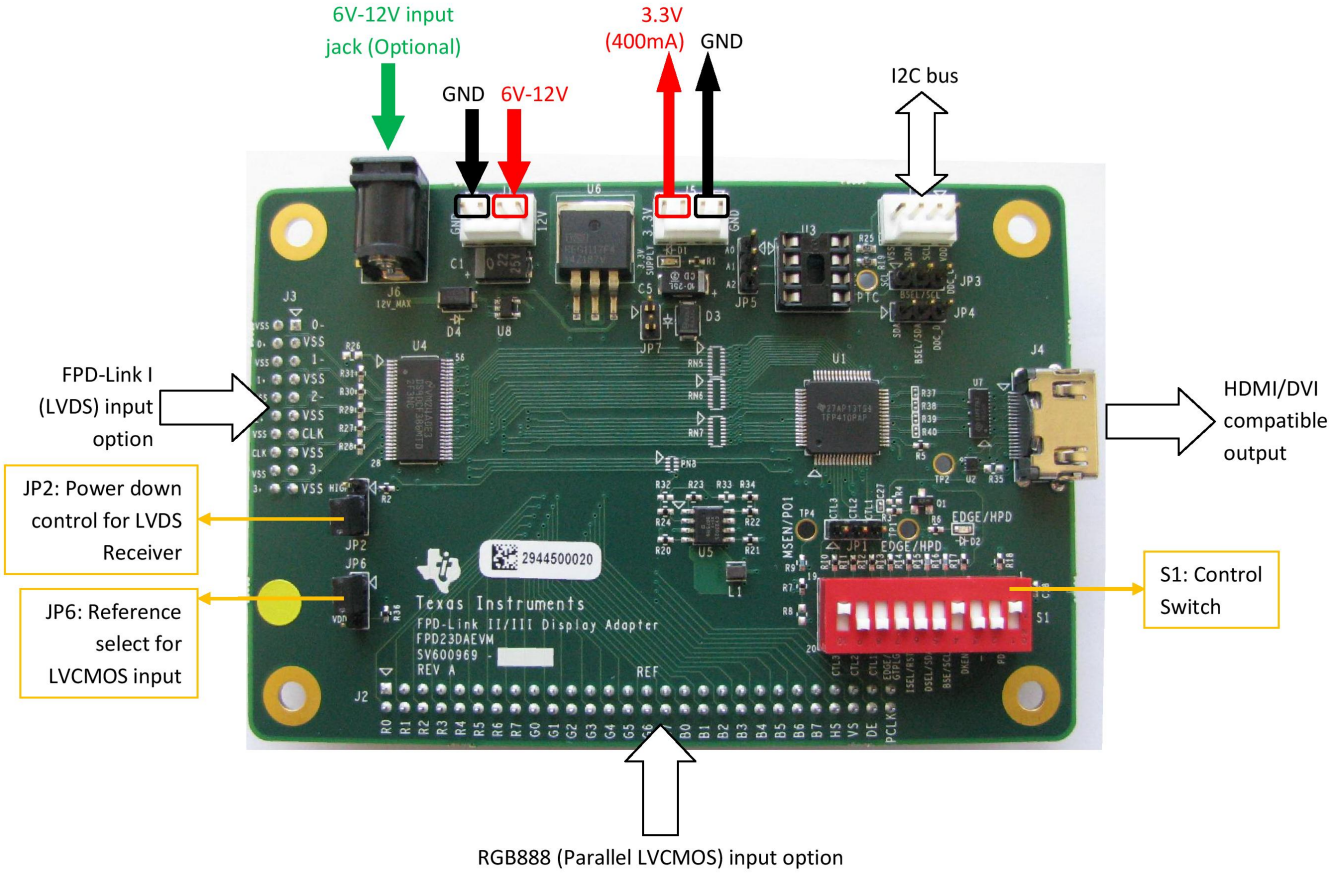

Figure 1-1. FPD-Link II/III Display Adapter

FPD23DAEVM contains FPD-Link II/III Display Adapter board only. (1)

(1) Other components required: 12V DC Supply, an HDMI cable or HDMI to DVI adapter cable, an HDMI or DVI compatible display.

1.2 FPD23DAEVM Features

1. *PanelBus* Digital Transmitter, TFP410 supports flat panel display resolutions up to UXGA and maximum pixel rate of 165 MHz in 24-bit true color pixel format.
2. It can accept FPD-Link I input or parallel LVCMOS (RGB888) input based on a simple set of hardware configuration.
3. Although designed to be used with an HDMI cable, it is easy to hook up the output to DVI display using an HDMI to DVI adapter cable.
4. Once a DC supply of 12V (recommended current limit is 500mA) is connected to FPD23DAEVM, it can supply 3.3V (400mA) DC to other devices used in the system such as deserializer.
5. Optionally, PCF8582C-2 can be populated, which is connected to on board I2C bus and allows implementation of EDID.
6. TFP410 allows minimization of the skew between parallel RGB data and clock signal through a control switch (S1).
7. TPD8S009 and TPD4E001 provide ESD protection at the output for display port.

1.3 Typical Application

Figure 1-2 below illustrates a typical setup for FPD23DAEVM with either FPD-Link I source or parallel LVCMOS (RGB888) as a source for RGB data and clock signals. These signals are then translated into TMDS for transmission over HDMI cable.

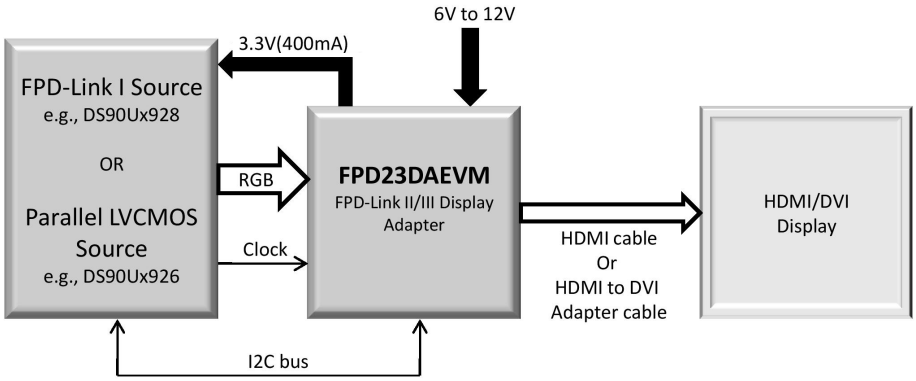

Figure 1-2. Typical Application/Evaluation Configuration

Quick Start Guide

This chapter provides minimal steps required to setup FPD23DAEVM in the two hardware configuration depending upon the type of input signals. Switch and jumper position required for this operation have been set at the factory.

1. Verify the factory settings for the adapter board as shown in Figure 2-1 and Figure 2-2.
2. Connect either FPD-Link I input to J3 or parallel LVCMOS (RGB888) input to J2. Make sure that board is configured for corresponding input type, refer to Section 2.1 and Section 2.2.
3. Connect 12V power supply to either J6 or J1 as shown in . LED D1(green) indicates that board is correctly powered up and 3.3V(200mA) supply is available at J5.
4. Connect an HDMI/DVI compatible display device to J4 using an HDMI cable. Desired results can be observed on the display. (2)

2.1 Board Setup with FPD-Link input

In this configuration, connect input to J3 and instructions below should be followed,

1. Make sure RN5, RN6, RN7 and RN8 are mounted.
2. To avoid stubs, RN1, RN2, RN3 and RN4 should not be mounted.
3. Verify pin HIGH and PDN to be shorted on JP2 while using FPD-Link I input.

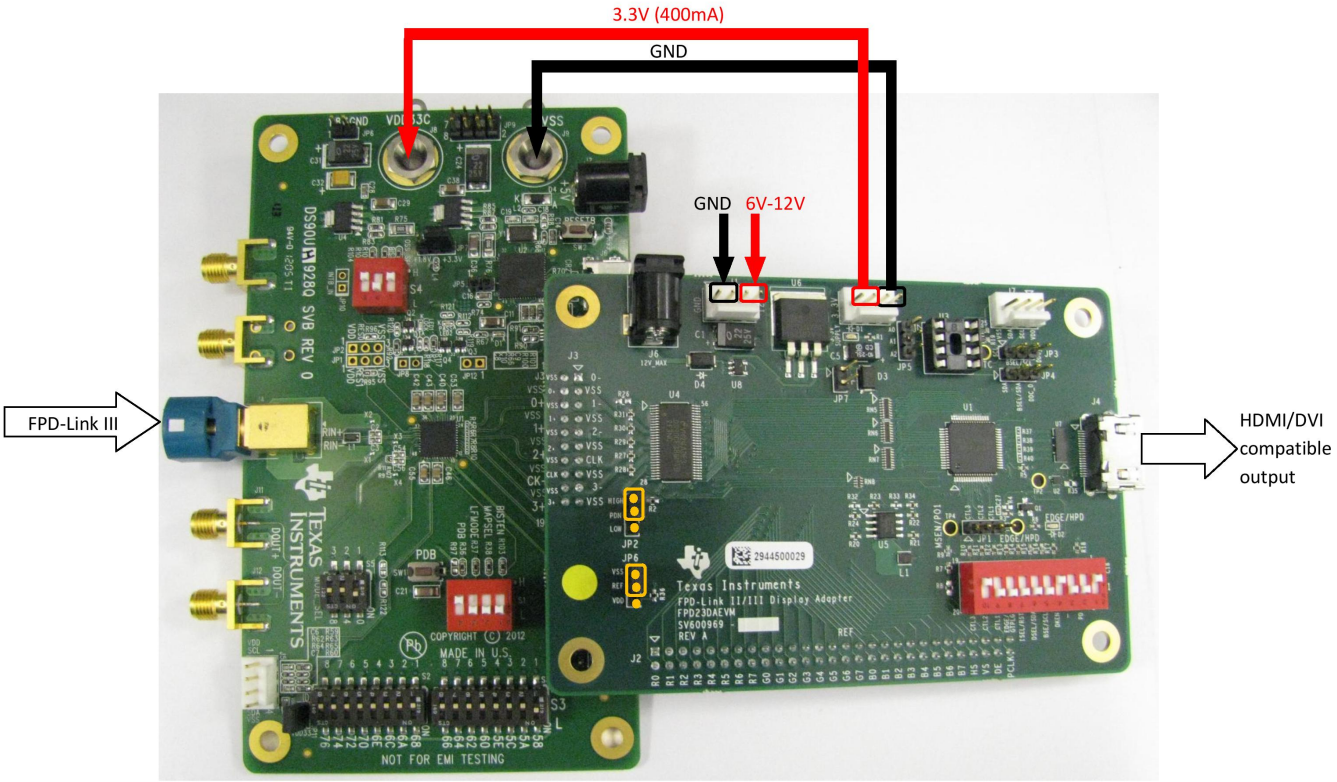

Figure 2-1. FPD23DAEVM with FPD-Link input

(2) MSEN/PO1 signal on TP4 should be high, once the display/receiver connected to J4 is detected properly.

2.2 Board Setup with Parallel LVCMOS input

In this configuration connect input to J2 and instructions below should be followed,

1. Make sure RN1, RN2, RN3 and RN4 are mounted.
2. RN5, RN6, RN7 and RN8 should not be mounted to avoid stubs.
3. Verify pin VSS and REF to be shorted on JP6 while using RGB888 parallel LVCMOS input.

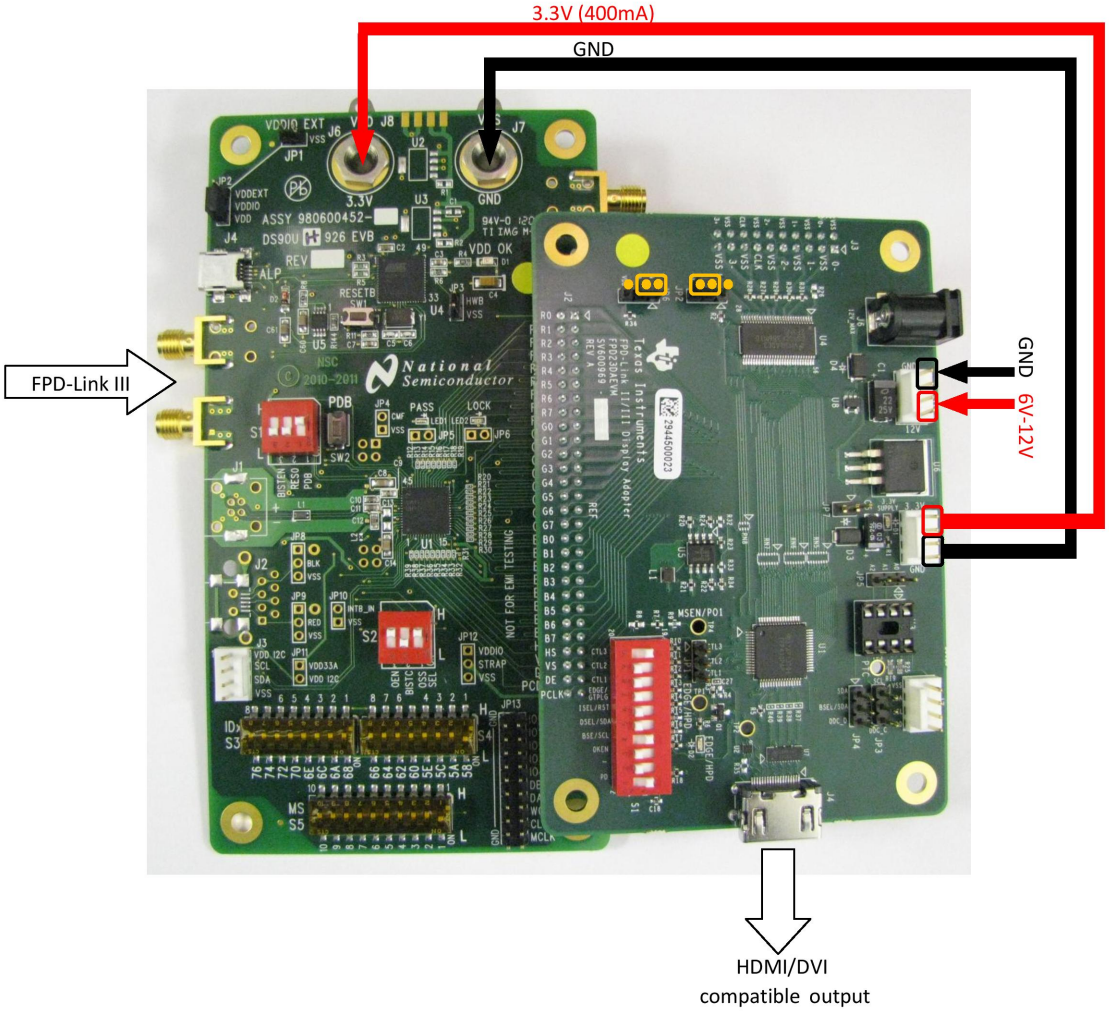

Figure 2-2. FPD23DAEVM with Parallel LVCMOS input

Evaluation Hardware Overview

FPD23DAEVM includes circuits and interfaces facilitating the full control over the devices present on the board.

3.1 Power

FPD23DAEVM can be powered up by 6V(min) to 12V(max) DC supply as detailed in Figure 2-1 and Figure 2-2. **Apply power to only ONE of these ports: J1 or J6.**

Table 3-1. Power

Reference	Description and Default settings
J1	**12V power port** Do not apply more than 12V and less than 6V DCsupply to this port.
J6	**12V power jack** Do not apply more than 12V and less than 6V DCsupply to this port.
J5	**3.3V power port** This port can be used to power up the Deserializer board to which the adapter is connected. It can source up to 400mA of current.

3.2 Video Data Input

As mentioned earlier, there two input options available.

NOTE: To ensure electrical signal compatibility,

1. Board is by default configured for LVCMOS threshold of $V_{IH(min)}$= 2.31V and $V_{IL(max)}$= 0.99V for the PanelBus Transmitter, TFP410. This allows using this board with deserializer VDDIO = 3.3V.
2. To work with low signal swings (with deserializer VDDIO = 1.8V), change R7 to 40kΩ and R8 to 15kΩ. This hardware change corresponds to $V_{IH(min)}$= 1.1V and $V_{IL(max)}$= 0.7V.

3.2.1 FPD-Link Video Data Input

Header J3 (mounted on bottom side) accepts a 20-pin IDC or similar 0.1" spaced male header. Connect the clock and 4 FPD-Link (LVDS) data pairs to this header as marked on the silk screen. 100Ω differential termination is provided on the board near DS90CF386 (U4) device pins.

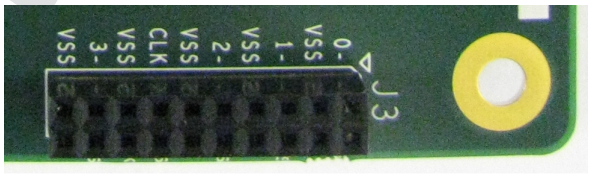

Figure 3-1. FPD-Link Input header: J3

3.2.2 Parallel LVCMOS Video Data Input

Header J2 (mounted on bottom side) accepts R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK as inputs. The even numbered pins are the inputs. The odd numbered pins are connected to REF (pin 2 of JP6). Jumper JP6 is factory set to select VSS as a reference.

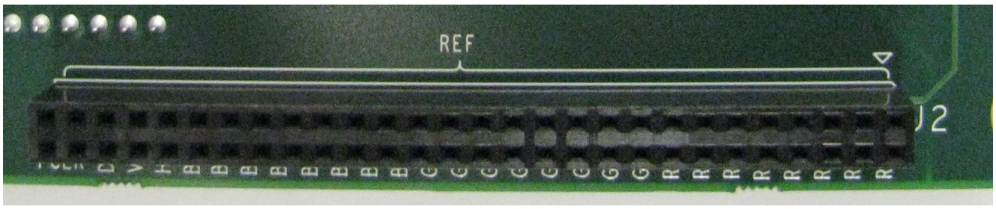

Figure 3-2. Parallel LVCMOS Input header: J2

3.3 Video Output

Connect an HDMI cable between connector J4 and an HDMI display OR
An HDMI to DVI adapter cable can be used to connect to a DVI display.

3.4 Hardware controls

Hardware controls present on the board determines the specific mode or state of operation.

Table 3-2. Description : Control element

Reference	Description and Default settings
JP1	Allows access to multifunction input (pin 6, 7, 8) of TFP410. For more details on function of these pin, refer Table 3-3 and device datasheet. Default : CTL[3:1] = 100 To pull these pins High or Low, switch S1 can be used.
JP2	Connected to PDN pin of DS90CF386. HIGH: DS90CF386 CMOS output will be switching. (This condition is required while using FPD-Link I input) LOW: DS90CF386 CMOS output will be low.
JP3	I2C clock port Allows access to SCL pin of TFP410(U1), U3 and DDC_C (1).
JP4	I2C serial data port Allows access to SDA pin of TFP410(U1), U3 and DDC_D (2).
JP5	Address select port for U3 It allows to select an appropriate address for U3 (PCF8582C-2, not provided) in the range 0x50 to 0x57. Default : floating
JP6	To select appropriate reference for LVCMOS inputs. Default : LVCMOS inputs refer to VSS. It also allows strapping of parallel LVCMOS input connector pins.
JP7	Allows shorting schottky diode D3, if required. Default : Open
S1	This switch controls the operation of TFP410 PanelBus digital transmitter only and the default settings are listed below, S1.10 : CTL3 : HIGH, Default de-skew settings, although de-skew is disabled. S1.9 : CTL2 : LOW, Default de-skew settings, although de-skew is disabled. S1.8 : CTL1 : LOW, Default de-skew settings, although de-skew is disabled. S1.7 : EDGE/HTPLG : LOW, Falling edge of input clock IDCK+ selected for primary latch to occur S1.6 : ISEL/RST : LOW, I2C disabled S1.5 : DSEL/SDA : LOW, Single ended input clock mode S1.4 : BSEL/SCL : HIGH, 24-bit, single edge input mode S1.3 : DKEN : LOW, De-skew disabled S1.2 : NONE : LOW, not used S1.1 : PD : HIGH, TFP410 is in normal operation mode Refer Table 3-3 for detailed description of TFP410 control associated with this switch.

(1) Pull up is not present for DDC_C pin.
(2) Pull up is not present for DDC_D pin.

Table 3-3 below describes function of switch S1 in more detail.

Table 3-3. Switch S1 Functions

Switch position	Control	Description	
		I2C Disabled (ISEL/$\overline{RST}$= LOW)	I2C Enabled (ISEL/$\overline{RST}$= HIGH)
S1.10 S1.9 S1.8	CTL3 CTL2 CTL1	When De-skew mode is disabled (DKEN= LOW), CTL2 & CTL1 can be used to send additional information across the DVI link during blanking interval (DE= LOW). When De-skew mode is enabled (DKEN= HIGH), these 3 inputs become DK[3:1], used to adjust the setup and hold times of the pixel data inputs relative to IDCK+. Refer device datasheet for more details.	Acts as 3 LSBs of the 7 bit I2C address of TFP410, A[3:1]=000 to select 7 bit I2C address as 0x38 through A[3:1]=111 for 0x3F. Based on read or write operation 1 or 0 is appended to form the 8 bit I2C address, refer device datasheet for more details.
S1.7	EDGE/HTPLG	HIGH : Primary latch occurs on the rising edge of IDCK+ LOW : Primary latch occurs on the falling edge of IDCK+ Make sure that R13 is mounted and R4 is not mounted for the operation.	Used to monitor the hot plug detect signal. Make sure that R4 is mounted, R13 is not mounted and S1.7 is set HIGH for the operation.
S1.6	ISEL/$\overline{RST}$	LOW : I2C disabled	HIGH : I2C enabled
S1.5	DSEL/SDA	Depends upon VREF and BSEL, refer TFP410 device datasheet.	This switch should be positioned high for the external pull up on SDA line.
S1.4	BSEL/SCL	HIGH : selects 24-bit input, single ended input mode. LOW : selects 12-bit input, dual edge input mode.	This switch should be positioned high for the external pull up on SCL line.
S1.3	DKEN	HIGH : Enables de-skew with the trim increment selected through S1.10, S1.9, S1.8 LOW : Disables de-skew and default trim setting is used	This pin should be tied either to GND or to VDD and avoid floating input. De-skew function can be accessed through I2C.
S1.2	Not used	-	-
S1.1	$\overline{PD}$	HIGH : Normal operating mode LOW : Power down mode	In this mode, $\overline{PD}$ pin should be tied to GND. Power down state is selected through I2C and default mode is Power down.

3.5 Indicators and Test points

Table 3-4. Description : Indicators and Test points

Reference	Description
D1	**3.3V LDO supply indicator : Green LED**
D2 **TP1**	**Hot plug detect / Edge Select : Red LED** • By default (I2C disabled on TFP410), it will indicate the status of the input clock (IDCK+) edge selected (though S1.7) for primary latch on TFP410, HIGH : Rising edge LOW : Falling edge (default) Make sure that R13 is mounted and R4 is not mounted for the operation. • When I2C enabled, it indicates hot plug detect signal status. Make sure that R4 is mounted, R13 is not mounted and S1.7 is set high for the operation.
TP2	**HDMI CEC pin test point**
TP3	**Programming time control output of U3**
TP4	**Monitor sense/ programmable output of TFP410** • When I2C is disabled, HIGH level on this pin indicates a receiver is detected at the differential outputs, Low level indicates a power on receiver is not detected • When I2C is enabled, this output is programmable through I2C interface, refer TFP410 device datasheet for more details.

3.6 I2C and Device Addressing (1)

FPD23DAEVM provides flexibility to configure I2C bus as per the requirement.

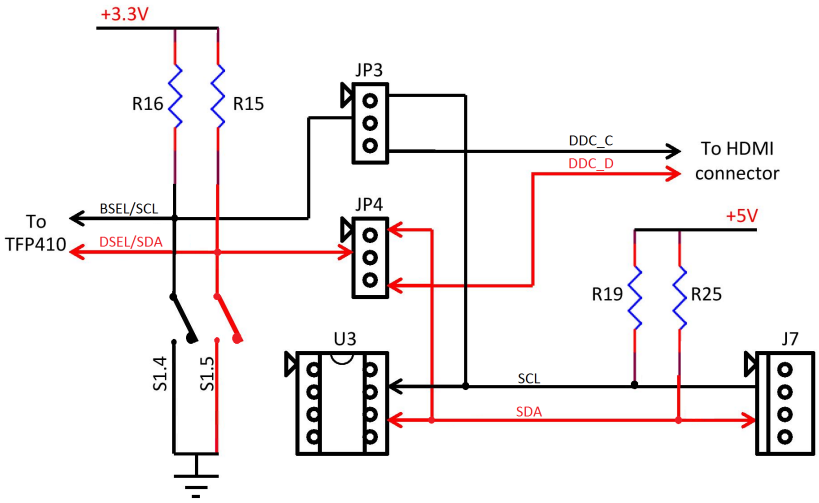

Figure 3-3. I2C and Device Addressing

1. Header J7 is directly connected to U3 as shown in Figure 3-3, which allows implementation of external EDID (2) (it requires mounting PCF8582C-2 on board). When 12V is supplied to the EVM, SCL and SDA lines are pulled high to 5V by resistor R19 and R25 on the board.
   The SCL and SDA lines are also connected to pin 1 of JP3 and JP4 respectively.
   I2C device address of U3 can be configured by connecting the JP5 pins to either VSS or VDD. Refer PCF8582C-2 device datasheet for more details.
2. Pin2 of JP3 and JP4 are connected to BSEL/SCL and DSEL/SDA pins of U1, TFP410. Note that, to communicate with TFP410 over I2C proper settings are required on switch S1. Refer Table 3-3.
3. Pin3 of JP3 and JP4 are connected to DDC_C and DDC_D lines from the HDMI connector, J4. This might be useful while using the actual EDID of the display.

(1) Unless resistor R19 and R25 are removed, do not put jumper across pin 1 and 2 of either JP3 or JP4. This may damage TFP410 on the board.

(2) EDID (Extended Display Identification Data) is a display's feature of describing its identity and capabilities to the source, e.g.: video formats, audio formats, colorimetry, lip-sync delays, etc.

Using Internal Test Pattern Generation of 720p FPD-Link III Devices

This section provides basic steps to use Internal Test Pattern Generator of 720p FPD-Link III devices to observe the output on HDMI/DVI compatible display through FPD23DAEVM.

ALP provides an interactive GUI to control the internal pattern generator of DS90Ux92x family of devices as shown below.

Here, a specific example of DS90UH925 & DS90UH926 serial link is considered, however similar procedure applies to other members of DS90Ux92x family.

1. Connect USB cable to DS90UH925QSEVB and launch ALP. Once DS90UH925 is detected by the software as shown in Figure 4-1, click on the device name and select **Pattern Generator** tab.

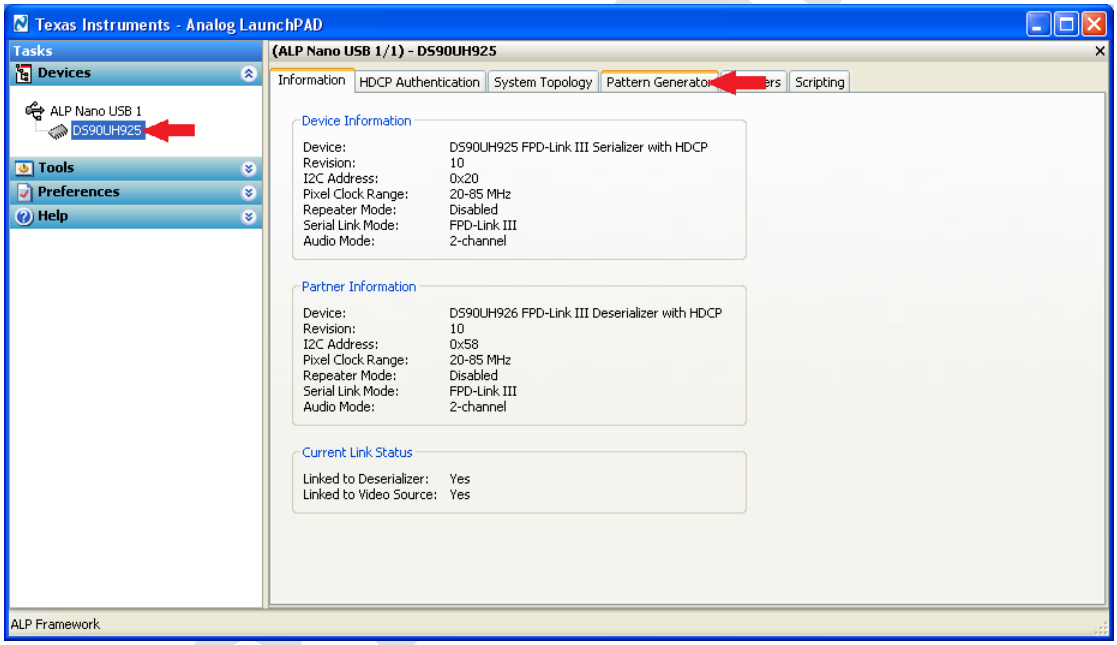

Figure 4-1. Initial Window

2. Under **Video Control**, select **Timing source** as **Internal** or **Internal w/Ext. Clock** as shown in Figure 4-2.

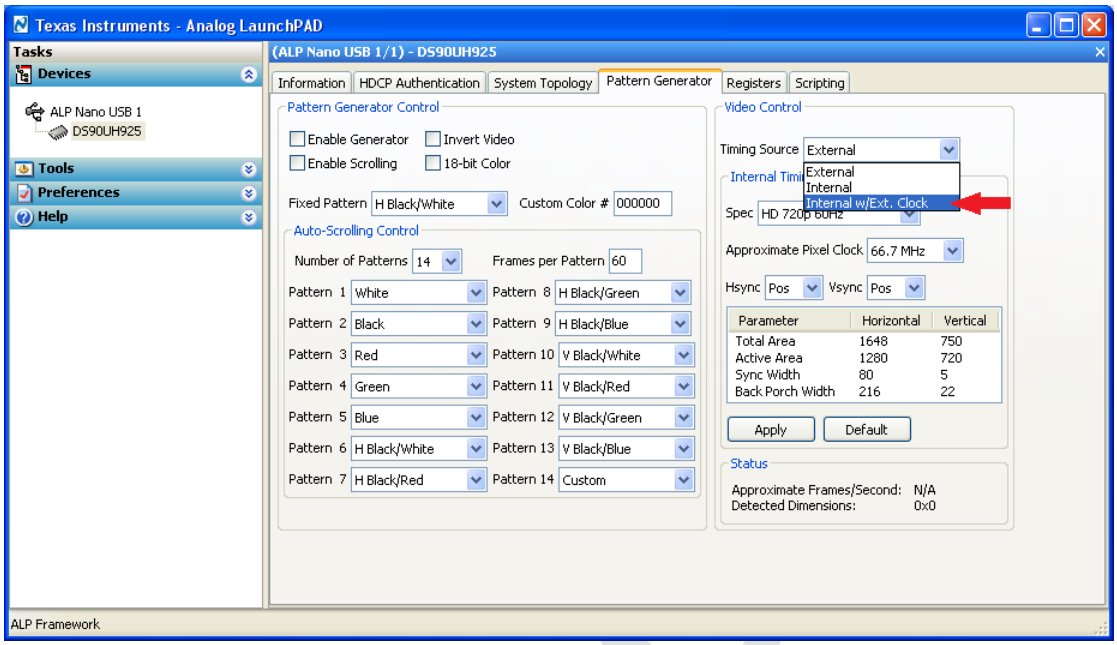

Figure 4-2. Timing Source (4) (5)

3. Under **Internal Timing> Spec**, select appropriate option depending upon the type of display.

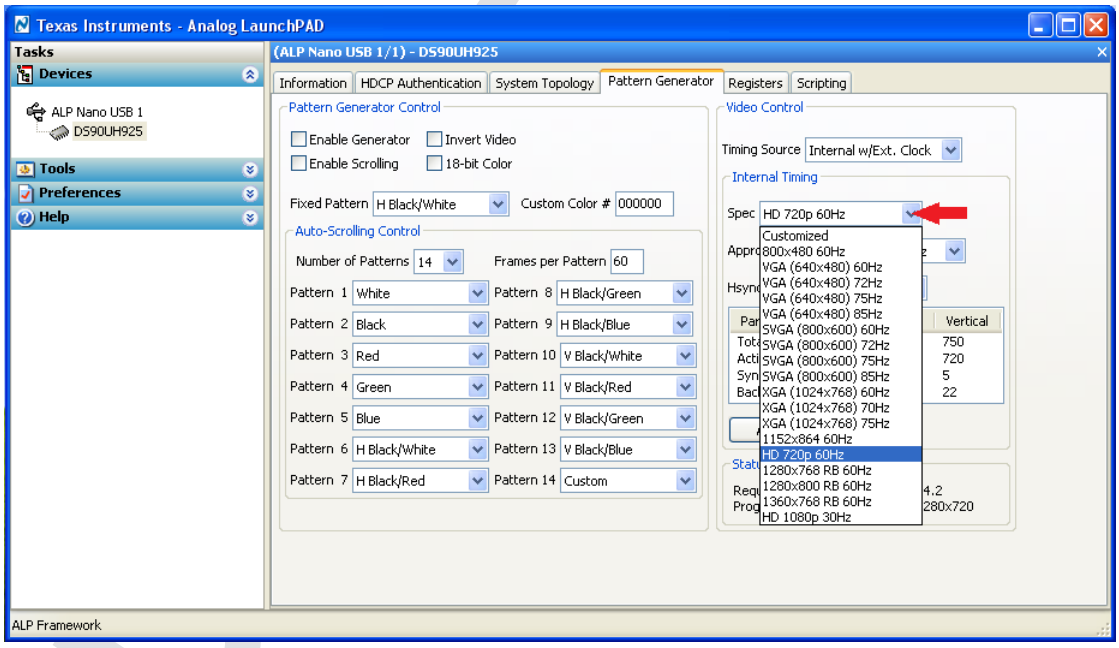

Figure 4-3. Internal Timing : Spec

(4) In **Internal w/Ext. Clock** mode, external PCLK is required on Serializer, all other signals are generated by the device itself.

(5) In **Internal** mode, all signals including PCLK are generated by the device itself.

4. If Timing Source is selected as **Internal**, it is required to select **Approximate Pixel Clock** which is within acceptable range of PCLK of the display device connected.

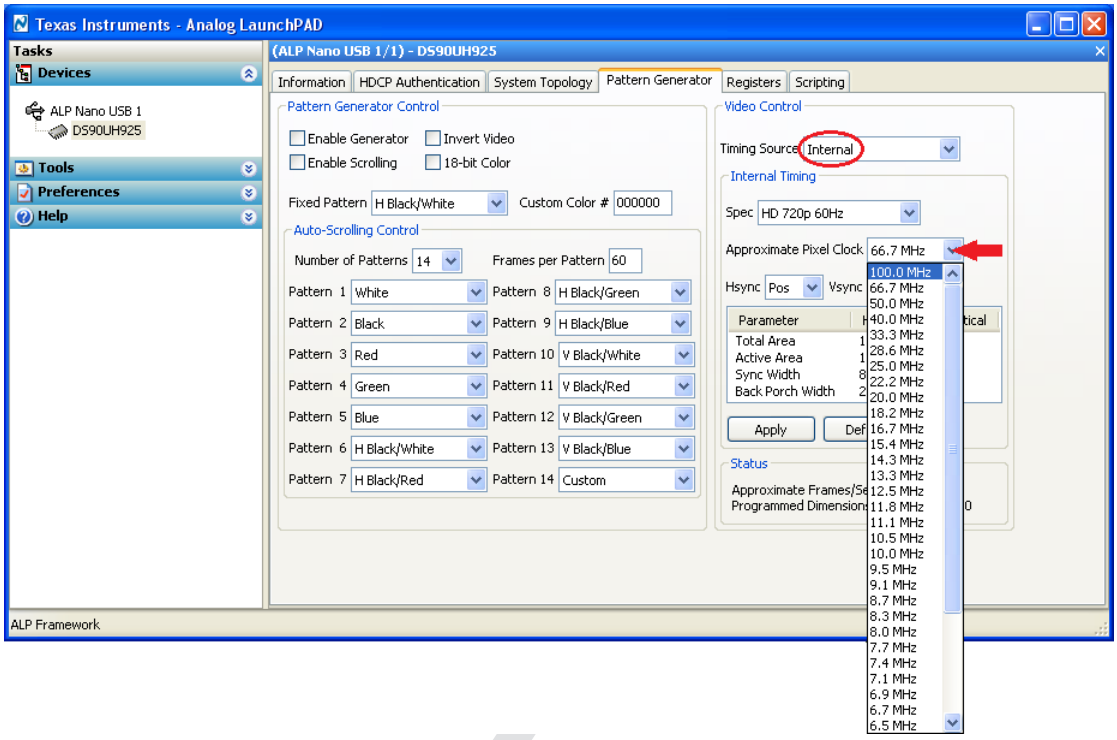

Figure 4-4. Approximate Pixel Clock

5. Finally, check on **Enable Generator** and observe the output on display. Optionally, **Enable Scrolling** to view changing patterns on the display.

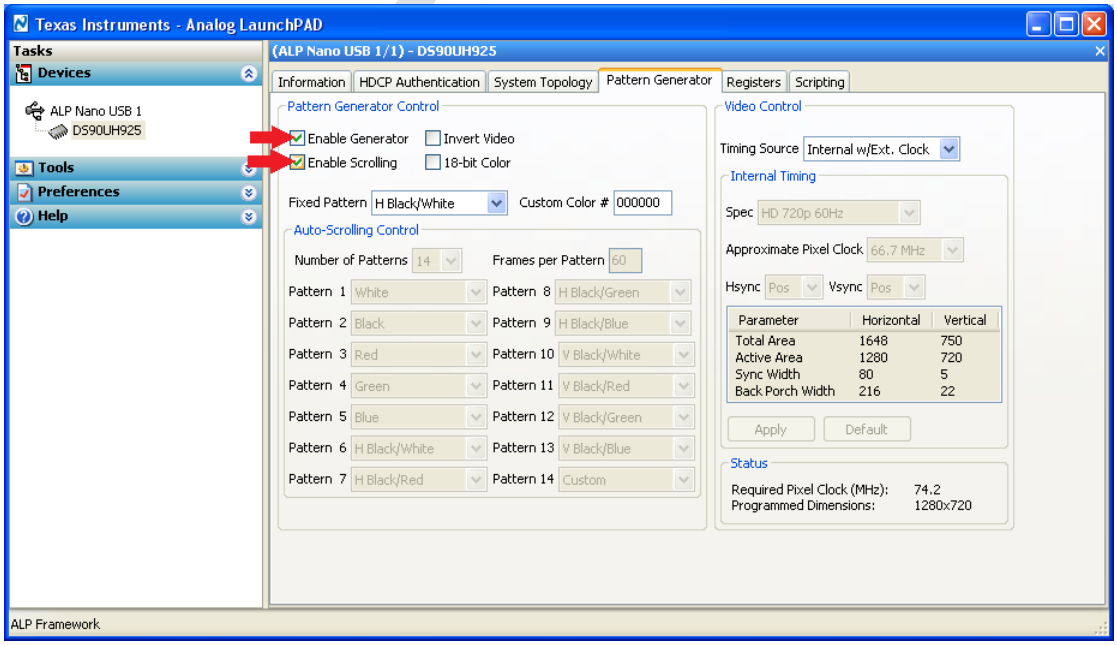

Figure 4-5. Enable Generator and Scrolling

Board Schematic

A.1 Board Stackup

	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Dielectric constant	Copper Plating Thickness (mils)	Thickness after lamination (mils)
Soldermask											0.80
	Signal	H	32			Foil				1.40	2.00
				Press thk = 4.50 mil		Prepreg	106(75)	PCL-370HR	3.9		4.50
							106(75)	PCL-370HR	3.9		
	Plane	1.0	100								1.20
	Blank / Targets										
				14.0 mil 1/—		Core		PCL-370HR	3.9		14.00
				Press thk = 16.90 mil		Prepreg	1080(65)	PCL-370HR	3.9		16.90
							2113(58)	PCL-370HR	3.9		
							2113(58)	PCL-370HR	3.9		
							2113(58)	PCL-370HR	3.9		
							1080(65)	PCL-370HR	3.9		
	Blank / Targets										
				14.0 mil —/1		Core		PCL-370HR	3.9		14.00
	Plane	1.0	100								1.20
				Press thk = 4.50 mil		Prepreg	106(75)	PCL-370HR	3.9		4.50
							106(75)	PCL-370HR	3.9		
	Signal	H	30			Foil				1.40	2.00
Soldermask											0.80

Specification (Over mask on plated copper:):	mil	Anticipated Board Thickness:	mil
Overall Board Thickness:	62.0	After lamination:	57.3
Tolerance:	+6.2/-6.2	Over mask on plated copper::	61.7
Min-Max Board Thickness:	55.8-68.2		

Impedance Table

Layer	Impedance Requirement [ohms]	Tolerance [ohms] +	Tolerance [ohms] -	Type	Upper Ref	Lower Ref	Designed Line Width [mil]	Designed Spacing [mil]	Coplaner Spacing [mil]	Finished Line Width [mil]	Finished Spacing [mil]	Impedance Simulation [ohms]	PLOTTED LINE WIDTH
l1comp	50	5.0	5.0	Coated microstrip SE	--	l2pp	7.00	--	--	7.00	--	50.1	7.5
l1comp	100	10.0	10.0	Coated microstrip Diff	--	l2pp	5.00	5.00	--	4.25	5.75	97.0	4.75
l4sold	50	5.0	5.0	Coated microstrip SE	--	l3pp	7.00	--	--	7.00	--	50.1	7.5

Figure A-1. Board Stackup

A.2 Panel Bus digital transmitter: TFP410

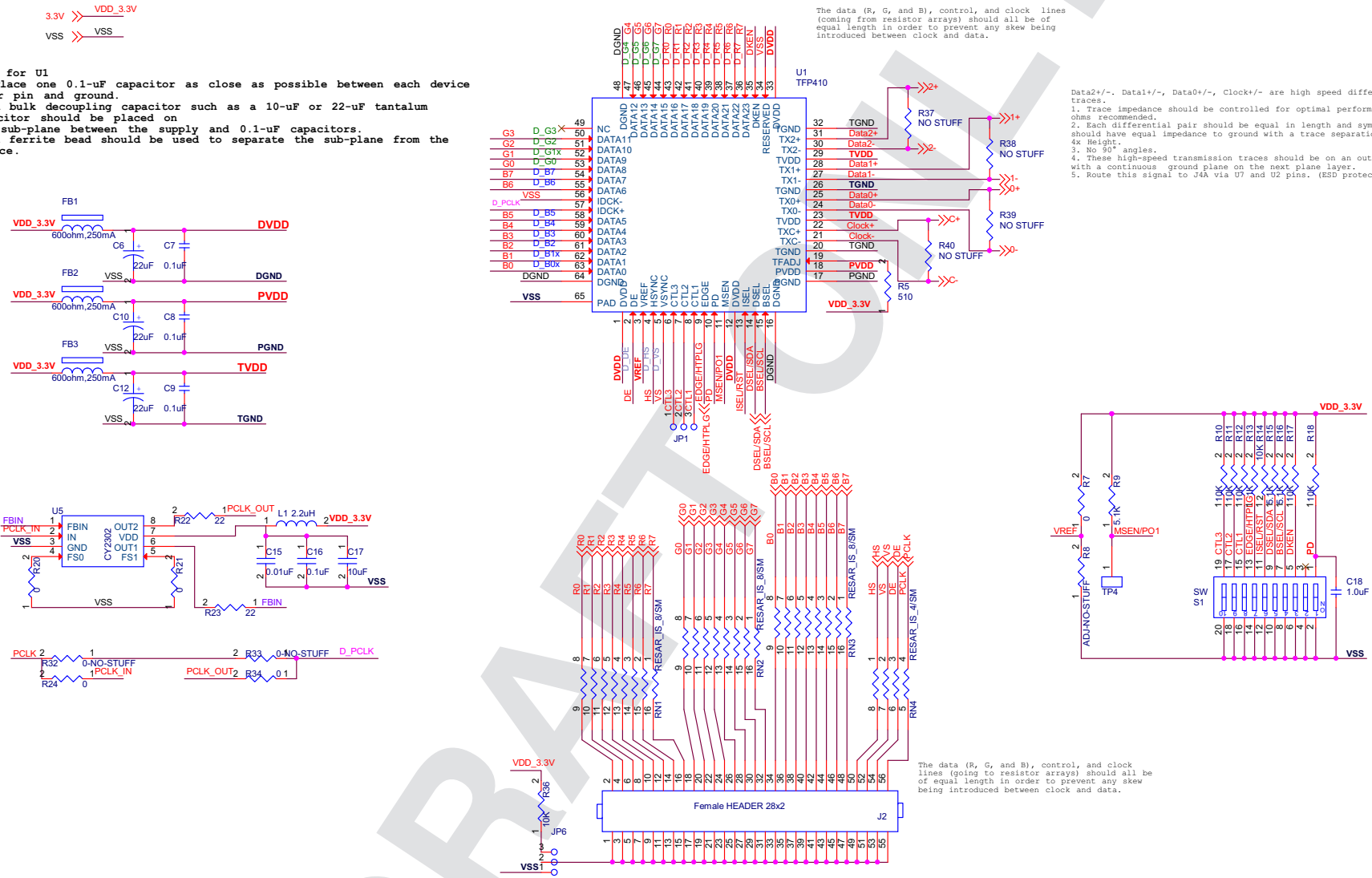

Figure A-2. Panel Bus digital transmitter: TFP410

A.3 LVDS Receiver: DS90CF386

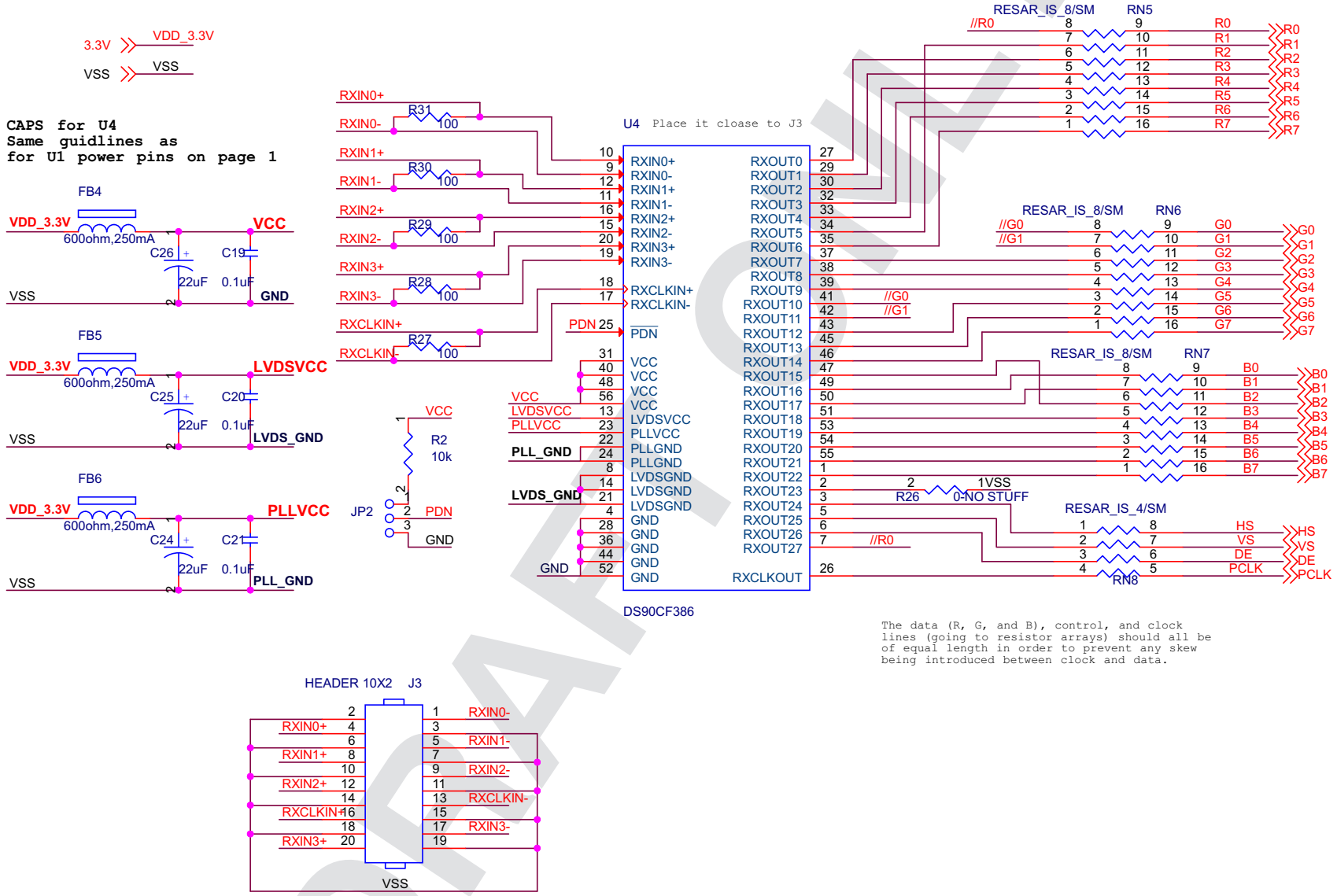

Figure A-3. LVDS Receiver: DS90CF386

A.4 Power and ESD

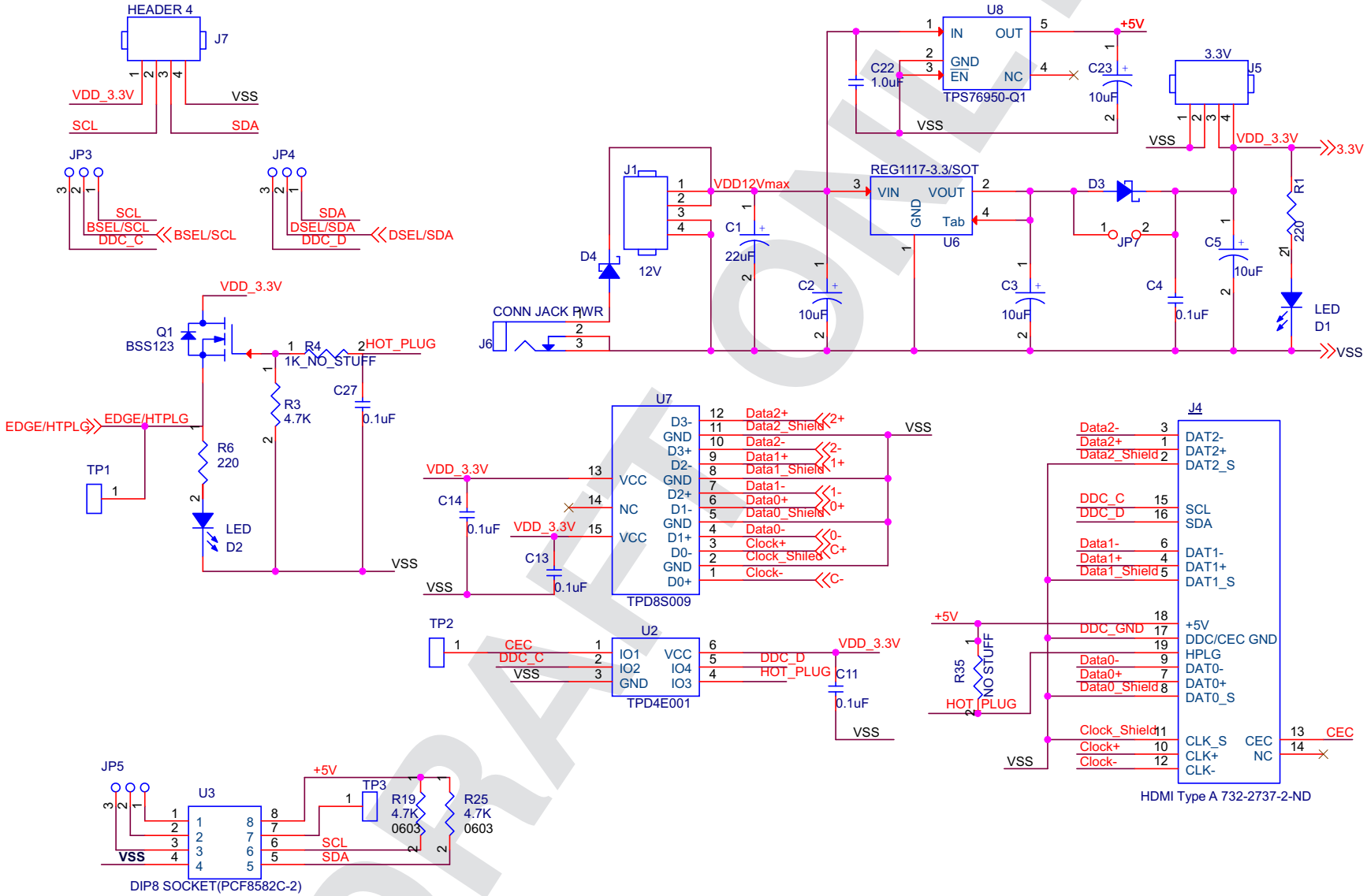

Figure A-4. Power and ESD

Bill of Materials

B.1 FPD23DAEVM BOM

Table B-1. Bill of Material for FPD23DAEVM

Qty	Reference	Part	PCB Footprint	Digi-Key P/N	Comments
1	C1	22uF	2917	493-2391-2-ND	CAP TANT 22UF 25V 20% 2917
3	C2, C3, C5	10uF	2312	718-1044-1-ND	CAP TANT 10UF 25V 20% 2312
1	C4	0.1uF	0805	478-3755-1-ND	CAP CER 0.1UF 25V 10% X7R 0805
6	C6, C10, C12, C24, C25, C26	22uF	1206	718-1473-1-ND	CAP TANT 22UF 10V 10% SMD
7	C7, C8, C9, C19, C20, C21, C27	0.1uF	0201	445-1796-1-ND	CAP CER .1UF 6.3V X5R 10% 0201
4	C11, C13, C14, C16	0.1uF	0603	490-4779-1-ND	CAP CER .1UF 50V X7R 0603
1	C15	0.01uF	0603	399-3189-1-ND	CAP CERAMIC .01UF 100V X7R 0603
1	C17	10uF	0612	445-4072-1-ND	CAP CER 10UF 6.3V X5R 0612
2	C18, C22	1.0uF	0402	PCC2364CT-ND	CAP CERAMIC 1UF 10V X5R 0402
1	C23	10uF	2312	718-1044-1-ND	CAP TANT 10UF 25V 20% 2312
1	D1	LED Green	0603_LED	160-1443-2-ND	LED GREEN CLEAR THIN 0603 SMD
1	D2	LED Red	0603_LED	160-1447-2-ND	LED SUPER RED CLR THIN 0603 SMD
2	D3, D4	DIODE SCHOTTKY	SMA	MBRA210LT3GOSTR-ND	DIODE SCHOTTKY 10V 2A SMA
6	FB1, FB2, FB3, FB4, FB5, FB6	600ohm,250 mA	0402	587-1839-1-ND	FERRITE BEAD 600 OHM 0402
6	JP1, JP2, JP3, JP4, JP5, JP6	3-Pin Header	Header_3P	A26545-ND	CONN HEADER VERT .100 3POS 15AU
1	JP7	JUMPER	Header_2P	A26542-ND	CONN HEADER VERT .100 2POS 30AU
1	J1	12V Header	Header_4P	WM2702-ND	CONN HEADER 4POS .100 VERT GOLD
1	J2	Female HEADER 28x2	HEADER_28 X2_F	S7096-ND	CONN HEADER FMAL 56PS .1" DL TIN
1	J3	HEADER 10X2	HEADER_10 X2_F	A26460-ND	CONN RECEPT 20POS .100 VERT DUAL
1	J4	HDMI Type A	HDMIconn	609-4614-2-ND	CONN HDMI RECPT 19POS SMT R/A
1	J5	3.3V Header	Header_4P	WM2702-ND	CONN HEADER 4POS .100 VERT GOLD
1	J6	CONN JACK PWR	DC_PWR_JA CK	CP-002A-ND	CONN POWER JACK 2.1MM
1	J7	HEADER 4	Header_4P	WM2702-ND	CONN HEADER 4POS .100 VERT GOLD
1	L1	2.2uH	1007	587-1954-2-ND	INDUCTOR 2.2UH 20% 1007 SMD

Table B-1. Bill of Material for FPD23DAEVM (continued)

Qty	Reference	Part	PCB Footprint	Digi-Key P/N	Comments
1	Q1	BSS123	SOT_23	BSS123LT1GOSTR-ND	MOSFET N-CH 100V 170MA SOT-23
3	(#1) RN1, RN2, RN3 (#2) RN5, RN6, RN7	RESAR_IS_8/SM	RN_1506	Y1000TR-ND	RES ARRAY ZERO OHM 8 RES 1506
1	(#1) RN4 (#2) RN8	RESAR_IS_4/SM	RN_0804	Y7000TR-ND	RES ARRAY ZERO OHM 4 RES 0804
1	R1	220	0402	P220JTR-ND RES	220 OHM 1/10W 5% 0402 SMDSMD
8	R2, R10, R11, R12, R14, R17, R18, R36	10K	0402	P10KJCT-ND	RES 10K OHM 1/10W 5% 0402 SMD
1	R3	4.7K	0402	P4.7KJTR-ND	RES 4.7K OHM 1/10W 5% 0402 SMD SMD
2	R4(NO STUFF), R13	1K	0402	P1.0KJTR-ND	RES 1K OHM 1/10W 5% 0402 SMD
1	R5	510	0402	P510LCT-ND	RES 510 OHM 1/10W 1% 0402 SMD
1	R6	220	0402	P220JTR-ND	RES 220 OHM 1/10W 5% 0402 SMD SMD
5	R7, R20, R21, R24, R34	0	0402	P0.0JTR-ND	RES ZERO OHM 1/16W 5% 0402 SMD.
1	R8	ADJ-NO-STUFF	603	NO STUFF	0603 SMD- DO NOT STUFF
3	R9, R15, R16	5.1K	0402	P5.1KJTR-ND	RES 5.1K OHM 1/10W 5% 0402 SMD
2	R19, R25	4.7K	0603	P4.7KGCT-ND	RES 4.7K OHM 1/10W 5% 0603 SMD
2	R22, R23	22	0402	P22.0LCT-ND	RES 22.0 OHM 1/10W 1% 0402 SMD
1	R26	0-NO STUFF	0603	NO STUFF	0603 SMD- DO NOT STUFF
5	R27, R28, R29, R30, R31	100	0402	P100JTR-ND	RES 100 OHM 1/10W 5% 0402 SMD
2	R32, R33	0-NO-STUFF	0402	P0.0JTR-ND	RES ZERO OHM 5% 0402 SMD - DO NOT STUFF
1	R35	NO STUFF	0603	NO STUFF	0603 SMD NO STUFF
4	R37, R38, R39, R40	NO STUFF	0201	P100AGTR-ND	0201 SMD- DO NOT STUFF
1	S1	SW	DIP_SW_10POS	GH7195-ND	SWITCH DIP EXTENDED UNSEAL 10POS
4	TP1, TP2, TP3, TP4	NO STUFF	TEST_POINT	5010K-ND	TEST POINT PC MULTI PURPOSE RED
1	U1	TFP410	64L_TQFP	296-12666-ND	IC TRANSMITTER DIGITAL 64-HTQFP
1	U2	TPD4E001	6_USON	296-30280-2-ND	IC ESD-PROT ARRAY 4CH 6USON
1	U3	DIP8 (for PCF8582C-2)	DIP8	3M5473-ND	SOCKET IC OPEN FRAME 8POS .3"
1	U4	DS90CF386	56_TSSOP	DS90CF386MTD	IC RCVR LVDS FPD 24BIT 56-TSSOP
1	U5	CY2302	8_SOIC	428-2188-5-ND	IC CLK FREQ MULTI/ZDB 2OUT 8SOIC
1	U6	REG1117-3.3/SOT	TO_263_4	296-15941-2-ND	IC REG LDO 3.3V .8A D2PAK-3
1	U7	TPD8S009	15_SON	296-23829-2-ND	IC 8CH ESD PROTECTION 15-SON
1	U8	TPS76950-Q1	SOT_23_5	296-2761-2-ND	IC REG LDO 5V .1A SOT-23-5

Board Layout

C.1 Board Layers

The following mechanical drawings illustrate the physical layout and stack-up of the 4-layer FPD23DAEVM evaluation board:

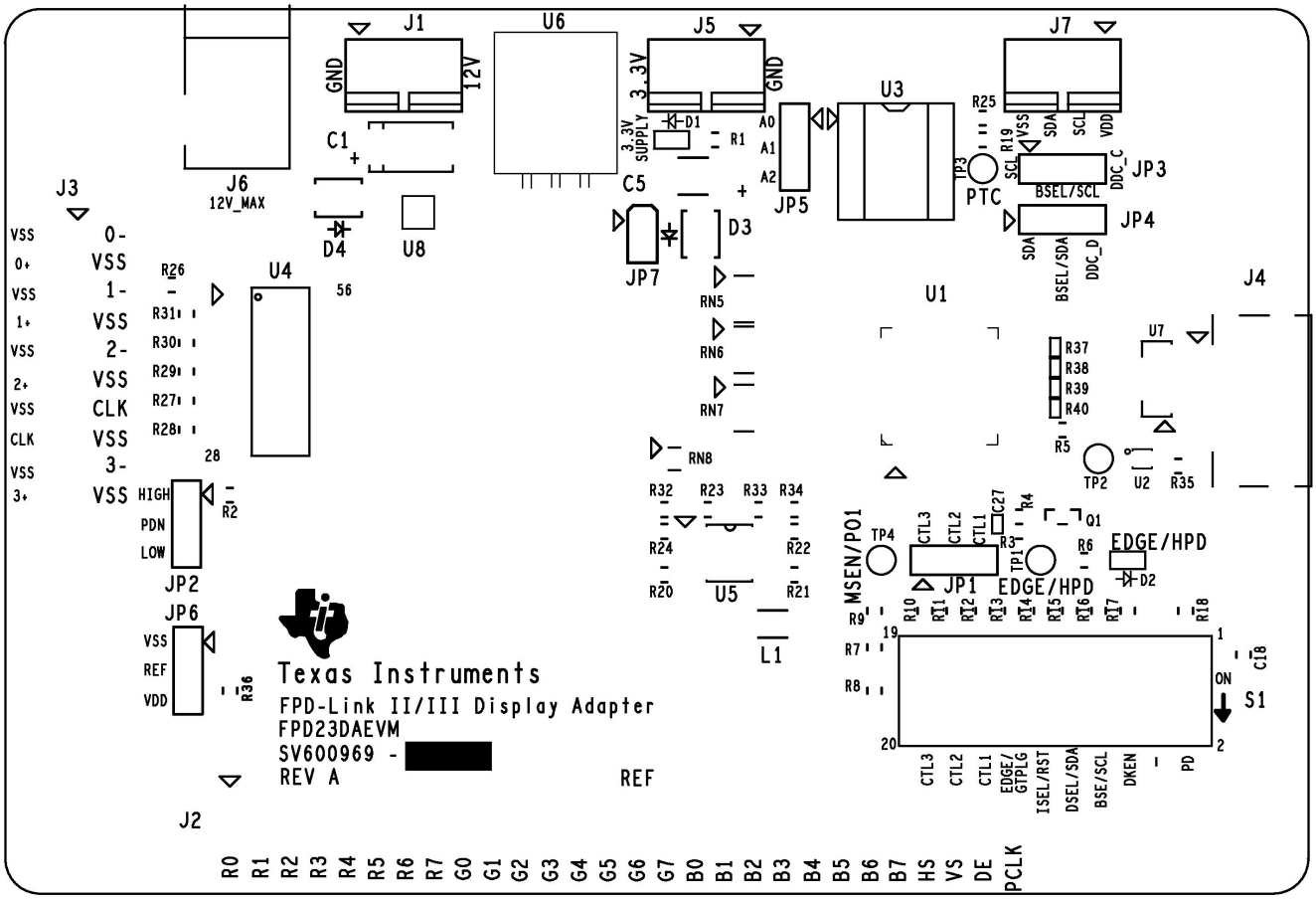

Figure C-1. Top Silkscreen

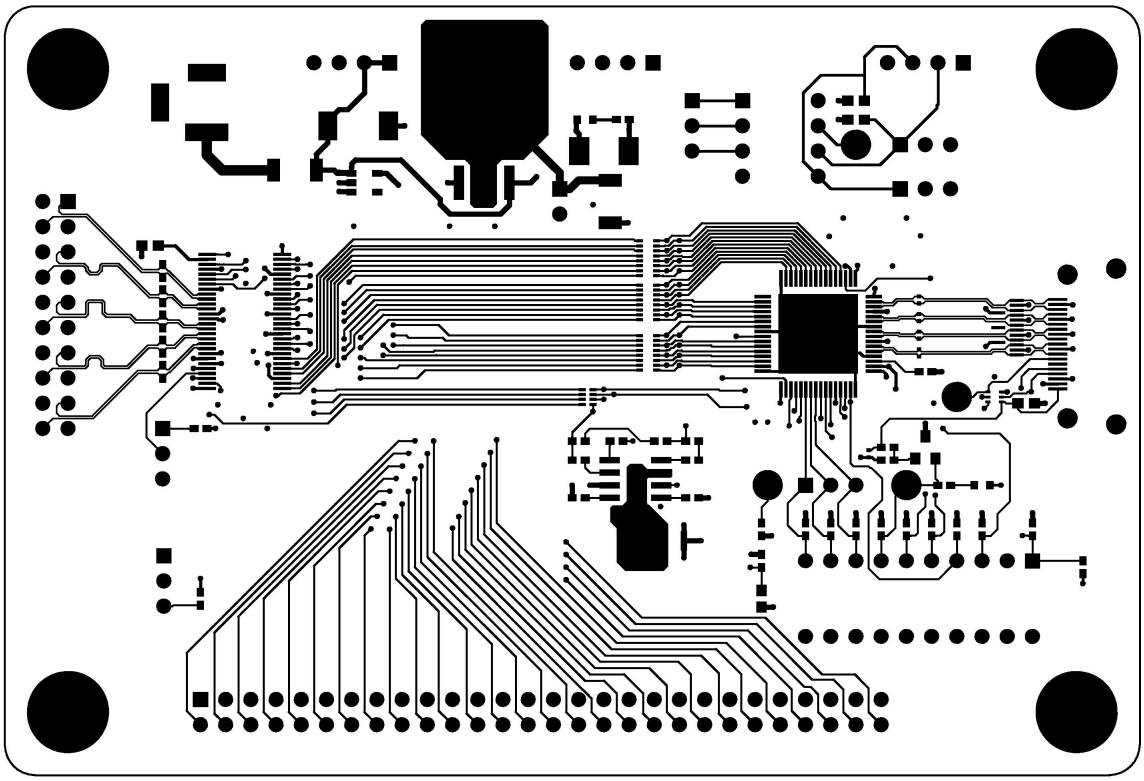

Figure C-2. Top Layer

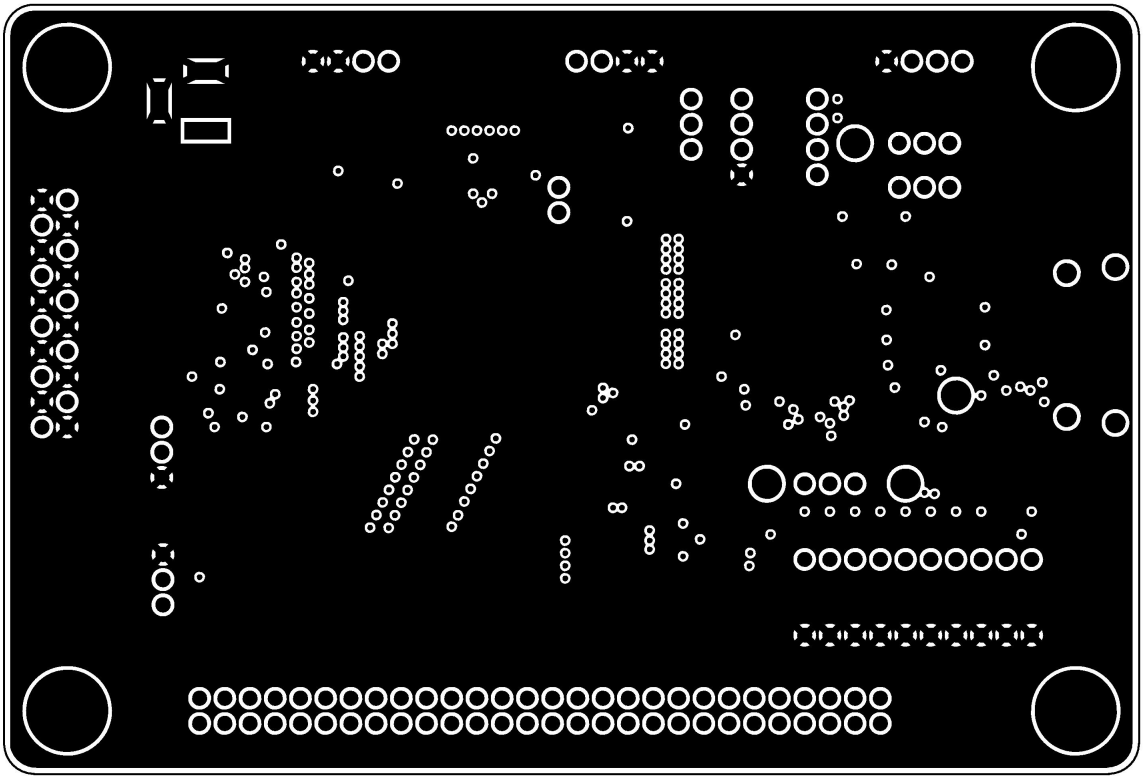

Figure C-3. Layer 2: Ground

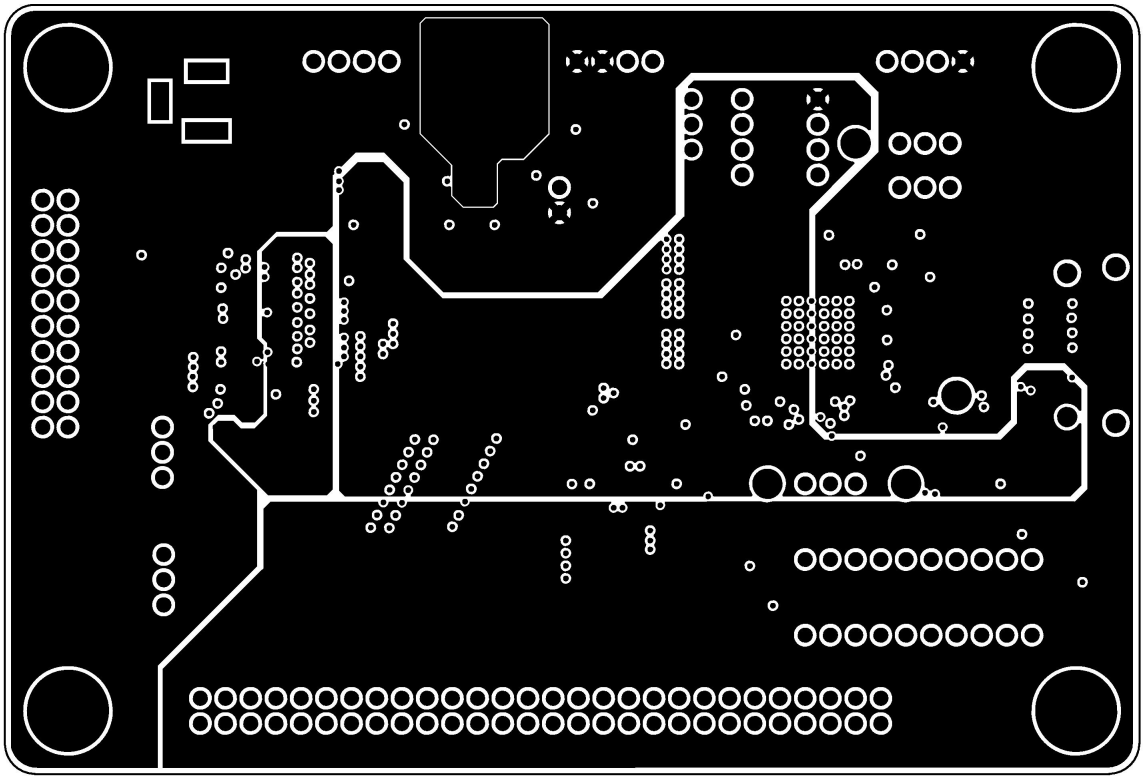

Figure C-4. Layer 3: Power

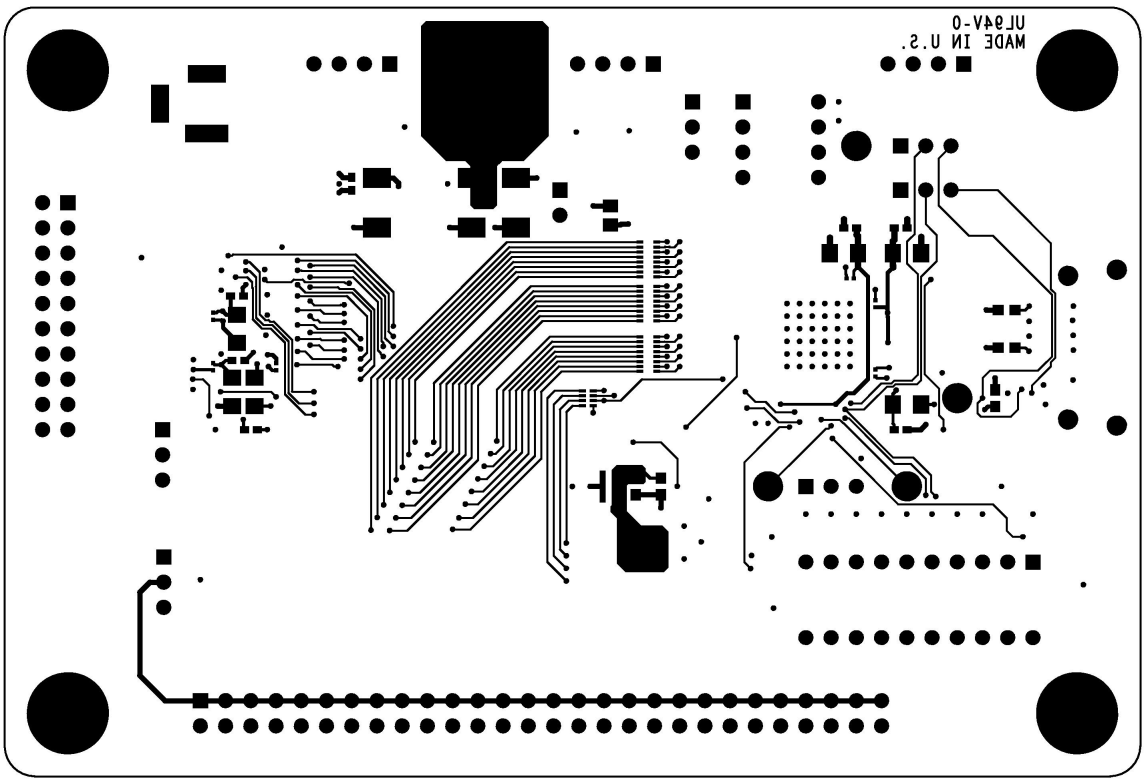

Figure C-5. Bottom Layer

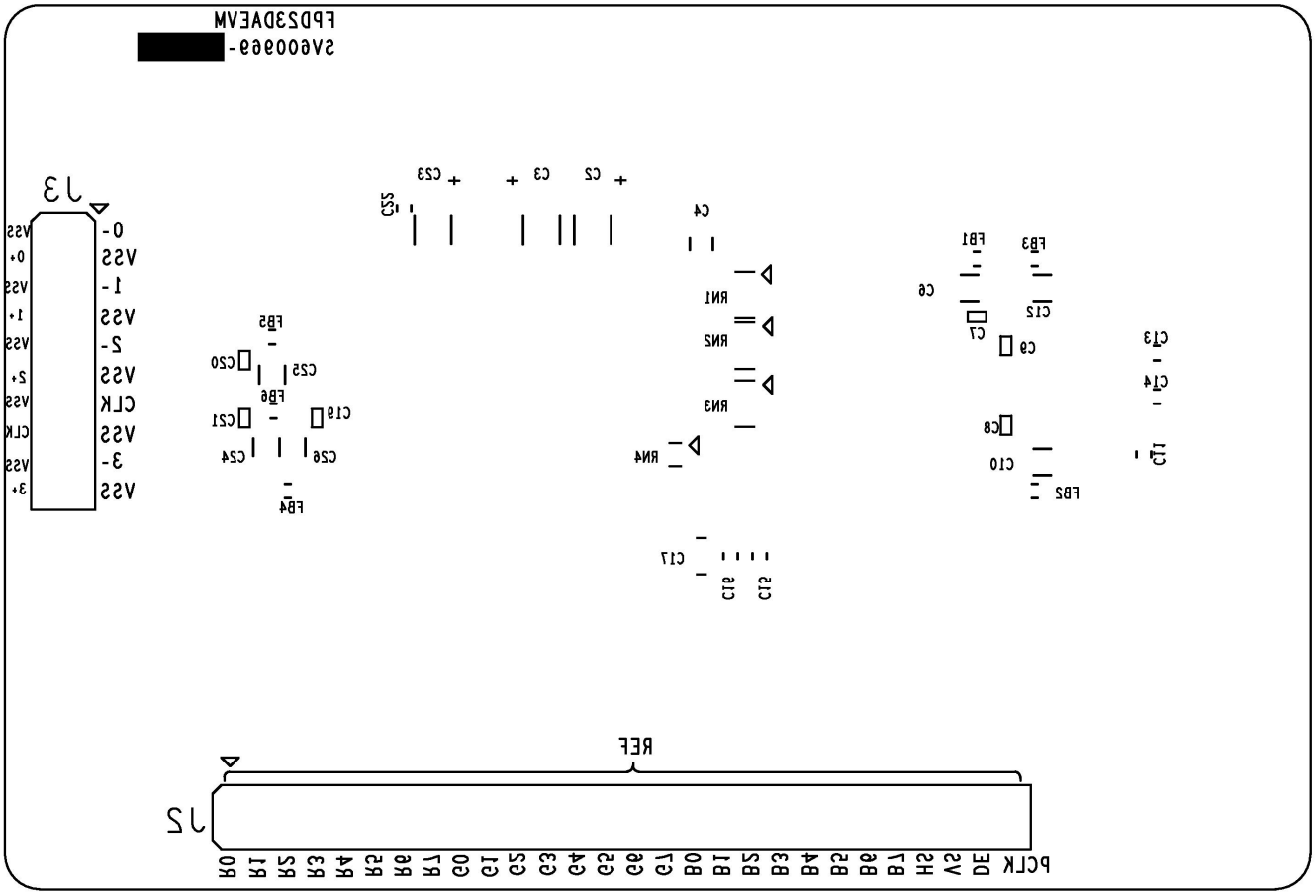

Figure C-6. Bottom Silkscreen