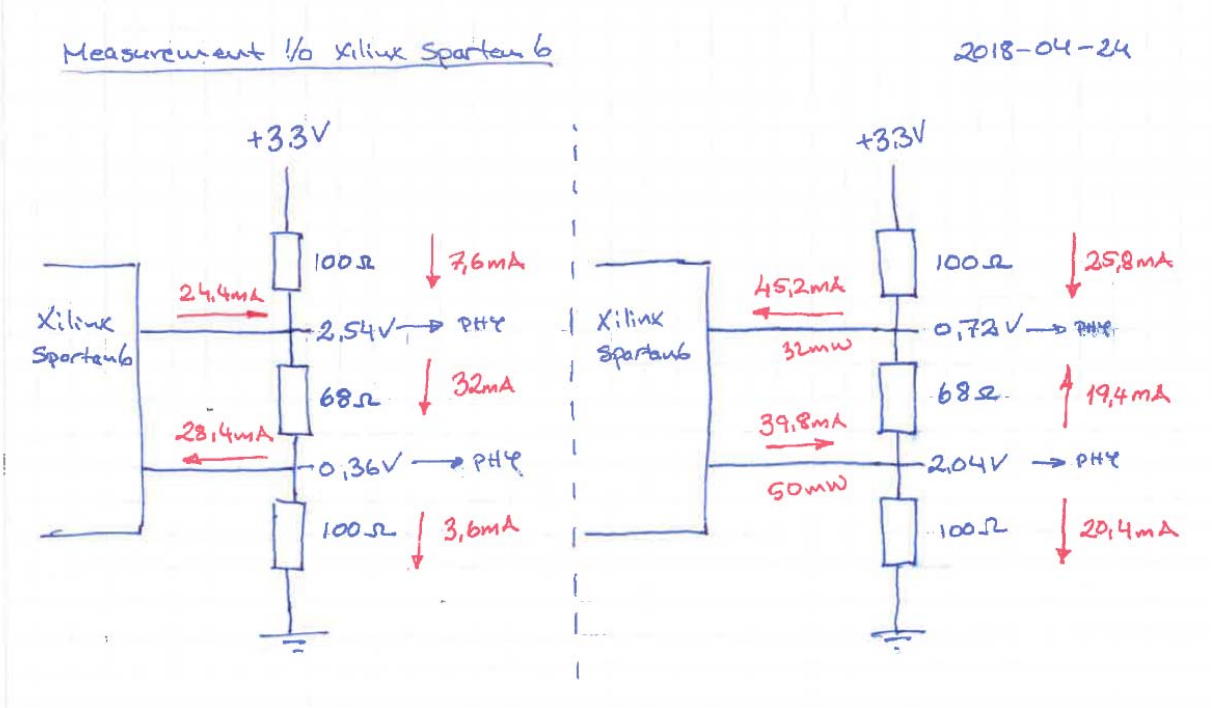
Functional Agile Team Report 2018/05/28

Issue Description: (e-mail 2018/05/15)

"Hi, ABB has a Spartan-6 based product (already at customers) with a I/O termination resulting in a 24mA-45mA current through two LVCMOS33 I/Os.
How will the device be affected? Limited lifetime, or should ABB be happy this even works for a short period?

Will upload schematic



Jan-Anders is the one driving this at ABB. I added Joakim Tolfmans as primary since he was already in the system, and is Jan-anders team lead".

Investigation

The answer from Xlilinx suggests that the outputs from the FPGA can be overloaded, but at the same time some questions arose, which are quite fair and answer to these questions is most likely only known to the designer of PS865:

"In Spartan-6 LVCMOS33 have drive strengths of 24mA (maximum) setting and based on the loads driven, the current value can be higher. The IO's can handle higher currents than 24mA.

Do you expect 45mA being driven consistently over a period of time or only just moments when the logic levels are reached? You can also run a quick IBIS simulation on your setup to check what the PHY is sinking/sourcing".

Can you clarify what was the IO Standard (LVCMOS33) drive strength setting (2/4/6/8/12/24 mA) on Spartan-6 used when you ran these tests?

1. From the Schematic is see the RD+/- pins connected to the FPGA and believe it's the same for TX+/- as well. Per DP83640 datasheet, these pins need to be connected to the RJ45 connector through magnetics.
   Any reason why you have these connected to FPGA?

2. These are Differential pins per spec, any reason for driving them with LVCMOS33?

Answers from Jan-Anders:

"I´ve tried to summarize:

0. The drive strength setting (LVCMOS33) was in this case 12mA.
1. This is an existing design and why this solution was chosen I don't have any information about.
   In this case these signals are driving optical transducers and not electrical Ethernet.
   Why they are connected to the FPGA I don´t have any answer (sorry)
2. The reason for driving them with LVCMOS33 is to get the appropriate voltage swing.

As you can see, this is an existing design where we found this (maybe odd) design giving these high IO-currents.

a. Is it possible to give some IO-setting advice when using this circuit design
b. Is it possible to give some comments regarding lifetime"

My investigation of the issue revealed the following:

The I/O of the FPGA are configurable

"Single-ended outputs use a conventional CMOS push/pull output structure, driving High towards V_{CCO} or Low towards
ground, and can be put into high-Z state. Many I/O features are available to the system designer to optionally invoke in each
I/O in their design, such as weak internal pull-up and pull-down resistors, strong internal split-termination input resistors,
adjustable output drive-strengths and slew-rates, and differential termination resistors. See the *Spartan-6 FPGA SelectIO Resources User Guide* for more details on available options for each I/O standard."

At the same time the TI spec says that RD+ and RD- are:

Differential common driver transmit output (PMD Output Pair). These differential outputs are automatically configured to either 10BASE-T or
100BASE-TX signaling. In Auto-MDIX mode of operation, this pair can be used as the Receive Input pair. In 100BASE-FX mode, this pair becomes the 100BASE-FX Transmit pair.
These pins require 3.3-V bias for operation.

In accordance to the TI specification, both RD+ and RD- bias resistors should be connected to +3.3V.
The layout pertinent to these two signals raises a question if such a low value resistors as termination are necessary.

To check both RD+ and RD- waveforms the test was run with the FPGA output set to 24 mA. The results of these tests are shown in fig 2 and fig 3.

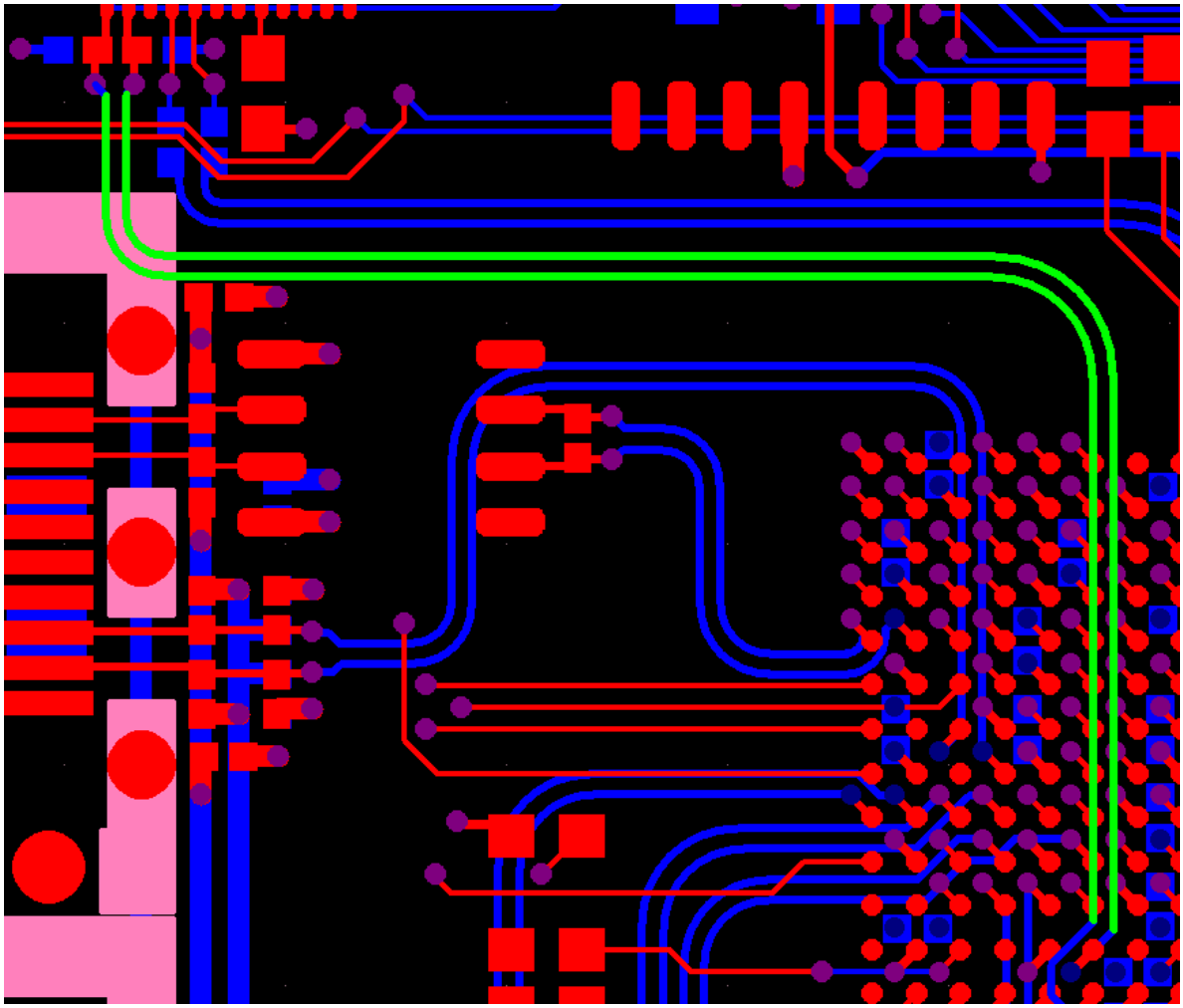


Fig 1 Fragment of PS865 layout with pertinent traces highlighted green

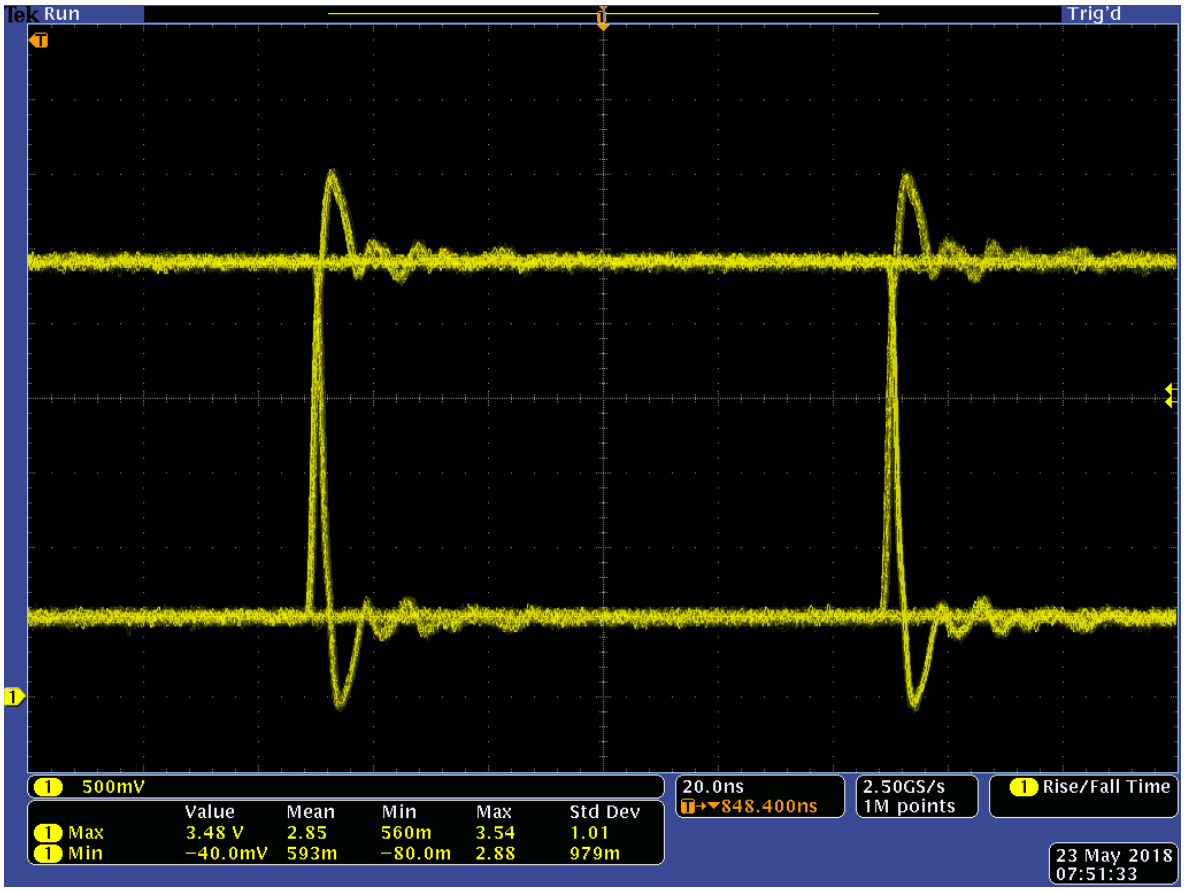


Fig 2 Eye diagram of the voltage at pin 14 of D13

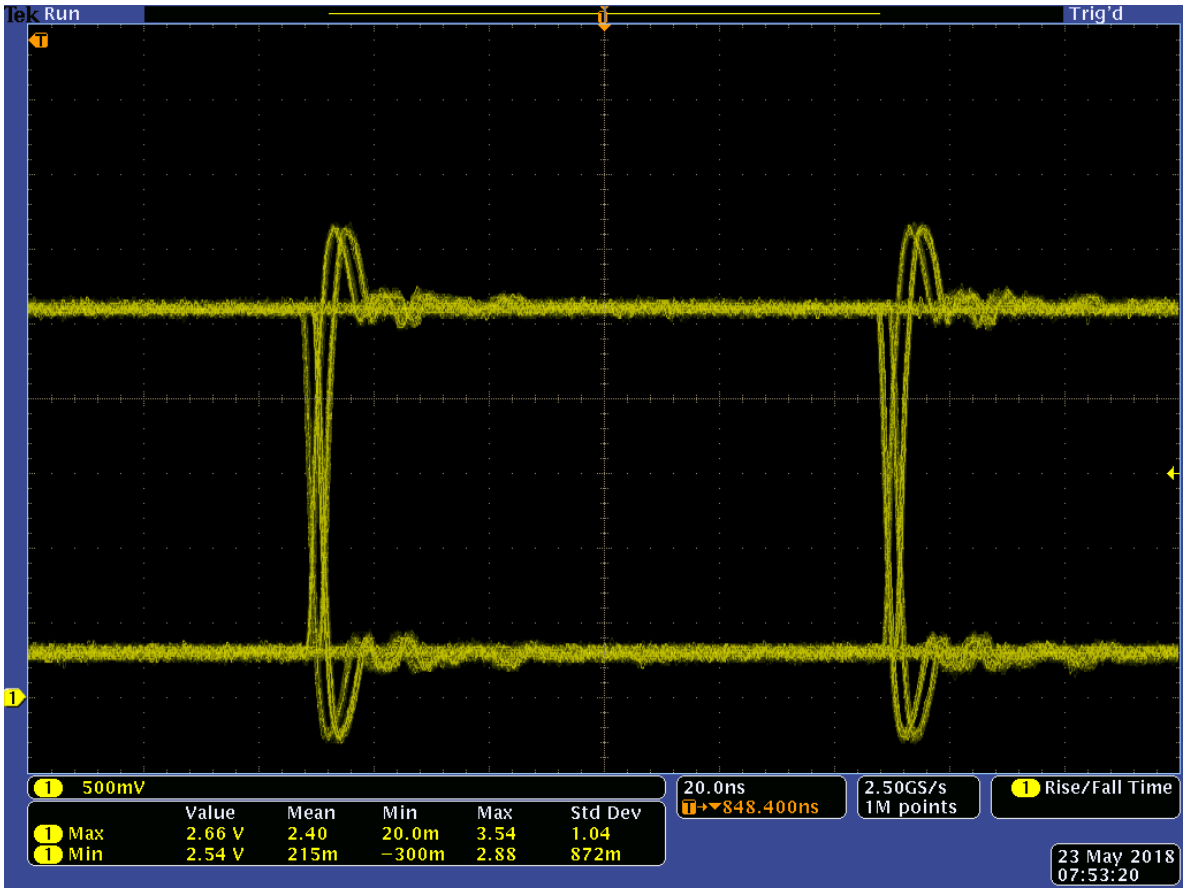
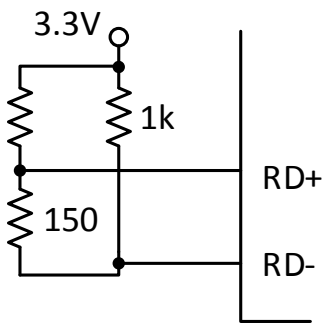


Fig 3 Eye diagram of the voltage at pin 13 of D13

It could be seen that the currents related to the steady state here are even higher than seen in the sketch on page 1. This is assuming that the Rd+ and RD- inputs present high impedance. In spite of some efforts trying to find out what are RD+ and RD- inputs the efforts proved to be in vain.

The simulation with different configuration of the resistor network, which complies with DP83640 specification is shown in the sketch below



The simulation proved that the impact of the bias resistors (1K) on the waveform is negligible. The waveform becomes more symmetrical and the currents are within 24 mA.

The waveforms presented below are showing eye diagrams of both inputs with the corrected resistor network.

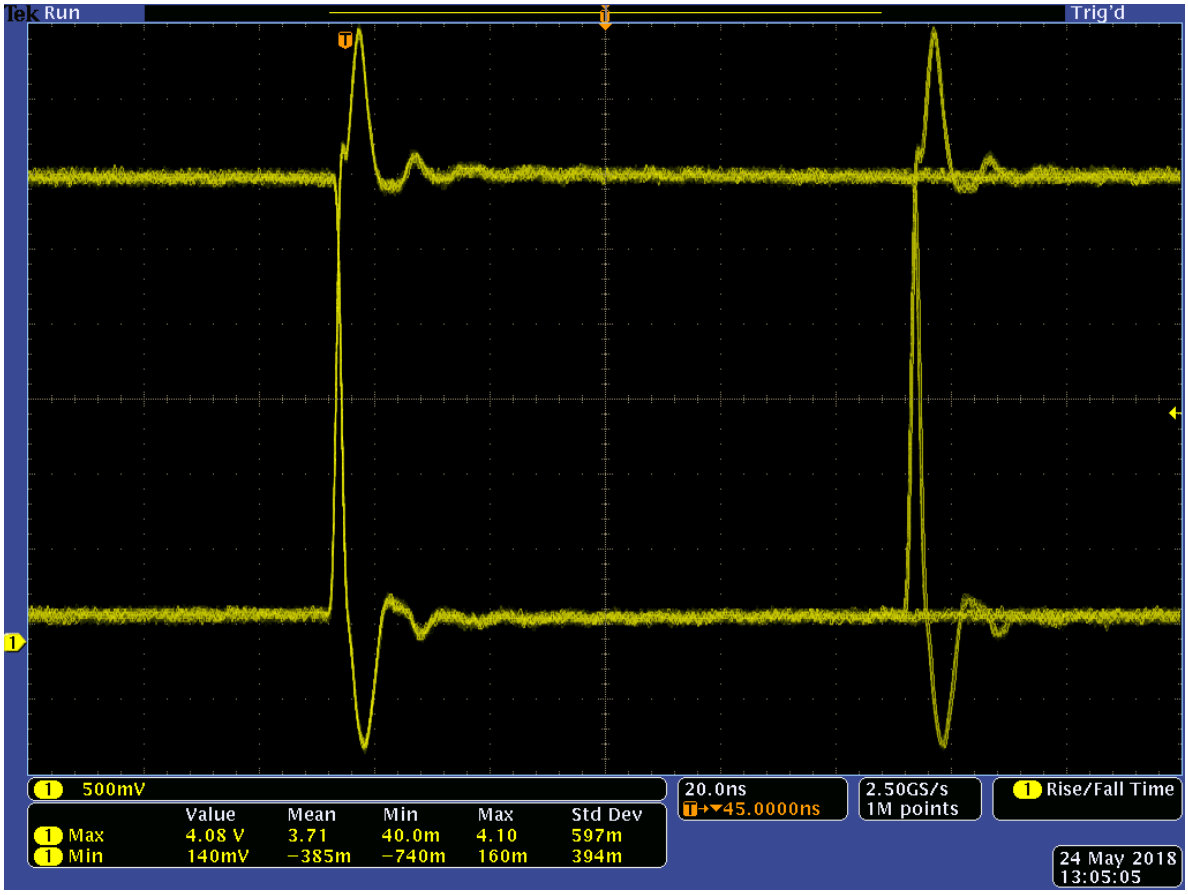


Fig 4 Eye diagram of the voltage at pin 14 of D13 with changed input network

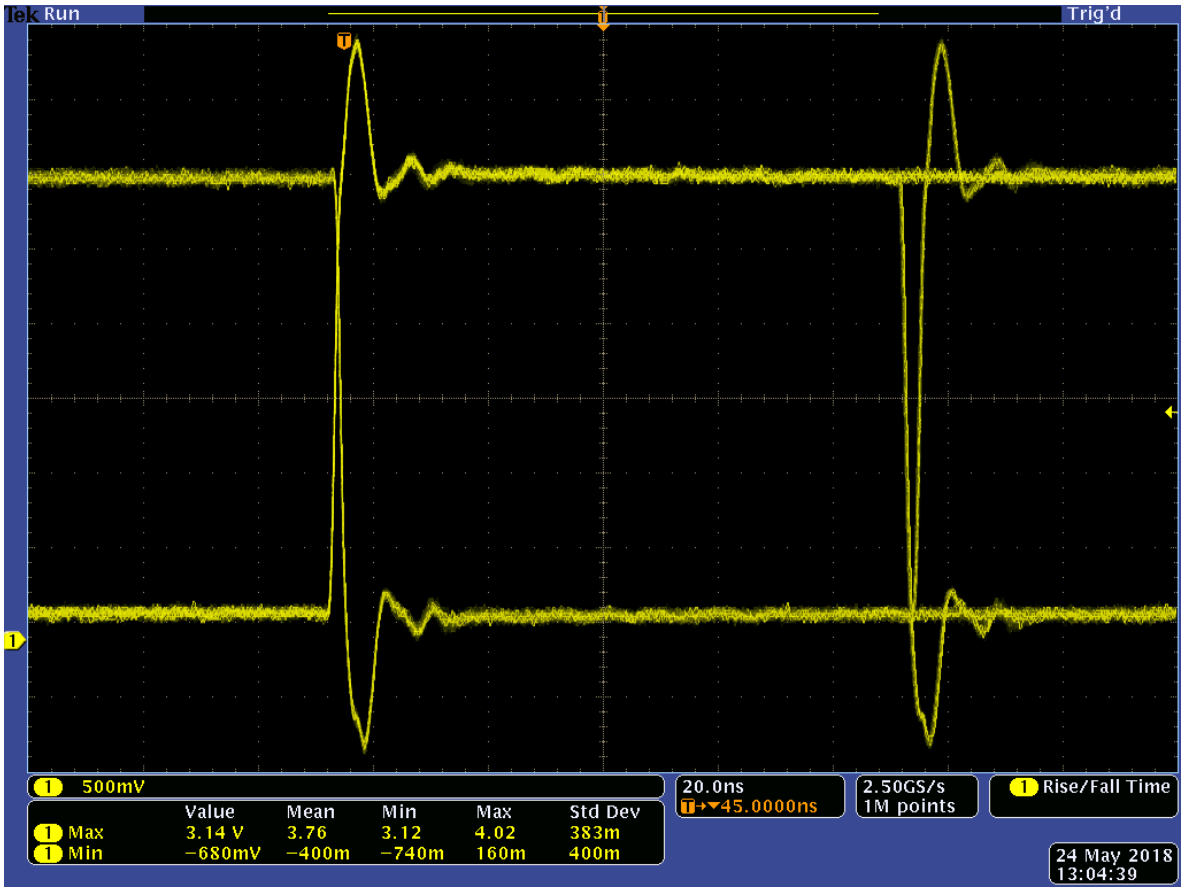


Fig 4 Eye diagram of the voltage at pin 13 of D13 with changed input network

Conclusions

- If no changes are allowed on the board then the answer from Xilinx must suffice, however it is unclear, what is the statement "The currents you noticed will not damage the device and shouldn't affect the lifetime of the device." is based on, if the specification of the device is clearly stating 24 mA max.
- The solution to the issue related to the FPGA currents is to change the biasing/termination network to one shown in the previous page.
- It is uncertain at this point if the switching transients are acceptable for the RD+ and RD- inputs, this still needs to be investigated
- The solution to these transient, provided that the layout can be corrected is quite simple. The distance between the D28 and D13 can be shortened which will change the parameters of the transmission line or Shottky diodes can be applied at both inputs of D13 to clamp these transients to 3.3V and GND.
- The application of DP83640 is yet another issue, but this is not a topic of this assignment

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