Related to issue with establishing GBit-link using DP83867, we have observed that utilizing

BIT(7) of register 0x0031 has a positive effect. Referring to the datasheet and CFG4 register:



The (linux) kernel driver implementation supporting this fix utilizes a device tree config. option as follows:

﻿        - ti,dp83867-rxctrl-strap-quirk - This denotes the fact that the

                                    board has RX\_DV/RX\_CTRL pin strapped in

                                    mode 1 or 2. To ensure PHY operation,

                                    there are specific actions that

                                    software needs to take when this pin is

                                    strapped in these modes. See data manual

                                    for details.

We struggle to find the appropriate details in the data manual to understand what effect – exactly - utilizing

BIT(7) of register 0x0031 shall have on the PHY and need your input on this. Please clarify.

Related; we also observe that the examples related to DTS config. for DP83867 uses the following

values for rx/tx delay and fifo depth:

﻿&davinci\_mdio {

        dp83867\_0: ethernet-phy@2 {

                reg = <2>;

                ti,rx-internal-delay = <DP83867\_RGMIIDCTL\_2\_25\_NS>;

                ti,tx-internal-delay = <DP83867\_RGMIIDCTL\_250\_PS>;

                ti,fifo-depth = <DP83867\_PHYCR\_FIFO\_DEPTH\_8\_B\_NIB>;

                ti,min-output-impedance;

                interrupt-parent = <&gpio6>;

                interrupts = <16 IRQ\_TYPE\_EDGE\_FALLING>;

                ti,dp83867-rxctrl-strap-quirk;

        };

};

Are these – somehow – the recommended settings for DP83867? Just FYI; we currently specify:

﻿            /\* TI DP83867 \*/

            mdio1 {

                #address-cells = <1>;

                #size-cells = <0>;

                compatible = "snps,dwmac-mdio";

                eth1\_phy: ethernet-phy@1 {

                    compatible = "ethernet-phy-id2000.A231", "ethernet-phy-ieee802.3-c22";

                    reg = <15>;

                    ti,rx-internal-delay = <DP83867\_RGMIIDCTL\_2\_25\_NS>;

                    ti,tx-internal-delay = <DP83867\_RGMIIDCTL\_2\_75\_NS>;

                    ti,fifo-depth = <DP83867\_PHYCR\_FIFO\_DEPTH\_4\_B\_NIB>;

                      ti,dp83867-rxctrl-strap-quirk = <1>;

                      enet-phy-lane-no-swap = <1>;

                };

            };

Do you consider any of our settings to be unfortunate regarding the DP83867 configuration/behavior;

based on previous experience in a linux kernel driver environment?