CH7024 TV Encoder

Features

- TV encoder targeting handheld and similar systems
- Support for NTSC, PAL
- Video output support for CVBS or S-video
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supporting various RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) input data formats
- Support for input resolutions up to 720x480 and 720x576 (e.g. 220x176, 320x240, 640x480, 720x480, 720x576, etc.)
- Adjustable brightness, contrast, hue and saturation.
- Detect TV / Monitor connection
- Two high quality10-bit video DAC outputs
- Fully programmable through serial port
- Flexible pixel clock frequency from graphics controller (2.3MHz—64MHz)
- Flexible input clock on the crystal or oscillator (2.3MHz—64MHz)
- Flexible up and down scaling on the display
- Master and slave mode
- Offered in 48-pin LQFP Package
- IO voltage and SPC/SPD from 1.2V to 3.3V
- Programmable power management
- Power down current less than 20uA typical
- Power consumption of <150mW for one CVBS output, single terminated and <350mW for two DAC outputs, double terminated.

General Description

The CH7024 is a TV encoder device targeting handheld, portable video applications such as digital still cameras and similar portable embedded systems. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards.

Supported TV output formats are NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/A/I, PAL-M, PAL-N and PAL-60.

The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) via 24 bit/18 bit/15 bit /12 bit /8 bit multiplexed digital inputs. Most embedded controllers are supported. The I/O interface voltage between CH7024 and digital video source controller can be selected by the I/O supply voltage (VDDIO). The I/O supply voltage range is from 1.2V to 3.3V. The digital input voltage will follow the I/O supply voltage.

CH7024 is offered in 48-pin LQFP package (7 x 7 mm). CH7024 48-pin LQFP package comes with fixed single serial port address.

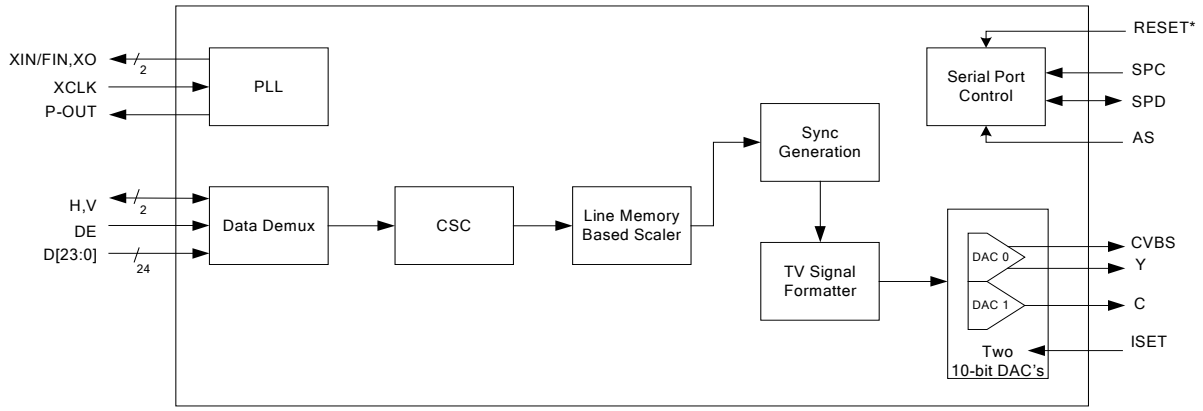

Figure 1: CH7024 Block Diagram

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1.0 PIN-OUT

The CH7024 48-pin LQFP comes with three video output pins, primary CVBS (pin 28), S-video Y (pin 27) and secondary CVBS or S-video C (pin 26).

The CH7024 48-pin LQFP package comes with fixed single serial port address (76h – 7 bit address) .

1.1 Package Diagram

1.1.1 The 48-pin LQFP Package Diagram

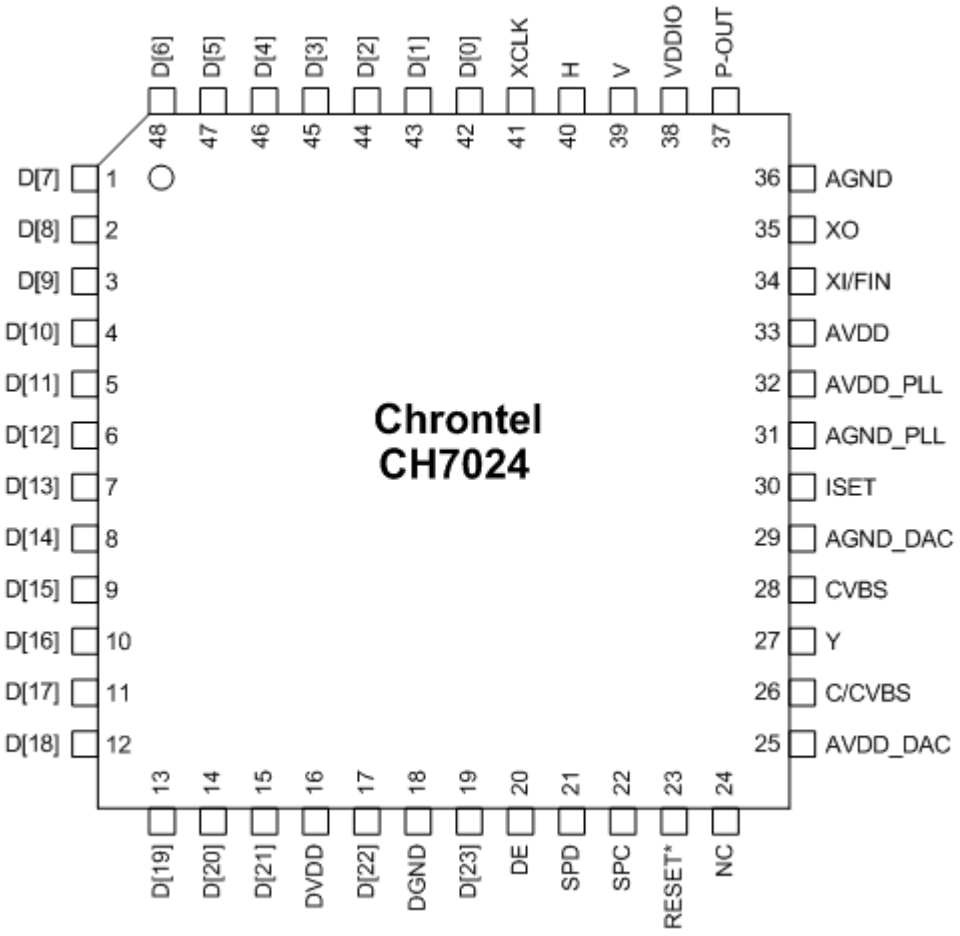

Figure 2: **48-LQFP Package (top view)**

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1.2 Pin Description

1.2.1 The 48-pin LQFP Pin Description

The 48-pin LQFP Package does not have AS pin to select second serial port address option. Refer to application note AN-98 for device address byte (DAB) details. The serial port device address for the read and write operation is fixed at ECh and EDh respectively.

It has internal switch to provide separate primary CVBS (pin 28) and S-video Y (pin27) outputs. Refer to section 2.3.2 Video DAC output and the Control Register 0Ah for the video DAC output control.

Table 1: Pin Description (48-pin LQFP)

Pin #	Type	Symbol	Description
42-48, 1-15, 17,19	In	D[0]-D[23]	Data[0] through Data[23] Inputs These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO.
40	In/Out	H	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The amplitude will be 0 to VDDIO.
39	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The amplitude will be 0 to VDDIO.
20	In	DE	Data Enable When the pin is high, the input data is active. When the pin is low, the input data is blanking.
24	–	NC	–
23	In	RESET*	Reset * Input This pin is internally pulled high. When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port. At reset process, the level of the external output pin is low. After reset process finished, the level of the external output pin depends on the default setting.
21	In/Out	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port and operates with input level from 0 to VDDIO. Outputs are driven from 0 to VDDIO.
22	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port and operates with input level from 0 to VDDIO. We need to wait until power on reset stable to use I2C communication.
28	Out	CVBS	Composite Video This is a primary composite vide output when S-video Y (pin 27) is not used. This output is turned off when S-video Y output is used.

Table 1: Pin Description (cont'd)

Pin #	Type	Symbol	Description
27	Out	Y	Luma Output The output is S-video luminance when the primary CVBS output (pin 28) is not used.
26	Out	C/CVBS	Chroma/CVBS Output The output is S-video chrominance when S-video is used. But, when dual CVBS outputs are needed, this out pin can be used for secondary CVBS output in addition to the primary CVBS output (pin 28).
30	In	ISET	Current Set Resistor This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC (pin 29) using short and wide traces.
37	Out	P-Out	Pixel Clock Output This pin provides a clock signal to the graphics controller, which can be used as a reference frequency. The output driver is driven from the VDDIO supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
34	In	XI/FIN	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
35	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
41	In	XCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
38	Power	VDDIO	IO Supply Voltage (1.2-3.3V)
16	Power	DVDD	Digital Supply Voltage (1.8V)
18	Power	DGND	Digital Ground
25	Power	AVDD_DAC	DAC Supply Voltage (2.5-3.3V)
29	Power	AGND_DAC	DAC Ground
32	Power	AVDD_PLL	PLL Supply Voltage (1.8V)
31	Power	AGND_PLL	PLL Ground
33	Power	AVDD	Crystal Supply Voltage (2.5-3.3V)
36	Power	AGND	Crystal Ground

2.0 FUNCTIONAL DESCRIPTION

2.1 Modes of Operation

Table 2: Operating Modes describes the possible operating modes for CH7024 TV encoder. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Basically, CH7024 can take non-interlaced data from graphics controller and encode it to analog NTSC and PAL waveforms. It can also take interlaced data from sources and perform SDTV encoding.

Table 2: Operating Modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode	Described In section
Non-Interlaced	RGB / YCrCb	Interlaced	CVBS, S-video	SDTV encoder (NTSC / PAL) with non-interlaced input	2.1.1
Interlaced (480i, 576i)	RGB / YCrCb	Interlaced	CVBS, S-video	SDTV encoder (NTSC / PAL) with interlaced input	2.1.2

2.1.1 Graphics Controller to SDTV Encoder

CH7024 is mainly designed as an SDTV encoder targeting handheld device market. In this mode, the graphics controller of the handheld system will send non-interlaced data, sync and clock signals to CH7024. CH7024 can run in clock master mode or clock slave mode. In clock master mode, an accurate (less than 20ppm) crystal is required between XI/FIN and XO pins or an accurate CMOS clock signal is needed on the XI/FIN pin. The frequency of the crystal or the clock has to be between 2.3MHz and 64MHz. CH7024 will generate a reference clock signal (P-Out) according to the requirement of the graphics controller. However, the range of this clock reference signal is between 2.3MHz and 64MHz. In clock slave mode, no reference clock is output to the graphics controller. So, the crystal becomes may only be necessary for color sub-carrier generation in the slave mode. However, if the clock from the graphics controller cannot meet the requirement of color sub-carrier generation, the crystal is still required, which will discuss in the latter part of this document. Horizontal and vertical sync signals are normally sent to the device from the graphics controller, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. However, the DE signal is NOT generated inside. Data can be unitary or 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data will be scaled, scan converted and filtered, then encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-video and CVBS format. The graphics resolutions supported are from 220x176 to 720x576. The typical resolutions are shown in Table 4.

Table 3: Typical Input Resolution

Typical Input Resolution	220x176	320x240	512x384	640x400	640x480	720x400	720x480	720x576
TV Output Standard	NTSC,PAL							

2.1.2 ITU-R BT.601/656 TV Encoder

In interlaced data, sync and clock signals are input to the CH7024 from a graphics controllers digital output port, or the output of an MPEG decoder device. The YCrCb data format is most commonly used in these modes. A clock signal (P-Out) can be output as a frequency reference to the graphics device. Horizontal and vertical sync signals are normally sent to the CH7024 from the graphics device, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. Data can be unitary or 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data bypasses the scaling, scan conversion and filtering blocks, is encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-video and CVBS format. The graphics resolutions supported for ITU-R BT.601/656 TV output are shown in Table 5 below. CH7024 is non-Macrovision™ part. The timing of the sync signals is shown in Figure 3 below. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7024 to identify the correct field.

Table 4: ITU-R BT.601/656 TV Encoder Operating Modes

Input Resolution	TV Output Standard
720x480i	NTSC
720x576i	PAL

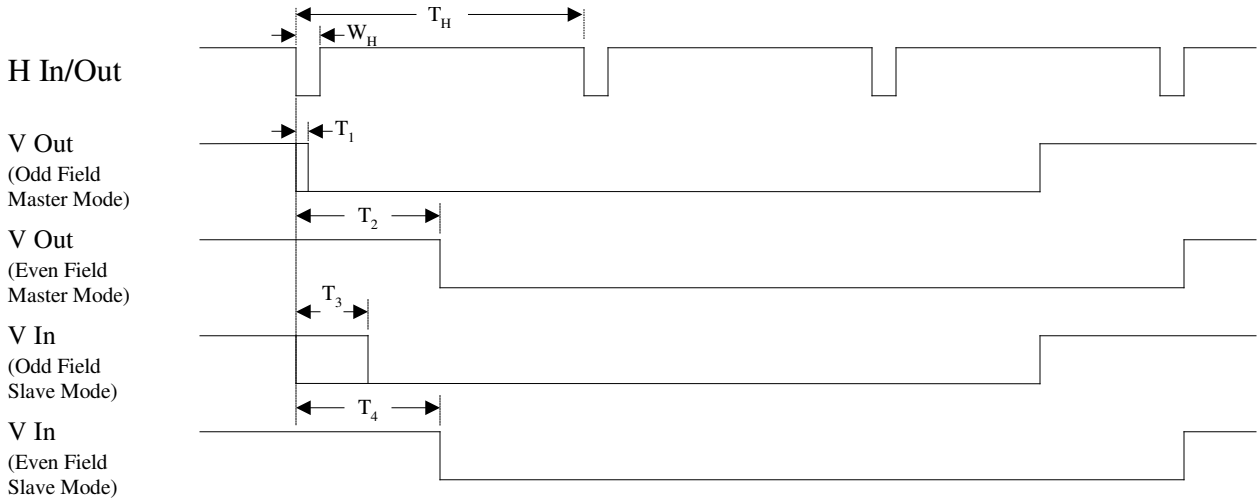

Figure 3: Interlaced Sync Input/Output Timing

Table 5: Interlaced Sync Input/Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{PCK}	Input clock period	6.73		47.62	us
T_H	Total Line Period SDTV	63.5		63.5	us
W_H	Hsync Width When output from CH7024 When input to CH7024	 1 1	 64 64		 Pixel clocks Pixel clocks
T_1	Odd Field (Field 1) V SYNC out to H SYNC out alignment		0		us
T_2	Even Field (Field 2) V SYNC out delay from H SYNC out		$0.5*T_H$		us
T_3	Odd Field (Field 1) V SYNC in to H SYNC in alignment	0		$W_H - T_{PCK}$	us
T_4	Even Field (Field 2) V SYNC in delay from H SYNC in	W_H		$T_H - T_{PCK}$	us

2.2 Input Interface

2.2.1 Overview

Three distinct methods of transferring data to the CH7024 are described. They are:
Unitary data, clock input at 1X the pixel rate
Multiplexed data, clock input at 1X the pixel rate
Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7024 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7024 is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7024 is latched with one edge of the clock .The polarity of the pixel clock can be reversed under serial port control.

2.2.2 Input Clock and Data Timing Diagram

Figure 4 below shows the timing diagram for input data and clocks. The first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in section 4.5.

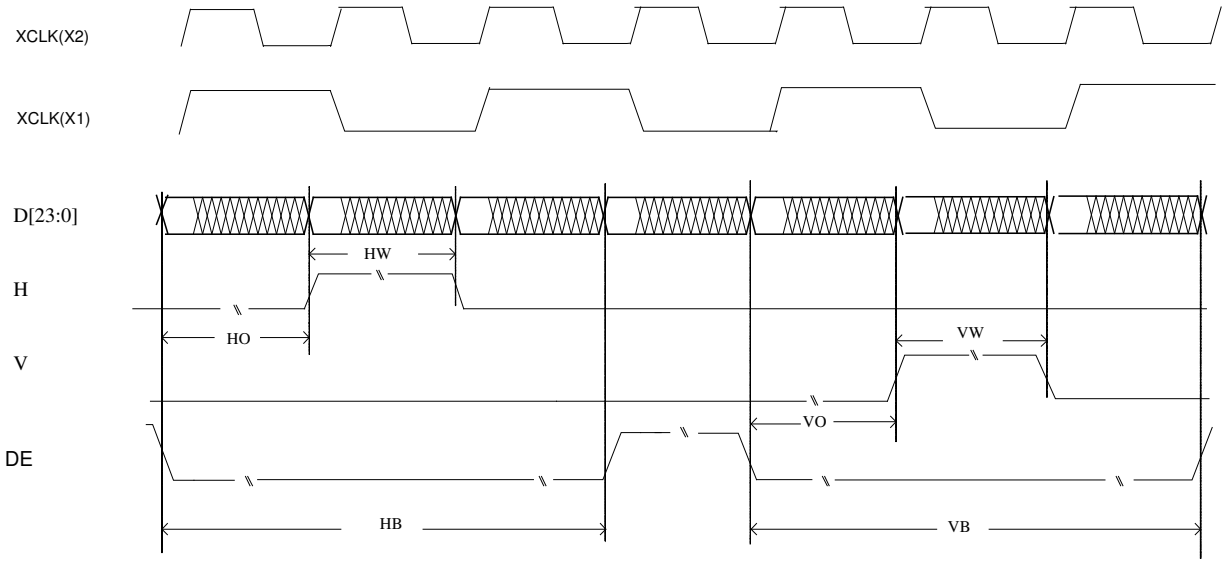

Figure 4: Clock, Data and Interface Timing

Figure 5: Input Diagram below shows the input diagram to help understand symbol meaning easily.

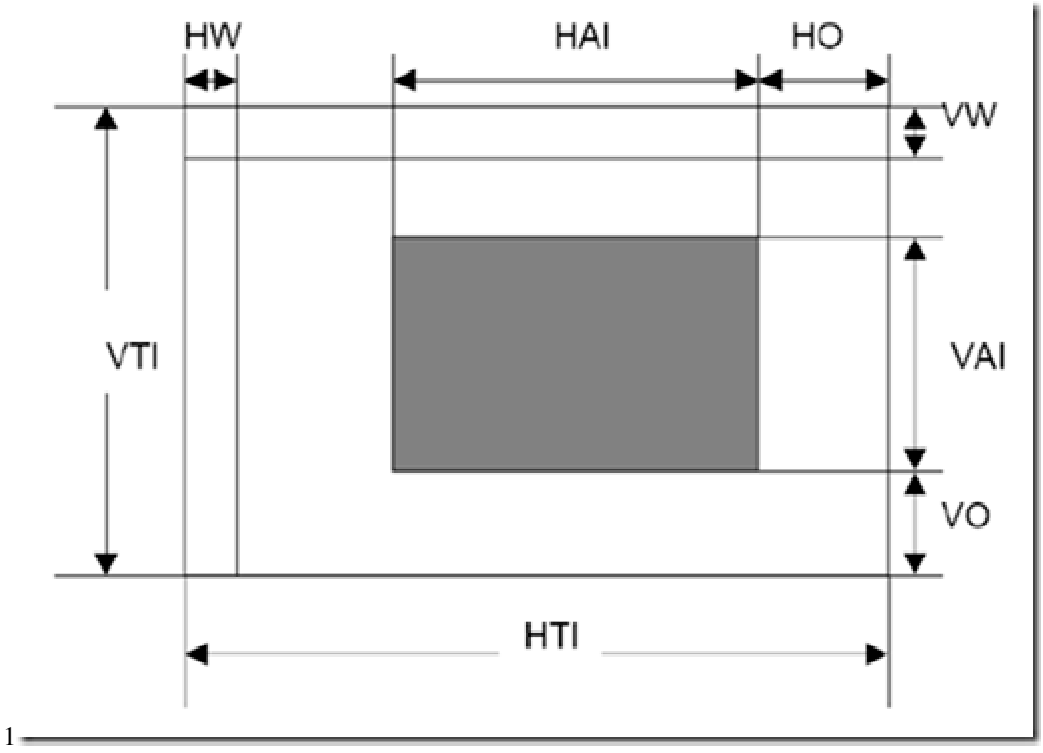

Figure 5: Input Diagram

HW: Input H Sync Width
HAI: Input H Active
HO: Input H Sync Offset
HTI: Input H total
VW: Input V Sync Width
VAI: Input V Active
VO: Input V Sync Offset
VTI: Input V total

Please refer to CH7024B Input Timing Register Information.

2.2.3 Input data voltage

The voltage level of input pins D[23:0], H, V, DE, SPC, SPD are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit DIFFEN(Control Register 0Eh) is high, the input is pseudo differential mode which use a reference voltage to compare with input voltage and decide input logic value. The pseudo differential mode can accept the wide range of the input voltage level from 1.2V to 3.3V, while the CMOS mode can accept 1.8V to 3.3V Input voltage.

2.2.4 Input data formats

The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) via 24 bit/18 bit/ 15 bit /12 bit / 8 bit multiplexed digital inputs to support most of existing industry Embedded controller to provide TV encoder solution.

CH7024 Input Data Format (IDF) are grouped into two major group. These are unitary IDF modes and multiplexed IDF modes. In the unitary IDF mode (Control Register 0Ch, control bit MULTI = 0), all of control bits SWAP, REVERSE and HIGH bit of the control register 0Dh can be used. While, in the multiplexed IDF mode (Control Register 0Ch, control bit MULTI = 1), only REVERSE and HIGH bits are used for IDF5, YCrCb 4:2:2 mode.
For the unitary IDF mode, refer to Table 7 and note for more description or refer to Table 8 for the multiplexed IDF mode.

Table 6: Input Data Formats in single data rate mode (MULTI = 0, see Register 0Dh)

IDF= Format=	PIN	0 RGB888 (standard order)	1 RGB888 (special order)	2 RGB666	3 RGB565	4 RGB555	5 YCrCb4:2:2 (CBCRSW =0)		5 YCbCr4:2:2 (CBCRSW =1)		6 YCbCr4:4:4
Pixel#		P0	P0	P0	P0	P0	P0	P1	P0	P1	P0
Busdata	D[23]	R[7]	R[7]								Y[7]
	D[22]	R[6]	R[6]								Y[6]
	D[21]	R[5]	R[5]	R[5]							Y[5]
	D[20]	R[4]	R[4]	R[4]	R[4]	R[4]					Y[4]
	D[19]	R[3]	R[3]	R[3]	R[3]	R[3]					Y[3]
	D[18]	R[2]	G[7]	R[2]	R[2]	R[2]					Y[2]
	D[17]	R[1]	G[6]	R[1]	R[1]	R[1]					Y[1]
	D[16]	R[0]	G[5]	R[0]	R[0]	R[0]					Y[0]
	D[15]	G[7]	R[2]				Y0[7]	Y1[7]	Y0[7]	Y1[7]	Cr[7]
	D[14]	G[6]	R[1]				Y0[6]	Y1[6]	Y0[6]	Y1[6]	Cr[6]
	D[13]	G[5]	R[0]	G[5]	G[5]		Y0[5]	Y1[5]	Y0[5]	Y1[5]	Cr[5]
	D[12]	G[4]	G[1]	G[4]	G[4]	G[4]	Y0[4]	Y1[4]	Y0[4]	Y1[4]	Cr[4]
	D[11]	G[3]	G[4]	G[3]	G[3]	G[3]	Y0[3]	Y1[3]	Y0[3]	Y1[3]	Cr[3]
	D[10]	G[2]	G[3]	G[2]	G[2]	G[2]	Y0[2]	Y1[2]	Y0[2]	Y1[2]	Cr[2]
	D[9]	G[1]	G[2]	G[1]	G[1]	G[1]	Y0[1]	Y1[1]	Y0[1]	Y1[1]	Cr[1]
	D[8]	G[0]	B[7]	G[0]	G[0]	G[0]	Y0[0]	Y1[0]	Y0[0]	Y1[0]	Cr[0]
	D[7]	B[7]	B[6]				Cr0[7]	Cb0[7]	Cb0[7]	Cr0[7]	Cb[7]
	D[6]	B[6]	B[5]				Cr0[6]	Cb0[6]	Cb0[6]	Cr0[6]	Cb[6]
	D[5]	B[5]	B[4]	B[5]			Cr0[5]	Cb0[5]	Cb0[5]	Cr0[5]	Cb[5]
	D[4]	B[4]	B[3]	B[4]	B[4]	B[4]	Cr0[4]	Cb0[4]	Cb0[4]	Cr0[4]	Cb[4]
	D[3]	B[3]	G[0]	B[3]	B[3]	B[3]	Cr0[3]	Cb0[3]	Cb0[3]	Cr0[3]	Cb[3]
	D[2]	B[2]	B[2]	B[2]	B[2]	B[2]	Cr0[2]	Cb0[2]	Cb0[2]	Cr0[2]	Cb[2]
	D[1]	B[1]	B[1]	B[1]	B[1]	B[1]	Cr0[1]	Cb0[1]	Cb0[1]	Cr0[1]	Cb[1]
	D[0]	B[0]	B[0]	B[0]	B[0]	B[0]	Cr0[0]	Cb0[0]	Cb0[0]	Cr0[0]	Cb[0]

Note: In IDF = 0 mode, 24 bits digital inputs D[23:0]can be assigned to the CH7024 internal RGB registers by either SWAP[2:0] or REVERSE bit via **Control Register** (**Address = 0Dh**) . SWAP controls R, G, B register byte order from the input D[23:0], while REVERSE bit controls reverse 7 bits assignment order within R,G, B registers.

For examples, If **REVERSE bit = 0 and SWAP[2:0] =** 000 , then D[23:0] = R[7:0]G[7:0]B[7:0],
else if **REVERSE bit = 1 and SWAP[2:0]** = 000 , then D[23:0] = R[0:7]G[0:7]B[0:7];
The **HIGH** control bit is used in the unitary mode only. For the **HIGH** bit usage , refer to IDF 2, 3, 4 in the unitary IDF mode.

1. In unitary IDF = 0 mode, RGB888 , from input D[23:0] to internal RGB register as shown below:

If **REVERSE bit = 0 and SWAP[2:0] =** 000 , then D[23:0] = R[7:0]G[7:0]B[7:0];
001 , then D[23:0] = R[7:0]B[7:0]G[7:0];
010 , then D[23:0] = G[7:0]R[7:0]B[7:0];
011 , then D[23:0] = G[7:0]B[7:0]R[7:0];
100 , then D[23:0] = B[7:0]R[7:0]G[7:0];
101 , then D[23:0] = B[7:0]G[7:0]R[7:0].

If **REVERSE bit = 1 and SWAP[2:0]** = 000 , then D[23:0] = R[0:7]G[0:7]B[0:7];
001 , then D[23:0] = R[0:7]B[0:7]G[0:7];
010 , then D[23:0] = G[0:7]R[0:7]B[0:7];
011 , then D[23:0] = G[0:7]B[0:7]R[0:7];
100 , then D[23:0] = B[0:7]R[0:7]G[0:7];
101 , then D[23:0] = B[0:7]G[0:7]R[0:7].

.

2. In unitary IDF = 1, RGB888 special order (see Control Register 0Dh)
{D[23:19],D[15:13],D[18:16],D[11:9],D[12],D[3],D[8:4],D[2:0]} = {R[7:0], G[7:0], B[7:0]}

3. In non-multiplexed IDF = 2, RGB666 (see Control Register 0Dh)

High bit of the Control Register (0Dh), controls insertion of logical value '1' into blank bit within R,G and B registers when input data bits width is less than 8 bit wide. When the High bit = 0, value '1' is inserted to bit 7 and bit 6 of internal R, G and B registers. If High bit = 1 is selected, value '1' is inserted to bit 1 and bit 0 of the CH7024 internal R, G and B registers. (2'b11 means assign corresponding 2 bits with logical value 1 in binary number.)

SWAP: (see Control Register 0Dh)
000 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2b'11} = {R[7:0], G[7:0], B[7:0]};
001 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {R[7:0], B[7:0], G[7:0]};
010 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {G[7:0], R[7:0], B[7:0]};
011 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {G[7:0], B[7:0], R[7:0]};
100 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {B[7:0], R[7:0], G[7:0]};
101 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {B[7:0], G[7:0], R[7:0]}.
110: then {D[17:12],2'b11, D[11:6],2'b11, D[5:0],2'b11} = {R[7:0], G[7:0], B[7:0]};
111: then {D[21:16],2'b11, D[15:14],D[11:8],2'b11, D[5:0],2'b11} = {R[7:0]G[7:0]B[7:0]}.

REVERSE: (see Control Register 0Dh)
0: {D[21:16],2'b11,D[13:8],2'b11,D[5:0],2'b11} = {R[7:0],G[7:0],B[7:0]};
1: {2'b11, D[21:16],2'b11,D[13:8],2'b11,D[5:0]} ={R[0:7],G[0:7],B[0:7]};

HIGH: (see Control Register 0Dh)
0: {2'b11,D[21:16], 2'b11,D[13:8], 2'b11,D[5:0]} = {R[7:0], G[7:0], B[7:0]};
1: {D[23:18],2'b11,D[15:10],2'b11,D[7:2],2'b11} = {R[7:0], G[7:0], B[7:0]};

4. In unitary IDF = 3, RGB565 (see Control Register 0Dh)
(Note: 2'b11 means assign corresponding 2 bits with logical value 1 in binary number.
3'B111 means assign corresponding 3 bits with logical value 1 in binary number.)

SWAP: (see Control Register 0Dh)
000: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
001: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {R[7:0], B[7:0], G[7:0]};
010: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {G[7:0], R[7:0], B[7:0]};
011: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {G[7:0], B[7:0], R7:0]};
100: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {B[7:0], G[7:0], G[7:0]};
101: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {B[7:0], G[7:0], B[7:0]};
110: {D[15:11],3'b111,D[10:5],2'b11,D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
111: {D[20:16],3'b111,D[15:14],D[11:8],2'b11,D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]}.

REVERSE: (see Control Register 0Dh)
0: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
1: {3'b111, D[20:16], 2'b11, D[13:8], 3'b111,D[4:0]} = {R[0:7], G[0:7], B[0:7]};

HIGH: (see Control Register 0Dh)
0: {3'b111,D[20:16], 3'b11,D[13:8], 3'b111,D[4:0]} = {R[7:0], G[7:0], B[7:0]};
1: {D[23:19],3'b111, D[15:10],2'b11, D[7:3],3'b111} = {R[7:0], G[7:0], B[7:0]};

5. In unitary IDF = 4, RGB555 (see Control Register 0Dh)
(3'B111 means assign corresponding 3 bits with logical value 1 in binary number.)
SWAP: (see Control Register 0Dh)
000: {D[20:16],3'b111, D[12:8],3'b111, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
001: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {R[7:0], B[7:0], G[7:0]};
010: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {G[7:0], R[7:0], B[7:0]};
011: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {G[7:0], B[7:0], R7:0]};
100: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {B[7:0], G[7:0], G[7:0]};
101: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {B[7:0], G[7:0], B[7:0]};
110: {D[14:10],3'b111, D[9:5],3'b111, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
111: {D[20:16],3'b111, D[14],D[11:8],3'b111, D[4:0],3'b111} = {R[7:0],G[7:0],B[7:0]}.
REVERSE: (see Control Register 0Dh)
0: {D[20:16],3'b111,D[12:8],3'b111,D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
1: {3'b111,D[20:16], 3'b111,D[12:8], 3'b111,D[4:0]} = {R[0:7], G[0:7], B[0:7]};
HIGH: (see Control Register 0Dh)
0: {3'b111,D[20:16], 3'b111,D[12:8], 3'b111,D[4:0]} = {R[7:0], G[7:0], B[7:0]};
1: {D[23:19],3'b111, D[15:11],3'b111, D[7:3],3'b111} = {R[7:0], G[7:0], B[7:0]};

6. In unitary IDF = 5, YCbCr 4:2:2 (see Control Register 0Dh)
Note that only the SWAP[0] bit is used in this mode.
SWAP: (see Control Register 0Dh)
xx0: D[15:0] = Y[7:0]C[7:0];
xx1: D[15:0] = C[7:0]Y[7:0];
REVERSE: (see Control Register 0Dh)
0: D[15:0] = Y[7:0]C[7:0];
1: D[15:0] = Y[0:7]C[0:7];
HIGH: (see Control Register 0Dh)
0: D[15:0] = Y[7:0]C[7:0]; (non-multiplexed format only)
1: D[23:8] = Y[0:7]C[0:7]; (non-multiplexed format only)

7. In unitary IDF = 6, YCbCr 4:4:4 (see Control Register 0Dh)
SWAP: (see Control Register 0Dh)
000: D[23:0] = Y[7:0], Cr[7:0], Cb[7:0];
001: D[23:0] = Y[7:0], Cb[7:0], Cr[7:0];
010: D[23:0] = Cr[7:0], Y[7:0], Cb[7:0];
011: D[23:0] = Cr[7:0], Cb[7:0], Y[7:0];
100: D[23:0] = Cb[7:0], Y[7:0], Cr[7:0];
101: D[23:0] = Cb[7:0], Cr[7:0], Y[7:0];
REVERSE: (see Control Register 0Dh)
0 : D[23:0] = Y[7:0], Cr[7:0], Cb[7:0].
1 : D[23:0] = Y[0:7], Cr[0:7], Cb[0:7].

In RGB666, RGB565, RGB555, the RGB data are continuously distributed when SWAP[2:0] = 110 .

Table 7: Multiplexed Input Data Formats (MULTI = 1, see Register 0Dh)

IDF = Format =	PIN	0 RGB888 (standard order)		1 RGB888 (special order)		5 YCrCb4:2:2 (CBCRSW =0)		5 YCbCr4:2:2 (CBCRSW =1)		6 YCbCr4:4:4	
Pixel #		P0a	P0b	P0a	P0b	P0a	P0b	P0a	P0b	P0a	P0b
Bus Data	D[11]	G[3]	R[7]	G[4]	R[7]					Y[3]	Cr[7]
	D[10]	G[2]	R[6]	G[3]	R[6]					Y[2]	Cr[6]
	D[9]	G[1]	R[5]	G[2]	R[5]					Y[1]	Cr[5]
	D[8]	G[0]	R[4]	B[7]	R[4]					Y[0]	Cr[4]
	D[7]	B[7]	R[3]	B[6]	R[3]	Cr0[7]	Y1[7]	Cb0[7]	Y0[7]	Cb[7]	Cr[3]
	D[6]	B[6]	R[2]	B[5]	G[7]	Cr0[6]	Y1[6]	Cb0[6]	Y0[6]	Cb[6]	Cr[2]
	D[5]	B[5]	R[1]	B[4]	G[6]	Cr0[5]	Y1[5]	Cb0[5]	Y0[5]	Cb[5]	Cr[1]
	D[4]	B[4]	R[0]	B[3]	G[5]	Cr0[4]	Y1[4]	Cb0[4]	Y0[4]	Cb[4]	Cr[0]
	D[3]	B[3]	G[7]	G[0]	R[2]	Cr0[3]	Y1[3]	Cb0[3]	Y0[3]	Cb[3]	Y[7]
	D[2]	B[2]	G[6]	B[2]	R[1]	Cr0[2]	Y1[2]	Cb0[2]	Y0[2]	Cb[2]	Y[6]
	D[1]	B[1]	G[5]	B[1]	R[0]	Cr0[1]	Y1[1]	Cb0[1]	Y0[1]	Cb[1]	Y[5]
	D[0]	B[0]	G[4]	B[0]	G[1]	Cr0[0]	Y1[0]	Cb0[0]	Y0[0]	Cb[0]	Y[4]

1 **In multiplexed IDF** = 5, YCbCr 4:2:2 (see Control Register 0Dh)
Note that only the SWAP[0] bit is used in this mode.

SWAP: (see Control Register 0Dh)

xx0 : D[15 :0] = Y[7 :0]C[7 :0] ;

xx1 : D[15 :0] = C[7 :0]Y[7 :0] ;

REVERSE: (see Control Register 0Dh)

0 : D[7 :0] = Y[7 :0]/C[7 :0] ;

1 : D[7 :0] = Y[0 :7]/C[0 :7] ;

The multiplexed input data format is shown in **Figure 6** below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel.

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

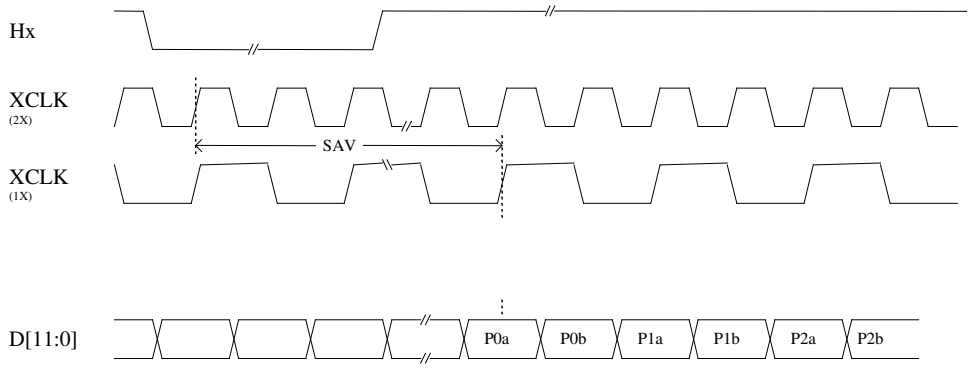

Figure 6: 12-bit Multiplexed Input Data Formats

In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connect error and correct it automatically, for example, if the input P14 and P15 are a group, but you take P13 and P14 as a group, the hardware can detect this error and correct it by run-in code.

2.3 TV Output

2.3.1 TV Output Format

The CH7024 support the following output formats:

Table 8: Supported SDTV standards

No.	Standards	Field Rate (Hz)	Total	Scan Type
0	NTSC-M	60/1.001	858x525	Interlaced
1	NTSC-J	60/1.001	858x525	Interlaced
2	NTSC-443	60/1.001	858x525	Interlaced
3	PAL-B/D/G/H/I	50	864x625	Interlaced
4	PAL-M	50	864x625	Interlaced
5	PAL_N	50	864x625	Interlaced
6	PAL-Nc	50	864x625	Interlaced
7	PAL_60	60/1.001	858x525	Interlaced

2.3.2 Video DAC Outputs

Table 10 below lists the DAC output configurations of the CH7024.

Table 9: Video DAC Configurations for CH7024

Output Type of 48 pin LQFP	DACA0=CVBS or DACA0=Y	DAC1-C/CVBS
Single CVBS	CVBS	off
Dual CVBS	CVBS	CVBS
S-video	Y	C

2.3.3 DAC single/double termination

The DAC output of CH7024 can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. See also the description of SEL_R bit of the Control Register 63h

2.3.4 TV connection detect

CH7024 support detecting the TV connection by setting the SENSEEN bit of the Control Register 62h**.** It can detect which DAC are connected, short to ground or not connected. So it can distinguish single CVBS connected with other connection, but it can not distinguish dual CVBS connected with S-video connected. See also the DUCVBS bit description of the Control Register 0Ch and the SVD/DDAC bit description of the Control Register 0Ah.

2.3.5 TV picture adjustment

The CH7024 has the capability of vertical and horizontal output picture position adjustment. The CH7024 will automatically put the picture in the display center, and the position is also programmable through user input. The CH7024 also provides brightness/sharpness/contrast, hue and saturation adjustments.

2.3.6 TV reference clock output

The CH7024 support operating in Clock Master Mode. The CH7024 integrates the low jitter PLL to generate a reference clock for the graphics controller for reference.

2.3.7 Color Sub-carrier Generation

The CH7024 has two ways to generate the color sub-carrier frequency. If the XCLK from the graphics controller has a steady center frequency and very small jitters, the sub-carrier can be derived from the XCLK. However, since even a ±0.01% sub-carrier frequency variation is enough to cause some TV to lose color lock, CH7024 has the ability to generate the sub-carrier frequency from the crystal when the XCLK from the graphics device cannot meet the requirement. In this case, the crystal has to be present. In other words, the only configuration where the off-chip crystal can be removed is when slave mode is used and the graphics controller provides XCLK with required characteristics.

In addition, the CH7024 has the capability to unlock the color sub-carrier with Vsync. Also, CH7024 has the ability to operate in a "stop dot crawl" mode for NTSC CVBS output when the first sub-carrier generation method is used.

2.3.8 ITU-R BT.470 Compliance

The CH7024 is mostly compliant with ITU-R BT.470 standard except for the items below.

- The frequencies of horizontal sync, vertical sync, and color sub-carrier depend on the quality of XCLK from graphics controller and/or the off-chip crystal.
- It is assumed that gamma correction, if required, is performed in the graphics device.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements. However, they may have a small variation depending on the actual input and output format.
- The actual bandwidths of the luminance and chrominance signals depend on the filter selection.

3.0 REGISTER CONTROL

The CH7024 is controlled via a serial control port. The serial bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device should retain all register values during power down modes.

3.1 Control Registers Index

Table 10: Serial Port Register Map

Name	Description	Address
A[31:0]	POUT divider ratio	24h-27h
ACIV	Sub-carrier generation method	1Ch
BRI[7:0]	Brightness Control	08h
BSTADJ[2:0]	Burst amplitude adjust	1Ch
CBCRSW	The order of CbCr component in the YcbCr4:2:2 input format.	10h of page 2
CBW	Chroma filter bandwidth	0Fh
CFBP	Chroma filter bypass	0Fh
CFRB	Sub-carrier periodic reset	0Fh
CKINV	Clock for input latch inversion	1Dh
CTA[6:0]	Contrast Control	07h
DACCKINV	DAC clock inversion	1Dh
DACSW[1:0]	DAC Switch	0Ah
DCKSEL	DCLK/PCLK selector	0Ch
DES	Decode embedded sync	0Eh
DID[7:0]	Device ID	00h
DIFFEN	Enable differential mode for input	0Eh
DKINV	DCLK inversion	1Dh
DOTCRB	Dot crawl reduction	1Ch
DUCVBS	Enable two CVBS output	0Ch
FLDS	Field selection	0Eh
FLDSEN	Field selection enable	0Eh
FPD	Full power down	04h
FSCISPP[15:0]	Sub-carrier frequency adjustment in free-running mode	32h, 33h
HAI[10:0]	Input H active	11h, 12h
HIGH	Input data alignment	0Dh
HTI[10:0]	Input H total	11h, 13h
HO[10:0]	Input H sync offset	14h, 15h
HP[9:0]	Horizontal position control	22h, 23h
HPO	H sync polarity	0Eh
HUE[6:0]	Hue control	05h
HW[9:0]	Input H sync width	14h, 16h
HVAUTO	Input timing auto generation	11h
IDF[2:0]	Input data format	0Dh
MULTI	Multiplexed data indicator	0Ch
N[23:0]	N value for UCLK divider	2Bh-2Dh
P[23:0]	P value for UCLK divider	28h-2Ah
PDDAC[1:0]	DAC power down	04h
PG	Select Control Register Map page	02h
PKINV	PCLK inversion	1Dh
PLL1N1[2:0]	PLL1 pre-divider ratio	2Fh
PLL2N2[2:0]	PLL2 pre-divider ratio	2Fh
PLL3N3[2:0]	PLL3 pre-divider ratio	30h
PLL3N4[2:0]	PLL3 post-divider 1 ratio	30h
PLL3N5[2:0]	PLL3 post-divider 2 ratio	31h
POUTEN	Enable POUT for master mode	0Eh

Name	Description	Address
RESETDB	Reset data path, active low	03h
RESETIB	Reset register map, active low	03h
REVERSE	Input data reverse	0Dh
SAT[6:0]	Saturation Control	06h
SCFREQ[26:0]	Value for calculate sub-carrier frequency from crystal	34h-37h
SEL_R	DAC termination indicator	63h
SENSEEN	Enable DAC sense	62h
SVD/DDAC	S-Video enable/dual DAC output enable	0Ah
SWAP[2:0]	Input data swap	0Dh
SYO	Sync direction	0Eh
T[7:0]	T value for UCLK divider	2Eh
TE[2:0]	Text enhancement control	09h
TV_BP	Bypass mode. TV_BP register controls interlace or non-interlace.	0Ah
TVHA[10:0]	Output H active	1Eh, 1Fh
UKINV	UCLK inversion	1Dh
VAI[9:0]	Input V active	17h, 18h
VID[7:0]	Version ID	01h
VOS[3:0]	Video output format selection	0Ah
VP[9:0]	Vertical position control	20h, 21h
VTI[9:0]	Input V total	17h, 19h
VW[5:0]	Input V sync width	1Bh
XCH	XCLK and data rate	0Fh
XTAL[3:0]	Preset crystal frequency index	0Bh
XTALSEL	Preset crystal frequency selection	0Bh
YCV[1:0]	CVBS luma filter	0Fh
YSV[1:0]	S-Video luma filter	0Fh

3.2 Control Registers Map

CH7024 has two pages of control register Index maps and the PG[bit 0] of the control register 02h select either control register index page 1 or 2 . Note that the control register index page 2 is used for IDF 5 YcrCb 4:2:2 input mode selection only. Otherwise, the control register index page1 should be used for the other control functions.

Table 11: Control Register Index (page 1)

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
01h	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
02h								PG
03h							RESETIB	RESETDB
04h					PDDAC[1]	PDDAC[0]		FPD
05h		HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]
06h		SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
07h		CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
08h	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
09h						TE[2]	TE[1]	TE[0]
0Ah	TV_BP	SVD/DDAC	DACSW[1]	DACSW[0]	VOS[3]	VOS[2]	VOS[1]	VOS[0]
0Bh	XTALSEL				XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]
0Ch	DUCVBS	DCKSEL						MULTI
0Dh	HIGH	REVERSE	SWAP[2]	SWAP[1]	SWAP[0]	IDF[2]	IDF[1]	IDF[0]
0Eh	POUTEN		DES	FLDSEN	FLDS	VPO	SYO	DIFFEN
0Fh	XCH	CFRB	CFBP	CBW	YSV[1]	YSV[0]	YCV[1]	YCV[0]
10h	UPSCL					AFF[2]	AFF[1]	AFF[0]
11h	HVAUTO		HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
12h	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
13h	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
14h				HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
15h	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
16h	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
17h			VO[9]	VO[8]	VTI[9]	VTI[8]	VAI[9]	VAI[8]
18h	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
19h	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
1Ah	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
1Bh			VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
1Ch				ACIV	BSTADJ[2]	BSTADJ[1]	BSTAJ[0]	DOTCRB
1Dh				DACCKINV	DKINV	PKINV	CKINV	UKINV
1Eh						TVHA[10]	TVHA[9]	TVHA[8]
1Fh	TVHA[7]	TVHA[6]	TVHA[5]	TVHA[4]	TVHA[3]	TVHA[2]	TVHA[1]	TVHA[0]
20h							VP[1]	VP[0]
21h	VP[9]	VP[8]	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]
22h							HP[1]	HP[0]
23h	HP[9]	HP[8]	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]
24h	A[31]	A[30]	A[29]	A[28]	A[27]	A[26]	A[25]	A[24]
25h	A[23]	A[22]	A[21]	A[20]	A[19]	A[18]	A[17]	A[16]
26h	A[15]	A[14]	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]
27h	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
28h	P[23]	P[22]	P[21]	P[20]	P[19]	P[18]	P[17]	P[16]
29h	P[15]	P[14]	P[13]	P[12]	P[11]	P[10]	P[9]	P[8]
2Ah	P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]
2Bh	N[23]	N[22]	N[21]	N[20]	N[19]	N[18]	N[17]	N[16]
2Ch	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]
2Dh	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]
2Eh	T[7]	T[6]	T[5]	T[4]	T[3]	T[2]	T[1]	T[0]
2Fh			PLL2N2[2]	PLL2N2[1]	PLL2N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
30h			PLL3N4[2]	PLL3N4[1]	PLL3N4[0]	PLL3N3[2]	PLL3N3[1]	PLL3N3[0]

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
31h						PLL3N5[2]	PLL3N5[1]	PLL3N5[0]
32h	FSCISPP[15]	FSCISPP[14]	FSCISPP[13]	FSCISPP[12]	FSCISPP[11]	FSCISPP[10]	FSCISPP[9]	FSCISPP[8]
33h	FSCISPP[7]	FSCISPP[6]	FSCISPP[5]	FSCISPP[4]	FSCISPP[3]	FSCISPP[2]	FSCISPP[1]	FSCISPP[0]
34h						SCFREQ[26]	SCFREQ[25]	SCFREQ[24]
35h	SCFREQ[23]	SCFREQ[22]	SCFREQ[21]	SCFREQ[20]	SCFREQ[19]	SCFREQ[18]	SCFREQ[17]	SCFREQ[16]
36h	SCFREQ[15]	SCFREQ[14]	SCFREQ[13]	SCFREQ[12]	SCFREQ[11]	SCFREQ[10]	SCFREQ[9]	SCFREQ[8]
37h	SCFREQ[7]	SCFREQ[6]	SCFREQ[5]	SCFREQ[4]	SCFREQ[3]	SCFREQ[2]	SCFREQ[1]	SCFREQ[0]
62h	SENSEEN							
63h							SEL_R	
7Eh			ATTACH2[1]	ATTACH2[0]	ATTACH1[1]	ATTACH1[0]	ATTACH0[1]	ATTACH0[0]

Table 12: Control Register Index (page 2)

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h					CBCRSW			

3.3 Control Register Descriptions

3.3.1 Control Register Descriptions (Index Map Page 1)

Device ID Register **Address: 00h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	1	**0**	0	0	1	0	1

Bits[7:0] The DID bits indicate the CH7024 device ID. This register is read-only and the value is 45h.

Revision ID Register **Address: 01h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

Bits [7:0] The VID bits indicate the CH7024 revision ID.

Page Selection Register **Address: 02h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	reserved	reserved	reserved	reserved	reserved	reserved	reserved	PG
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bit 0 The PG is for page selection. This register is physically the same for both page 1 and page 2.
When PG is '0', 1st page of the control register index map page is selected . Otherwise, 2nd page is selected.

Reset Register **Address: 03h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESETIB	RESETDB
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

Bits [7:2] are reserved.

Bit [1] The RESETIB bit resets all control registers. When RESETIB is '0', the control registers are reset to power-on default values. The RESETIB bit must be toggled back to '1' to resume normal operation of the control registers.

Bit [0] The RESETDB bit resets all internal circuit data path except serial bus control circuit. When RESETDB is '0', the data path is reset. The RESETDB bits must be toggled back to '1' to resume normal CH7024 operation.

Changing the state of RESETDB will not affect the content of the control registers.

Power State Register

Address: 04h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	PDDAC[1]	PDDAC[0]	Reserved	FPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	1

Bit [7:4], Bit[1] are reserved.

Bit [3] The PDDAC[1] bit is the power-down control for DAC1. DAC1 is powered down when this bit is set to '1'.

Bit [2] The PDDAC[0] bit is the power-down control for DAC0. DAC0 is powered down when this bit is set to '1'.

Bit [0] The FPD bit controls CH7024 power on/off state. When FPD is "0", CH7024 is in power-on state. When FPD is "1", CH7024 is in power-down state. During the power-down state, the serial buses will still remain active.

TV Hue Control Register

Address: 05h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	0	0	0	0	0

Bit [7] is reserved.

Bits [6:0] The HUE bits adjust hue setting of the image. The color can be tuned based on the formula – (HUE[6:0]-64)/2 degrees. The power-on default angle is 0 degree. The weight of magenta color will be increased if the degree of angle is getting more positive. The weight of green color will be increased if the degree of angle is getting more negative.

TV Saturation Control Register

Address: 06h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	0	0	0	0	0

Bit [7] is reserved.

Bits [6:0] The SAT bits adjust the color saturation of the image.

TV Contrast Control Register

Address: 07h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	0	0	0	0	0

Bit [7] is reserved.

Bits [6:0] The CTA bits adjust the contrast level of the image. Each increment will increase a level of contrast and vise versa.

TV Brightness Control Register

Address: 08h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bits [7:0] This register adjusts the brightness level of the image. Each increment will increase a level of brightness and vise versa.

TV Sharpness Control Register

Address: 09h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	TE[2]	TE[1]	TE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	0

Bits [7:3] are reserved.

Bits [2:0] The TE bits control the sharpness (text enhancement) adjustment of the image. In default, bits [2:0] are set to '100' for normal operation. Setting values higher than the power-on default will boost the high frequency band of the image. In contrast, setting values less than the power-on default will soften the image.

Video Output Format Register

Address: 0Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TV_BP	SVIDEO	DACSW[1]	DACSW[0]	VOS[3]	VOS[2]	VOS[1]	VOS[0]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	0	0	0

Bit [7] The TV_BP bit determines whether or not the scaler engine will be used to process the image. In default, the scaler engine is enabled. This bit is used to select interlace or non-interlace mode. "1" turns on the interlace mode.

Bit [6] The SVIDEO bit is a switch between S-Video and Composite outputs. When this bit is '1', the DACs will output S-Video signal, otherwise the Composite signal will be generated.

Bits [5:4] The DACSW bits control the DACs output (Table 14).

Table 13: DAC switch control settings

DACSW[1:0]	Note
00	ALL DAC output switched off
01 (CVBS format)	DAC0 output CVBS signal
10 (S-Video format)	DAC0 output Y signal, DAC1 output C signal
11	Reserved (Invalid state)

Bits [3:0] The VOS bits define CH7024 video output format (Table 15).

Table 14 : Video Output Format VOS[3 :0]

VOS[3 :0]	Video Output formats
0000	NTSC_M
0001	NTSC_J
0010	NTSC_443
0011	PAL_B/D/G/H/K/I
0100	PAL_M
0101	PAL_N
0110	PAL_Nc
0111	PAL_60

Crystal Control Register

Address: 0Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	XTALSEL	Reserved	Reserved	Reserved	XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	0

Bit [7] The XTALSEL bit activates the predefined crystal frequency in XTAL[3:0]. When this bit is '0', the predefined value on the XTAL [3:0] will be used to save programming effort. When this bit is '1', other CH7024 timing control registers need to be programmed.

Bits [6:4] are reserved.

Bits [3:0] The XTAL bits predefine crystal frequencies as the followings:

[3:0] = '0000': 3.6864MHz,
[3:0] = '0001': 3.579545MHz,
[3:0] = '0010': 4MHz,
[3:0] = '0011': 12MHz,
[3:0] = '0100': 13MHz,
[3:0] = '0101': 13.5MHz,
[3:0] = '0110': 14.318MHz,
[3:0] = '0111': 14.7456MHz,
[3:0] = '1000': 16MHz,
[3:0] = '1001': 18.432MHz,
[3:0] = '1010': 20MHz,
[3:0] = '1011': 26MHz,
[3:0] = '1100': 27MHz,
[3:0] = '1101': 32MHz,
[3:0] = '1110': 40MHz,
[3:0] = '1111': 49MHz.

Input Data Format Register 1 Address: 0Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DUCVBS	DCKSEL	Reserved	Reserved	Reserved	Reserved	Reserved	MULTI
TYPE:	R/W	R/W	R/W	R/W	**R/W**	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bit [7]: The DUCVBS bit will output CVBS signal on both DACs. When this bit is '0', only DAC0 will output CBVS signal. When this bit is '1', both DAC1 and DAC2 will output CVBS signal.

Bit [6] The DCKSEL bit indicates whether the DCLK or the PCLK is supplied by the host graphic controller. If this bit is '0', the PCLK is selected, otherwise the DCLK is chosen.

Bits [5:1] are reserved.

Bit [0] The MULTI bit indicates whether or not the input data will be multiplexed. When is bit is set to '1', the input data is multiplexed and will be latched during the falling edge and the rising edge at each clock cycle.

Input Data Format Register 2 Address: 0Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	**HIGH**	REVERSE	SWAP[2]	SWAP[1]	SWAP[0]	IDF[2]	IDF[1]	IDF[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bit [7] The HIGH bit aligns the input data to start on the higher order of D[23:0] pins. Please refer to Section 2.2.4 for detail.

Bit [6] The REVERSE bit will reverse the order of input data format if it's set to '1'. For example: R[7:0] -> R[0:7], G[7:0] -> G[0:7] and B[7:0] -> B[0:7]. Please refer to Section 2.2.4 for detail.

Bits [5:3] The SWAP bits will change the order of RGB or YUV components. Please refer to Section 2.2.4 for detail.

Bits [2:0] The IDF bits define the input data format. Please refer to Section 2.2.4 for details.

SYNC Control Register Address: 0Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	POUTEN	DES	FLDSEN	FLDS	HPO	VPO	SYO	DIFFEN
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	1	0	0

Bit [7] The POUTEN bit enables the pixel clock output through POUT pin. It also serves as an indicator for master and slave mode selection. If this bit is set to '1', the CH7024 will behave as a master and output pixel clock frequency through POUT pin.

Bit [6] The DES bit defines decoding the embedded input sync type. If this bit is set to '1', input sync are encoded inside the input data, otherwise input sync are independent with input data.

Bit [5] The FLDSEN bit enable FLD field select function. If this bit is set to '1', it enable FLD field selection Otherwise disable FLD function of field selection..

Bit [4] The FLDS bit select either odd or even output filed when FLDSEN bit is enabled. If this bit is set to '1', output odd fields; otherwise output even fields.

Bit [3] The HPO bit selects the polarity of input horizontal sync. If this bit is set to '1', the polarity is positive; otherwise the polarity is negative.

Bit [2] The VPO bit selects the polarity of vertical sync. If this bit is set to '1', the polarity is positive; otherwise the polarity is negative.

Bit [1] The SYO bit determines the direction of sync. If this bit is set to '0', input sync is expected; otherwise CH7024 will generate a output sync.

Bit [0] The DIFFEN bit enables the pseudo differential input mode when it is set to '1'. Otherwise, the CMOS input mode is enable. Refer section 2.2.3 input data voltage for more information.

TV Filter Register 1

Address: 0Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	XCH	CFRB	CFBP	CBW	YSV[1]	YSV[0]	YCV[1]	YCV[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bit [7] The XCH bit indicates how the input data will be latched. If this bit is '1', data will be latched in both rising edge and falling edge.

Bit [6] The CFRB will reset the color burst period if it's set to '1'. Toggle this bit back to '0' to resume the normal operation.

Bit [5] The CFBP bit controls bypass TV Chroma filter. If this bit is set to '1', bypass TV Chroma filter, otherwise enable TV Chroma filter.

Bit [4] The CBW bit controls TV Chroma bandwidth. If this bit is set to "1', increase TV Chroma bandwidth, otherwise decrease the TV Chroma bandwidth.

Bits [3:2] These YSV bits define the S-video Luma channel bandwidth control. Larger YSV value results in higher luma channel bandwidth.

Bits [1:0] These YCV bits define the Composite Luma channel bandwidth. Larger YCV value results in higher luma channel bandwidth.

TV Filter Register 2

Address: 10h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	AFF[2]	AFF[1]	AFF[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	1

Bits [6:3] are reserved.

Bits [2:0] The AFF bits control the CH7024 TV adaptive flicker filter. Higher value means stronger De-flicker effect.

Input Timing Register 1 Address: 11h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HVAUTO	Reserved	HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	0	0	1

Bit [7] The HVAUTO bit determines how the input timing information can be achieved. If this bit is '0', the timing information will be obtained from HTI, HAI (registers from 11h to 1Bh). If this bit is '1', the CH7024 internal circuitry will automatically calculate for the input timing.

Bits [6] is reserved.

Bits [5:3] This is the upper two bits of HTI. It combines with HTI [7:0] to form an 11-bits Input Horizontal Total Pixels.

Bits [2:0] This is the upper two bits of HAI. It combines with HAI[7:0] to form an 11-bits Input Horizontal Active Pixels.

Input Timing Register 2 Address: 12h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	0	0	0	0	0

Bits [7:0] The HAI[7:0] bits combine with HAI[10:8] to form an 11-bits Input Horizontal Active Pixels.

Input Timing Register 3 Address: 13h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bits [7:0] The HTI[7:0] bits combine with HTI[10:8] to form an 11-bits Input Horizontal Total Pixels.

Input Timing Register 4 Address: 14h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:5] are reserved.

Bits [4:3] The HW[9:8] bits combine with HW[7:0] to form a 10-bits Input Horizontal Sync Pulse Width.

Bits [2:0] The HO[10:8] bits combine with HO[7:0] to form an 11-bits Input Horizontal Sync Offset.

Input Timing Register 5

Address: 15h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	0

Bits [7:0] The HO[7:0] bits combine with HO[10:8] to form an 11-bits Input Horizontal Sync Offset.

Input Timing Register 6

Address: 16h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	1	0

Bits [7:0] The HW[7:0] bits combine with HW[9:8] to form a 10-bits Input Horizontal Sync Pulse Width.

Input Timing Register 7

Address: 17h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VO[9]	VO[8]	VTI[9]	VTI[8]	VAI[9]	VAI[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [6:7] are reserved.

Bits [5:4] The VO[9:8] bits combine with VO[7:0] to form a 10-bits Input Vertical Sync Offset.

Bits [3:2] The VTI[9:8] bits combine with VTI[7:0] to form a 10-bits Input Vertical Total Pixels.

Bits [1:0] The VAI[9:8] bits combine with VAI[7:0] to form a 10-bits Input Vertical Active Pixels.

Input Timing Register 8

Address: 18h

BIT :	7	6	5	4	3	2	1	0
SYMBOL :	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	0	0	0	0

Bits [7:0] The VAI[7:0] bits combine with VAI[9:8] to form a 10-bits Input Vertical Active Pixels.

Input Timing Register 9 Address: 19h

BIT :	7	6	5	4	3	2	1	0
SYMBOL :	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	0	1	1

Bits [7:0] The VTI[7:0] bits combine with VTI[9:8] to form a 10-bits Input Vertical Total Pixels.

Input Timing Register 10 Address: 1Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	0

Bits [7:0] The VO [7:0] bits combine with VO[9:8] to form a 10-bits Input Vertical Sync Offset.

Input Timing Register 11 Address: 1Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	1	1

Bits [7:6] are reserved.

Bits [5:0] The VW[5:0] bits define the Input Vertical Sync Pulse Width.

Burst Amplitude Adjustment Register Address: 1Ch

BIT :	7	6	5	4	3	2	1	0
SYMBOL :	Reserved	Reserved	Reserved	ACIV	BSTADJ[2]	BSDADJ[1]	BSDADJ[0]	DOTCR13
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bits [7:5] are reserved.

Bit [4] The ACIV bit determines if the FSCI value will be used to set the sub-carrier frequency. When the ACIV value is '1', the content of the Sub-carrier Frequency registers (34h to 37h) will be used to calculate the sub-carrier frequency. When the ACIV value is '0', CH7024 will automatically calculate the sub-carrier frequency.

Whenever this bit is set to '1', the CFRB bit should be set to '0'.

Bits [3:1] The BSTADJ bits define the SDTV reference burst amplitude adjustment as shown in Table 16.

Table 15: SDTV reference burst amplitude adjustment BSTADJ[2:0]

BSTADJ[2:0]	Function
PAL, PAL-Nc,	
111	-28mV
110	-14mV
000	Nominal
001	+14mV
010	+28mV
011	+42mV
100	+56mV
101	+70mV
NTSC-M,NTSC443	
111	-4 IRE
110	-2 IRE
000	Nominal
001	+2 IRE
010	+4 IRE
011	+6 IRE
100	+8 IRE
101	+10 IRE
PAL-M/N	
111	-28mV
110	-14mV
000	Nominal
001	+14mV
010	+28mV
011	+42mV
100	+56mV
101	+70mV
NTSC-J	
111	-4 IRE
110	-2 IRE
000	Nominal
001	+2 IRE
010	+4 IRE
011	+6 IRE
100	+8 IRE
101	+10 IRE

Bit [0] The DOTCRB bit enables TV Dot Crawl reduction when set to ‘1’ otherwise disables Dot Crawl reduction.

Clock Tree Control Register

Address: 1Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	DACCKINV	DKINV	PKINV	CKINV	UKINV
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	1	1	1	0	0

Bits[7:5] are reserved.

DACCKINV (bit 4) inverts the DAC clock.

DKINV (bit 3) inverts the DCLK.

PKINV (bit 2) inverts the PCLK.

CKINV (bit 1) inverts the clock for input latch.

UKINV (bit 0) inverts the UCLK.

Output Timing Register 1

Address: 1Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	TVHA[10]	TVHA[9]	TVHA[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	1

Bits [7:3] are reserved.

Bits [2:0] TVHA[10:8] bits combine with TVHA[7:0] to form an 11 bits TV Output Horizontal Active pixels.

Output Timing Register 2

Address: 1Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TVHA[7]	TVHA[6]	TVHA[5]	TVHA[4]	TVHA[3]	TVHA[2]	TVHA[1]	TVHA[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	1	0	0	0	0	0

Bits [7:0] TVHA[7:0] bits combine with TVHA[10:8] to form an 11 bits TV Output Horizontal Active pixels.

TV Vertical Position Register 1

Address: 20h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VP[1]	VP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:2] are reserved.

Bits [1:0] VP[1:0] bits combine with VP[9:2] to form a 10 bits TV vertical position adjustment.

TV Vertical Position Register 2 Address: 21h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VP[9]	VP[8]	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bits [7:0] VP[9:2] bits combine with VP[1:0] to form a 10-bits TV vertical position adjustment.

The number of lines to be adjusted can be calculated by the formula: VP[9:0]-512. If the result is positive, the image will move up. If the result is negative, the image will be move down.

TV Horizontal Position Register 1 Address: 22h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HP[1]	HP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:2] are reserved.

Bits [1:0] The HP[1:0] bits combine with HP[9:2] to form a 10-bits TV horizontal position adjustment.

TV Horizontal Position Register 2 Address: 23h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HP[9]	HP[8]	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bits [7:0] The HP[9:2] bits combine with HP[1:0] to form a 10-bits TV horizontal position adjustment.

The number of pixels to be adjusted can be calculated by the formula: HP[9:0]-512. If the result is positive, the image will move to the right. If the result is negative, the image will move to the left.

PCLK Clock Divider Register 1 Address: 24h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A[31]	A[30]	A[29]	A[28]	A[27]	A[26]	A[25]	A[24]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	0

Bits [7:0]: The A[31:24] bits combine with A[23:16], A[15:8] and A[7:0] to form a 32-bits clock divider for PCLK.

*Program CH7024 PLL registers (24h to 31h) for particular pixel clock frequency can be complicated. Please contact Chrontel for further detail.

PCLK Clock Divider Register 2 Address: 25h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A[23]	A[22]	A[21]	A[20]	A[19]	A[18]	A[17]	A[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:0] The A[23:16] bits combines with A[31:24], A[15:8] and A[7:0] to form a 32-bits clock divider for PCLK.

PCLK Clock Divider Register 3 Address: 26h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A[15]	A[14]	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:0] The A[15:8] bits combine with A[31:24], A[23:16] and A[7:0] to form a 32-bits clock divider for PCLK.

PCLK Clock Divider Register 4 Address: 27h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:0] The A[7:0] bits combine with A[31:24], A[23:16] and A[15:8] to form a 32-bits clock divider for PCLK.

Clock Divider Numerator Register 1 Address: 28h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	P[23]	P[22]	P[21]	P[20]	P[19]	P[18]	P[17]	P[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	1	1

Bits [7:0] The P[23:16] bits combine with P[15:8] and P[7:0] to form a 24-bits the clock divider numerator.

Clock Divider Numerator Register 2 Address: 29h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	P[15]	P[14]	P[13]	P[12]	P[11]	P[10]	P[9]	P[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	1	1	1	1

Bits [7:0] The P[15:8] bits combine with P[23:16] and P[7:0] to form a 24-bits the clock divider numerator.

Clock Divider Numerator Register 3 Address: 2Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	1	1	0	0	0

Bits [7:0] The P[7:0] bits combine with P[15:8] and P[23:16] to form a 24-bits clock divider numerator.

Clock Divider Denominator Register 1 Address: 2Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N[23]	N[22]	N[21]	N[20]	N[19]	N[18]	N[17]	N[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	1	0	0

Bits [7:0] The N[23:16] bits combine with N[15:8] and N[7:0] to form a 24-bits denominator of Digital Divider for UCLK.

Clock Divider Denominator 2 Register 2 Address: 2Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	1	0	1	0	1

Bits [7:0] The N[15:8] bits combine with N[23:16] and N[7:0] to form a 24-bits denominator of Digital Divider for UCLK.

Clock Divider Denominator 2 Register 3 Address: 2Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	1	0	0

Bits [7:0] The N[7:0] bits combine with N[23:16] and N[15:8] to form a 24-bits denominator of Digital Divider for UCLK.

Clock Divider Integer Register Address: 2Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	T[7]	T[6]	T[5]	T[4]	T[3]	T[2]	T[1]	T[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	1	0	1	1	0

Bits [7:0] This register sets the M value for PLL.

PLL Ratio Register 1

Address: 2Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	PLL2N2[2]	PLL2N2[1]	PLL2N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	0	1	0

Bits [7:6] are reserved.

Bits [5:3] The PLL2N2 bit provides a setting of the video PLL2 pre-divider

Bits [2:0] The PLL1N1 bit provides a setting of the video PLL1 pre-divider

PLL Ratio Register 2

Address: 30h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	PLL3N4[2]	PLL3N4[1]	PLL3N4[0]	PLL3N3[2]	PLL3N3[1]	PLL3N3[0]
Bits [5:3]:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	0	1	0	0	1

Bits [7:6] are reserved.

Bits [5:3] The PLL3N4 bits provide the setting of the video PLL3 post-divider 1.

Bits [2:0] The PLL3N3 bits provide the setting of the video PLL3 pre-divider.

PLL Ratio Register 3

Address: 31h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	PLL3N5[2]	PLL3N5[1]	PLL3N5[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	1	0	0

Bits [7:3] are reserved.

Bits [2:0] The PLL3N5 bits provide the setting of the video PLL3 post-divider 2.

FSCI Adjustment Register 1

Address: 32h

BIT :	7	6	5	4	3	2	1	0
SYMBOL :	FSCISPP[15]	FSCISPP[14]	FSCISPP[13]	FSCISPP[12]	FSCISPP[11]	FSCISPP[10]	FSCISPP[9]	FSCISPP[8]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:0] The FSCISPP [15:8] bits combine with FSCISPP [7:0] to form a 16-bits adjustment control to the TV sub-carrier frequency. Also, the FSCI registers in 0x32h-0x33h are used for calculating the sub-carrier frequency, the formula is: SCFREQ = (FSCI / Fs) * (2 ^ 26), in which, Fs is the crystal clock frequency. The FSCISPP uses 2's compliment. Each step is 12.87Hz and the adjustment range is between –421KHz and 421KHz.

FSCI Adjustment Register 2 Address: 33h

BIT :	7	6	5	4	3	2	1	0
SYMBOL :	FSCISPP[7]	FSCISPP[6]	FSCISPP[5]	FSCISPP[4]	FSCISPP[3]	FSCISPP[2]	FSCISPP[1]	FSCISPP[0]
TYPE :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:0] The FSCISPP[7:0] bits combine with FSCISPP[15:8] to form a 16-bits adjustment control to the TV sub-carrier frequency. The FSCISPP uses 2's compliment. Each step is 12.87Hz and the adjustment range is between –421KHz and 421KHz.

Sub-carrier Frequency Register 1 Address: 34h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	SCFREQ[26]	SCFREQ[25]	SCFREQ[24]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	1

Bits [7:3] are reserved.

Bits [2:0] The SCFREQ[26:24] bits combine with SCFREQ[23:16], SCFREQ[15:8], and SCFREQ[7:0] to form a 27 bits sub-carrier frequency adjustment.

SCFREQ = (Fsc / Fs) * (2 ^ 26)
Fsc is the desired sub-carrier frequency. There are five values of sub-carrier frequency (Table 17)

Table 16: The sub-carrier frequency

NTSC-M/J	3.579545 MHz
NTSC-M/J, no dot Crawl	3.57956 MHz
PAL-M	3.57561149 MHz
PAL-N/B/D/G/H/K/I, PAL-60	4.43361875 MHz
PAL-Nc	3.58205625 MHz

Note: the PAL-M frequency in the ITU-R.BT.470-6 has a typo. The correct value should be the one shown above.

Fs is the sampling rate (crystal clock frequency). The crystal clock frequency range is from 2.3 MHz to 64 MHz

Sub-carrier Frequency Register 2 Address: 35h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCFREQ[23]	SCFREQ[22]	SCFREQ[21]	SCFREQ[20]	SCFREQ[19]	SCFREQ[18]	SCFREQ[17]	SCFREQ[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	1	0	0	1

Bits [7:0] The SCFREQ[23:16] bits combine with SCFREQ[26:24], SCFREQ[15:8], and SCFREQ[7:0] to form a 27 bits sub-carrier frequency adjustment.

Sub-carrier Frequency Register 3 Address: 36h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCFREQ[15]	SCFREQ[14]	SCFREQ[13]	SCFREQ[12]	SCFREQ[11]	SCFREQ[10]	SCFREQ[9]	SCFREQ[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	0	1	0	1

Bits [7:0] The SCFREQ[15:8] bits combine with SCFREQ[26:24], SCFREQ[23:16], and SCFREQ[7:0] to form a 27 bits sub-carrier frequency adjustment.

Sub-carrier Frequency Register 4 Address: 37h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCFREQ[7]	SCFREQ[6]	SCFREQ[5]	SCFREQ[4]	SCFREQ[3]	SCFREQ[2]	SCFREQ[1]	SCFREQ[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	1	1	1	1	1

Bits [7:0] The SCFREQ[7:0] bits combine with SCFREQ[26:24], SCFREQ[23:16], and SCFREQ[15:8] to form a 27 bits sub-carrier frequency adjustment.

DAC trimming register Address: 62h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SENSEEN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	0	1	0	0

Bit [7] The SENSEEN bit is the TV connection detection register. Toggle this bit will generate a pulse to detect the presence of TV.

TV Detection procedure is the following: Toggle this bit to '1' and then read the status on ATTACH2[1:0], ATTACH1[1:0] and ATTACH0[1:0]from register 7Eh to determine the connection on the DACs. Toggle the SENSEEN bit back to '0' after the connection status is read.

Bits [6:0] are reserved

Data I/O register Address: 63h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEL_R	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	**0**	0	0	0

Bits [7:2] are reserved.

Bit [1] The SEL_R bit indicates the termination of the DAC. When this bit is '0', single termination (no 75ohm on PCB) is selected. Double termination (both 75 ohm on PCB and TV side) is chosen if this bit is '1'.

Bit [0] is reserved.

Attached Display Register Address: 7Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	ATTACH2[1]	ATTACH2[0]	ATTACH1[1]	ATTACH1[0]	ATTACH0[1]	ATTACH0[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0

Bits [7:6] are reserved.

Bits [5:4] The ATTACH2[1:0] bits return the status of TV detection (Table 18) – The C channel only

Table 17: Attached Display Mapping for S-Video C channel

ATTACH2[1:0]	Attached Display
00	No Attached Display
01	S-Video C channel Connected
10	S-Video C channel Short Connected
11	Reserved

Bit [3:2] The ATTACH1[1:0] bits return the status of TV detection (Table 19) – The Y channel only

Table 18: Attached Display Mapping for S-Video Y channel

ATTACH1[1:0]	Attached Display
00	No Attached Display
01	S-Video Y channel Connected
10	S-Video Y channel Short Connected
11	Reserved

Bits [1:0] The ATTACH0[1:0] bits return the status of TV detection (Table 20) – for Composite Video only

Table 19: Attached Display Mapping for for Composite Video channel

ATTACH0[1:0]	Attached Display
00	No Attached Display
01	Composite Video Display Connected
10	Composite Video Display Short Connected
11	Reserved

3.3.2 Control Register Descriptions (Index Map Page 2)

Below are the descriptions for Control Registers 10h of page 2.

CBCR Input Switch Register **Address: 10h**

	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	CBCRSW	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bit [3] The CBCRSW bit switches the order of CrCb component in the YcrCb4:2:2 input format .
When CBCRSW is set to '0', it is selects IDF 5 of YcrCb 4:2:2. Otherwise, it selects IDF5 of YcrCb in Input data
Default is YcrCb 4:2:2 input data format. Refer to section 2.2.4 Input data format for more information.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
VDD18	All 1.8V power supplies relative to GND	-0.5		2.5	V
VDD33	All 3.3V power supplies relative to GND	-0.5		5.0	V
VDDIO	Input voltage of all digital pins (see note)	GND – 0.5		VDDIO+0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 seconds)			260	°C
	Vapor phase soldering (11 seconds)			245	°C
	Vapor phase soldering (60 seconds)			225	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the recommended operating condition of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V may cause permanent damage to the device.

The digital input voltage will follow the I/O supply voltage (VDDIO). The I/O supply voltage range is from 1.2V to 3.3V

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Crystal and I/O Power Supply Voltage	3.1	3.3	3.5	V
AVDD_DAC	DACs Power Supply Voltage	3.1	3.3	3.5	V
AVDD_PLL	PLL Power Supply Voltage	1.71	1.8	1.89	V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
VDDIO	Data I/O supply voltage	1.1		3.5	V
RL1	Output load to DAC Current Reference Pin ISET		1.2k		Ω
RL2	Output load to DAC Outputs, Pins CVBS, Y, and C		37.5 75 ◈2		Ω
VDD18	Generic for all 1.8V supplies	1.71	1.8	1.89	V
VDD33	Generic for all 3.3V supplies	3.1 ◈3	3.3	3.5	V
T_{AMB}	Ambient operating temperature (Commercial / Automotive Grade 4)	0		70	°C
T_{AMB}	Ambient operating temperature (Industrial / Automotive Grade 3)	-40		85	°C

Note ◈2: Single terminated.
Note ◈3: Except otherwise indicated.

4.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD18=1.8V± 5%, VDD33=3.3V± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		34		mA
	Video level error			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		32		mA
I_{VDD33}	Total VDD33 supply current (3.3V supplies) (See Note)		25		mA
I_{PD}	Total Power Down Current		< 20		uA

Note: The VDD33 supply current is 18mA for one DAC single 75-Ohm termination. The current will be 35mA for one DAC double 75-Ohm termination (37.5Ohm). For two DACs, the current will be doubled according to different termination.

4.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD33 + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DATAIH}	Data Input High Voltage (see Note 1)		VDDIO/2+0.25		VDDIO + 0.5	V
V_{DATAIL}	Data Input Low Voltage		GND-0.5		VDDIO/2-0.25	V
V_{MISCIH}	Miscellaneous Input High Voltage (see Note 2)		2.7		VDD33 + 0.5	V
V_{MISCIL}	Miscellaneous Input Low Voltage		GND-0.5		0.6	V
I_{MISCPU}	Miscellaneous input Pull Up Current	V_{IN} = 0V	0.5		5.0	uA
$V_{P-OUTOH}$	P-OUT Output High Voltage	I_{OH} = - 0.4mA	VDD18-0.2			V
$V_{P-OUTOL}$	P-OUT Output Low Voltage	I_{OL} = 4 mA			0.2	V

Note :

1. Data input means the following pins: D[23:0], XCLK, H, V and DE. VDDIO is the I/O supply voltage. The range is from 1.2V to 3.3V.
2. Vmisc means the following pins: AS, RESET*.

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$f_{CRYSTAL}$	Input (CRYSTAL) frequency		2.3		64	MHz
f_{XCLK}	Input (XCLK) frequency		2.3		64	MHz
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_S	Setup Time: D[23:0], H, V and DE to XCLK	XCLK to D[23:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[23:0], H, V and DE to XCLK	D[23:0], H, V, DE = Vref to XCLK	0.5			ns
t_R	Pout, Output Rise Time (20% - 80%)	15pF load VDD33= 3.3V, VDD18=1.8V			1.50	ns
t_F	Pout Output Fall Time (20% - 80%)	15pF load VDD33=3.3V, VDD18=1.8V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

4.6 ESD Rating

2KV HBM per JEDEC standard JESD22-A114C.

5.0 PACKAGE DIMENSIONS

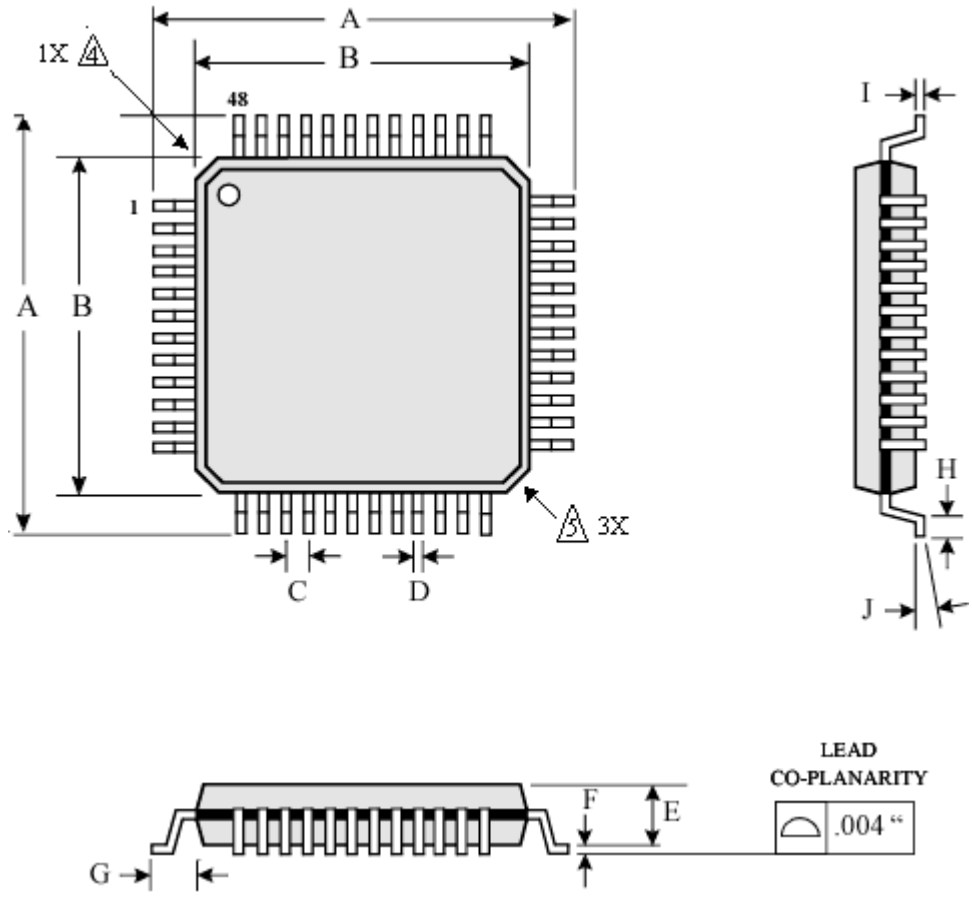

Figure 7: 48 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
48 (7 X 7 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	9	7	0.5	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D
2. Dimension B: Top package body size may be smaller than bottom package size by as much as 0.15mm
3. Dimension B does not include allowable mold protrusions up to 0.25mm per side

4. (1X) Corner in quadrant with pin1 identifier (dot) is always chamfered. Exact shape of chamfer is optional.

5. (3X) Corner in quadrants without pin1 identifier (dot) may be square or chamfered. Exact shape of chamfer is optional.

6.0 REVISION HISTORY

Rev. #	Date	Section	Description
1.0	6/6/2006	-	Official release.
1.1	12/15/2006	1.2.1, 1.2.2	Updated Pin Description.
1.11	1/15/2007	4.1, 4.2	Updated Section 4.1 and 4.2
1.12	2/8/2007	3.3.1	Corrected Register 0Fh YCV[1] and Register 1Ch BSTADJ bit corrected to Bits[3:1].
1.13	4/25/2007	5.0	Updated Figure 8, 49-Pin TFBGA package drawing.
1.14	6/8/2007	2.2.4	Corrected Table 8.
1.15	2/19/2008	2.2.4 3.3.1	Corrected Table 8. Updated Register:1Dh, (Clock Tree Control Register).
1.16	9/30/2009	2.2.4	Corrected Table 7, Table 8.
2.0	4/2/2012	All	Discontinued TFBGA package. All references were removed.
3.0	8/14/2012	4.0, 5.0	Removed CH7023 product. Updated ambient operating temperature into Commercial / Automotive Grade 4 and Industrial / Automotive Grade 3. Modified some “Absolute Maximum rating”. Added some notes for “Package Dimensions”.
3.1	1/7/2014	4.1, 4.2	Move T_{AMB} from 4.1 to 4.2.
3.2	4/29/2016	1.2, 2.2, 3.1, 3.2, 3.3,	Add some chip pin description. Add some register pin description. Add an input diagram to help understand symbol meaning. Correct some mistakes.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply	Temperature Grade
CH7024B-DF	Lead-free LQFP with Exposed pad	48	1.8V & 3.3V	Commercial / Automotive Grade 4
CH7024B-DF-I	Lead-free LQFP with Exposed pad	48	1.8V & 3.3V	Industrial / Automotive Grade 3
CH7024B-DF-TR	Lead-free LQFP with Exposed pad	48	1.8V & 3.3V	Commercial / Automotive Grade 4
CH7024B-DF-I-TR	Lead-free LQFP with Exposed pad	48	1.8V & 3.3V	Industrial / Automotive Grade 3

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